Intel740™ Graphics Accelerator

Design Guide

August 1998

Order Number: 290619-003

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Revision History

Date	Revision	Description
2/98	-001	Initial Release.
4/98	-002	Part 2: Added Figure 2-2; added “Note” verbiage in 2.14. Part 3: Added verbiage to 3.3.5; Modified Figures 3-14, 3-15, 3-16, 3-19; Modified Table 3-10. Part 5: Modified Figure 5-6.
7/98	-003	Restructured document and added a motherboard design: Chapter 2 contains the Addin Card design. This chapter combines revision 2 Chapters 1, 2, 3, and Appendix A. Only re-organizaiton; the information is the same. Chapter 2 adds the motherboard design.

1

Introduction

Introduction 1

This document provides a complete package of design information for the Intel740™ Graphics Accelerator. There are two design discussed:

- ATX Addin Card Design (Chapter 2 provides design considerations, layout and routing guidelines, and schematic diagrams)
- Motherboard Design (Chapter 3 provides design considerations, layout and routing guidelines, and schematic diagrams)

The purpose of the reference design is to provide a comprehensive design encompassing every Intel740™ graphics accelerator interface. The designer of another board may then modify this design as needed since the basic hook-up will remain the same.

For the latest Intel740™ graphics accelerator information, please visit Intel's website at:

http://developer.intel.com/design/graphics/740.htm

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- This chapter introduces the designer to the organization and purpose of this design guide and provides a list of references and related documents.
- Chapter 2, "Addin Card Design"—This chapter provides a detailed set of Intel740™ graphics accelerator design information for ATX and NLX graphics cards. The basis of the design information is a reference ATX card design. Schematics for the reference design are provided at the end of the chapter.
- Chapter 3, "3 Device AGP Motherboard Design"—This chapter provides design guidelines for developing a motherboard based on the Pentium II® processor, Intel® 440BX AGPset, and the Intel740™ graphics accelerator. The main focus of this chapter is the guidelines for developing a 3-point AGP solution with the Intel740 graphics accelerator and provides a detailed set of design information for a 3-point AGP reference design (DS1P/440BX/I740). Schematics for the reference design are provided at the end of the chapter.
- Chapter 4, "Thermal Considerations"—This chapter introduces the topic of thermal considerations. See *Application Note 653* in Appendix A for a comprehensive description of thermal considerations.
- Chapter 5, "Mechanical Information"— This chapter provides mechanical information on Fan/Heatsink, VMI Header Placement, Video Connector, brackets, and NLX considerations.
- Chapter 6, "Third Party Vendor Information"— This section includes information regarding various third-party vendors who provide products to support the Intel 440BX AGPset and the Intel740 graphics accelerator.
- Appendix A, "Application Notes"—This appendix contains *Application Note 653, Thermal Design Considerations*. The application note provides a comprehensive guide to thermal design
- Appendix B, "Reference Information"—This appendix provides reference information for designing with the Intel740 graphics accelerator. The appendix contains information on

SDRAM/SGRAM Graphics SO-DIMM Modules. The appendix also contains information on PC SGRAM specifications.

1.2 References

- Intel740™ Graphics Accelerator Datasheet: Contact your field sales representative (Literature order #290618) or visit the Intel740™ Graphics Accelerator WEB page at: http://developer.intel.com/design/graphics/740.htm
- Accelerated Graphics Port Interface Specification Rev 1.0: Contact www.agpforum.com
- Bt829A/Bt827A/Bt825A VideoStreamII Decoders Oct. 1996: Contact Rockwell* Semiconductor
- Bt868/869 Flicker-Free Video Encoder with Ultrascale^{TM} Technology: Contact Rockwell* Semiconductor
- VMI 1.4 Interface Specification: Contact SGS Thompson Microelectronics
- PC ’98: Contact www.microsoft.com/hwdev
- PC SGRAM Specification: See Appendix B
- SO-DIMM Module Specification: See Appendix B
- Intel740™ Graphics Accelerator Application Note 653 - Thermal Design Considerations: See Appendix A
- Intel 440BX AGPset Design Guide. Contact your field sales representative (Literature order #290634). or visit the 440BX AGPSet WEB page at: http://developer.intel.com/design/pcisets/designex/290634.htm

2

Intel740™ Graphics Accelerator Addin Card Design

Addin Card Design 2

This chapter provides a complete package of design information for the Intel740™ graphics accelerator. Usage of the Intel740™ graphics accelerator on an ATX and NLX graphics card is discussed. The basis of this document is a reference ATX card.

2.1 Introduction

The reference design card described in this document contains the following features.

- ATX Form Factor
- Memory
  - 100 MHz SDRAM or SGRAM
  - SO-DIMM Memory Upgrade Socket
  - 2,4 MB Solder-Down Option
- BIOS
  - Support for Flash or ROM
  - Capable of Supporting up to 256KB
- Monitor
  - Hardware Support for DDC 2B
- Video
  - Capture
    - Bi-Directional VMI Video Port for DVD Hardware
    - CCIR 601 8/16-bit Video Capture Port
    - NTSC, PAL, and SECAM Inputs Accepted
    - Intercast Capable
    - Video-Conferencing Capable
  - Output
    - NTSC or PAL TV Output
    - Flicker Free TV Output
    - Overscan Compensation
  - 50-Pin Video Connector
    - S-Video In/Out
    - Composite In/Out
    - TV Tuner
- I^2C Programmability

Table 2-1 lists the various functions capable of being supported by the reference card design. This table describes which component is necessary for a specific feature. For hookup information, the corresponding schematic page should be referenced.

Table 2-1. Mix and Match Options For Intel740™ Graphics Accelerator Card

Component/ Functionality	Intel740™ Graphics Accelerator Page 3	BT829 Page 5	BT869 Page 6	DVD Chip/ Daughter Card Page 7	SO-DIMM Module Page 11	Memory Components Page 12
2D/3D	X					
Video Capture	X	X				
TV Out	X		X			
DVD (HW)	X			X		
2 MB	X				(1) 256K x 64	(2) 256K x 32
4 MB	X				(1) 512K x 64 or (2) 256K x 64	(2) 512K x 64 or (4) 256K x 32
8 MB	X				(1) 1M x 64	(4) 1M x 16

2.1.1 Design Features

2.1.1.1 Intel740™ Graphics Accelerator

The Intel740™ graphics accelerator is the main component of the graphics reference design. This component delivers high performance 3D/2D graphics and video capabilities. Each of the interfaces are described below.

- **Accelerated Graphics Port (AGP) Interface.** The AGP interface is a new interface designed for 3D graphics. This interface provides increased bandwidth over PCI, side band addressing, and AGP memory 3D texture storage. For a more complete description of the AGP interface refer to the Intel740™ Graphics Accelerator Datasheet and AGP Specification.
- **Local Memory Interface.** The memory interface on the Intel740™ graphics accelerator can operate at speeds up to 100 MHz. An SDRAM interface supports SGRAM and SDRAM to be used for different memory densities.
- **VMI Interface.** A bi-directional VMI like port is incorporated into the Intel740™ graphics accelerator providing a mechanism for affordable DVD. Video capture is also supported using the video port pins.
- **TV Out Interface.** Intel has worked with Rockwell* (Brooktree*) to design an interface capable of supporting a high quality TV out chip. This interface allows the Intel740™ graphics accelerator to output on a monitor, TV, or both.
- **BIOS Interface.** The Intel740™ graphics accelerator supports a FLASH or ROM BIOS. Up to 256Kx8 can be supported.
- **GPIO Interface.** Nine GPIO signals exist on the Intel740™ graphics accelerator. GPIO[8:0] allow for power management, DDC, I^2C, thermal fault sensing, and other general features.
- **DAC Interface.** An integrated DAC provides display resolutions up to 1600x1200.

2.1.2 BT829B - Video Decoder

The Bt829B is a video capture processor used to convert analog video data into CCIR 601 digital video data. This chip contains the following capabilities.

- **Analog Inputs.** The Bt829B contains four composite video inputs along with one chroma and one luma input for s-video.
- **I^{2}C Interface.** Control of the Bt829B is accomplished though the use of an I^{2}C interface. All of the chip's registers are programmed using this interface as is the selection of the analog input source to use in generating digital video data.
- **Video Port.** The Bt829B contains a video port capable of outputting 8 or 16 bit data. The data format is YUV 4:2:2 with HSYNC, VSYNC, and PIXEL CLOCK as control signals.

2.1.2.1 BT869 - TV Encoder

The Bt869 provides high quality TV out. This component contains the following interfaces:

- **Input Port.** The Bt869 is capable of receiving data in two formats. The format used by this reference design for receiving data is through the 24 bit digital port accepting data on both edges of the reference clock. This mode of operation is documented in the *Intel740™ Graphics Accelerator Datasheet*. The second method for capturing data is through the use of the VMI protocol. This interface is documented in the *VMI 1.4 Interface Specification*.
- **Flicker Filter Output.** The output of the Bt869 is a very high quality flicker filtered output. This is due to a 5 tap internal filter. Output can be displayed in interlaced, non-interlaced, PAL, or NTSC formats. Macrovision7 output is also supported in the Bt869 component. The Bt869 is capable of displaying composite or S-Video data.
- **I^{2}C Interface.** Control of the Bt869 is achieved through the I^{2}C port.

2.1.3 Terminology

2.1.3.1 Power Sources

The card is supplied with four voltages through the edge connector. Other voltages are derived on-board. Thus, the Power Layer of the board must be divided into several distinct planes. Table 2-2 lists the various power elements on the Intel740™ graphics accelerator reference design. Each of the voltage sources are supplied by a plane except for 12 volts, which is supplied by a 25 mil trace.

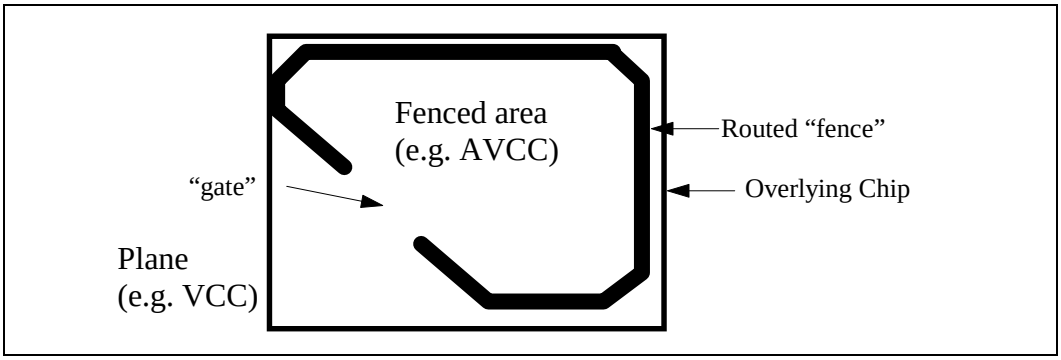
Table 2-2. Intel740™ Graphics Accelerator Power Supplies

Schematic Symbol	Description	Voltage	Max Current	Source
VDDQ3	3.3V AGP Supply	+3.3V	8.0A	Edge connector
VCC3	3.3V Logic Supply	+3.3V	6.0A	Edge connector
VCC	5V Logic Supply	+5.0V	2.0A	Edge connector
+12V	12V Supply	+12V	1.0A	Edge connector
VCC2	2.7V Core Supply	+2.7V	3.0A	VCC3, via Voltage Regulator
3VAA_BT869	3.3V Analog Supply	+3.3V	< 1.0A	VCC3, via Ferrite Bead
AVCC	5V Analog Supply	+5.0V	< 1.0A	VCC, via "fence"

2.1.3.2 Fences

A “fence” is a line routed out of the plane such that a given area is isolated from the rest of the plane except at a single point of contact, conceptually the “gate” in the fence. A fence will minimize noise originating from digital signaling onto the analog signals. This provides higher quality video for both the Bt829B and Bt869. An example of a fenced power plane is shown in Figure 2-1. The heavy black line is the routed area. The width of the gate or opening can be up to 75% of the length of the IC in question. The width of the routed fence should conform to the separation routing between power planes (i.e., 25 mils minimum).

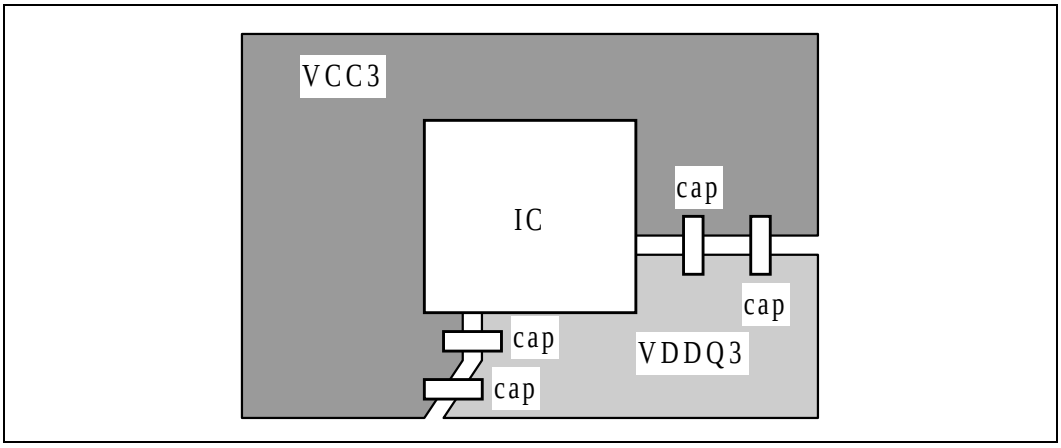
Figure 2-1. Example of Power Plane Separation ("fencing")



2.1.3.3 Stitching

Power plane “stitching” is required between the VCC3 and VDDQ3 planes. Stitching two isolated planes together with capacitors allows a current return path for high frequency signals which pass over split power planes. This helps to eliminate EMI. The six 0.1 µF capacitors coupling VCC3 to VDDQ3 should be spaced evenly if possible. Note the VDDQ3 plane is only near the AGP connector. An example of stitching is shown in Figure 2-2. This figure illustrates the power planes and, therefore, does not show signal traces between capacitors. The general rule for power plane stitching is to have a capacitor placed between every four signals crossing the two planes. As an example, there should be a capacitor, four signals, a capacitor, another four signals, and so forth ending with a capacitor.

Figure 2-2. Example of Power Plane Stitching



2.2 Layout and Routing Guidelines

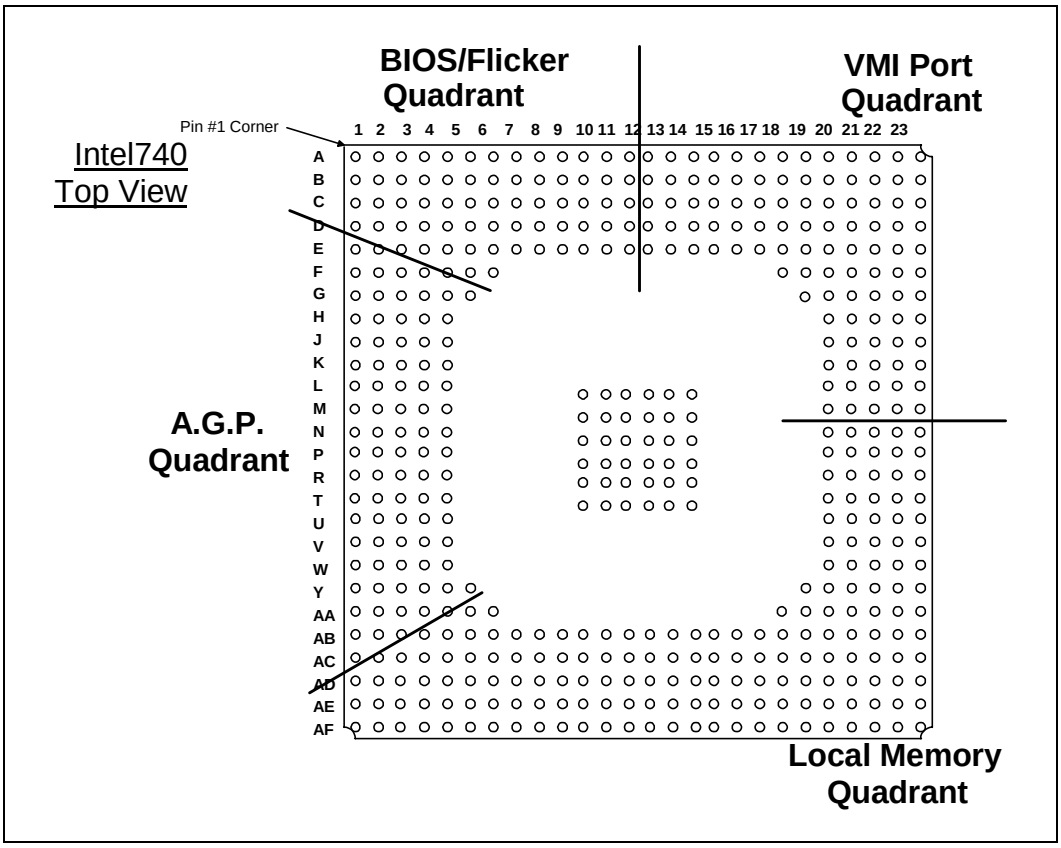
This chapter describes layout and routing recommendations to insure a robust design. These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

2.2.1 Placement

The ball connections on the Intel740™ graphics accelerator have been assigned to simplify routing and keep board fabrication costs down by enabling a 4-layer design. Figure 2-3 shows the four signal quadrants of the Intel740 graphics accelerator. Component placement should be done with this general flow in mind. This will simplify routing and minimize the number of signals which must cross. The individual signals within the respective groups have also been optimized to be routed using only 2 PCB layers.

A complete list of signals and ball assignments can be found in the Intel740™ Graphics Accelerator Datasheet.

Figure 2-3. Major Signal Sections

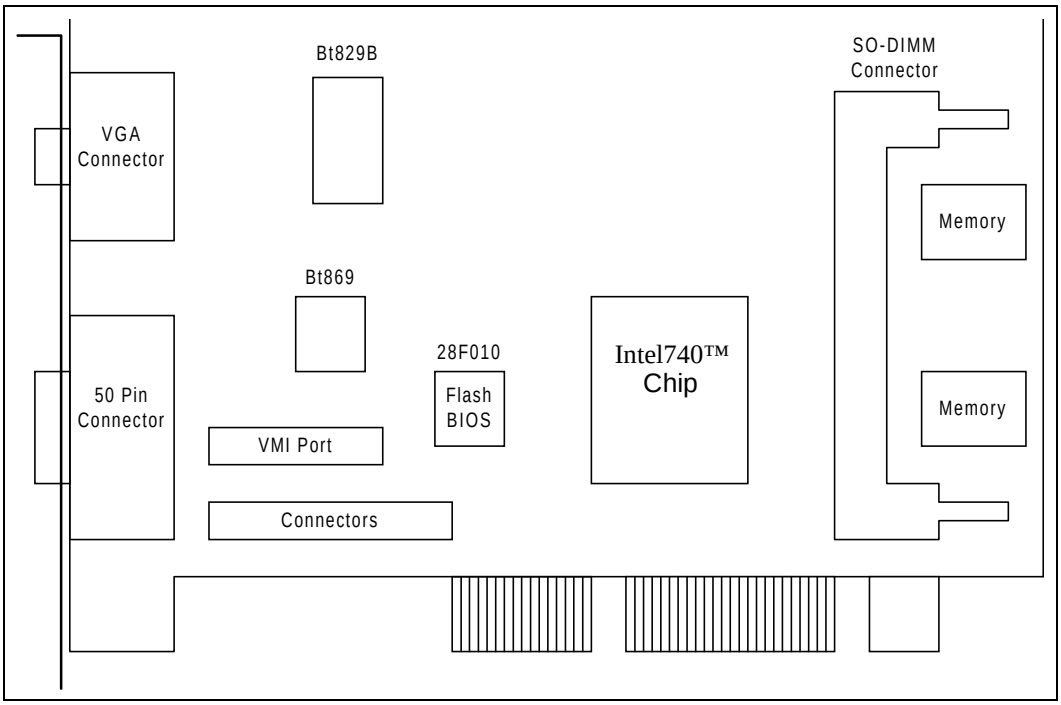


An example of the proposed component placement for an ATX form factor design is shown in Figure 2-4. This is the placement used on the reference card. For NLX placement issues, refer to Section 5.6, “NLX Considerations” on page 5-5.

ATX Form Factor:

- The example placement (Figure 2-4) shows the Bt829B, Bt869, SO-DIMM Module, Intel740 graphics accelerator, VMI Port connections along with a 50 pin video connector.
- The trace length limitation between critical connections will be addressed later in this document.
- Figure 2-4 is for ***reference only***. The choice of size of memory, whether to have an SO-DIMM connector, what video components to place on the board, and which video connectors to have on the bracket will have to be evaluated by the board designer.

Figure 2-4. Example ATX Layout

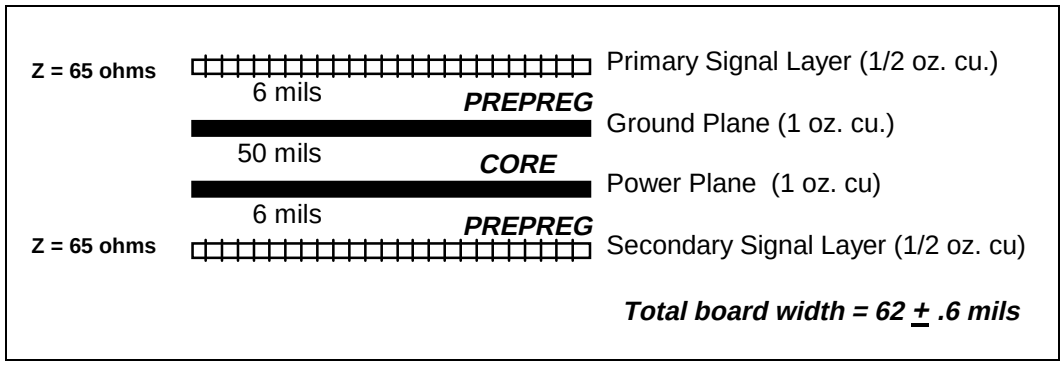


2.2.2 Board Description

Even with the following recommendations, it is important to simulate your design.

A 4-layer stack-up arrangement is recommended. The stack-up of the board is shown in Figure 2-5. The impedance of all the signal layers are to be between 50 and 80 ohms. Lower trace impedance will slow signal edge rates, over & undershoot, and have less cross-talk than higher trace impedance. Higher trace impedance will create faster edge rates and decrease signal flight times. Prepreg is FR-4 material.

Figure 2-5. Four Layer Board Stack-up



Note: Top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will end up with about 1 oz. cu. Please check with your fabrication vendor on the exact value and insure that any signal simulation accounts for this.

Note: Thicker core helps reduce board warpage issues, while thinner prepreg reduces trace impedance.

Additional guidelines on board buildup, placement and layout include:

- All layers should be cut back from the substrate outer edge by 0.050". A 0.025"-wide strip should be added to all signal and power layers around the outer edge and tied to the ground plane.
- All power and ground traces between vias and pads for all components should be at least as wide as the component power or ground pad itself.
- Through-hole vias, unless otherwise noted, are 10 mil drill, 25 mil diameter pad. Via capping is required. All vias on the secondary side should be covered with solder mask. All vias on the primary side are to be encroached with solder mask and anti-pad unless board dryness has been guaranteed.
- To minimize solder wicking with the BGA, the component side solder mask should be applied prior to tinning the copper. There should be no surface mount over bare copper (S.M.O.B.C.).
- The solder mask must cover the trace between the via and pad.
- The board impedance (Z) should be between 50 and 80 ohms (65 ohms ±20%).
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on a VCC plane, not the ground plane.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.
- Keep isolated power planes as close as possible to each other. This will minimize impedance mismatch at the split.
- All decoupling capacitors should be tied to the ground plane by a trace at least as wide as the via ring to the plane.

2.2.3 BGA Component

2.2.3.1 Layout Requirements

The following layout requirements should be followed when routing the 468 MBGA package.

- All non-ground BGA lands should be Metal Defined (MD) lands with the following nominal dimensions (see Figure 2-6).
  - — Metal pad: 20 (6/6 routing) / 24 mils (5/5 routing)
  - — Solder mask opening: 24 mil (20 mil pad) / 27 mils (24 mil pad)
- Any trace connected to a MBGA land or PTH via in the MBGA land grid array should be teardropped. The teardrop should leave the trace at a 45° angle and intersect the via tangentially (see Figure 2-7).
- The minimum distance between the gold finger edge of the card and the center of the first row of MBGA lands should be 525 mils, and 480 mils from the end of the start of the bevel.
- All BGA ground vias should use 16 mil drill with **no thermal reliefs**.

Figure 2-6. Metal Defined land dimensions

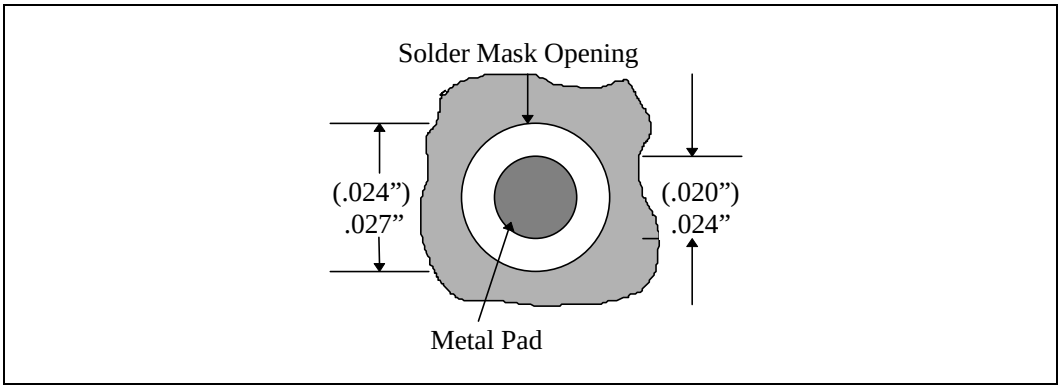
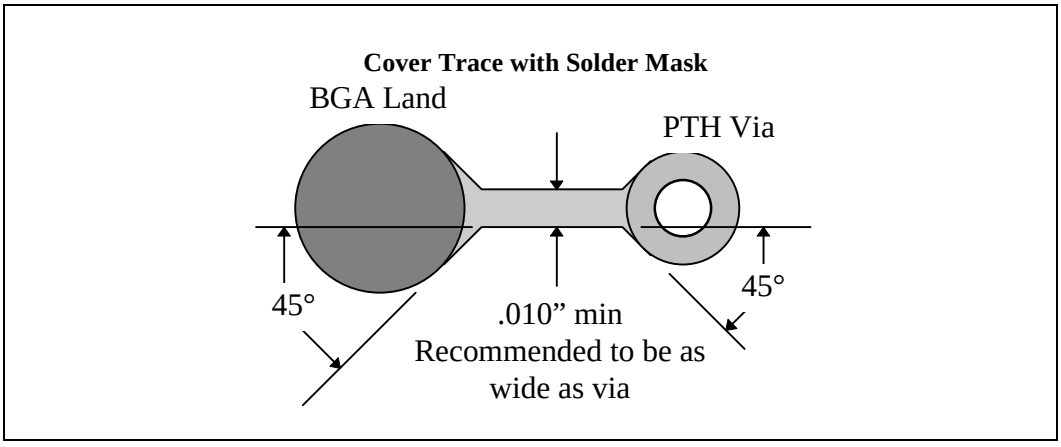


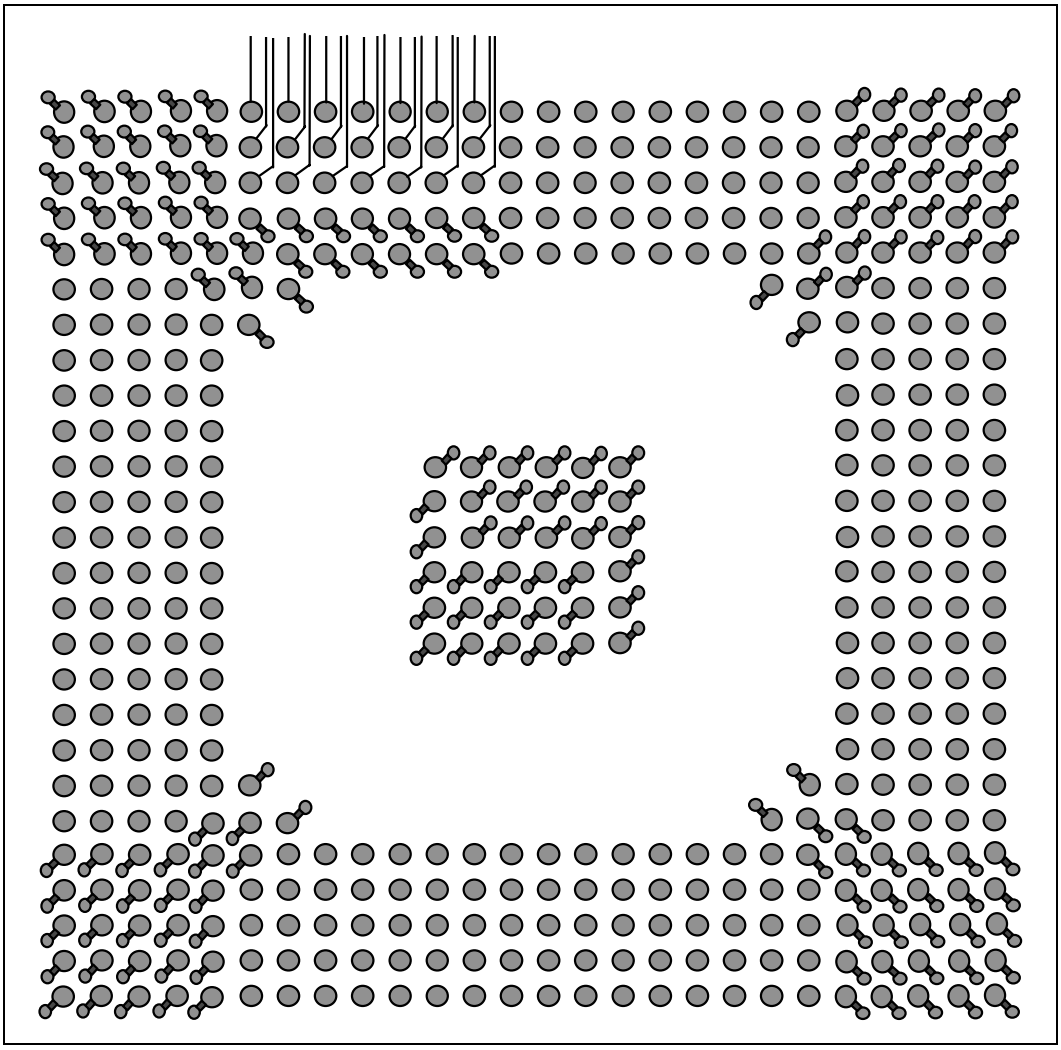
Figure 2-7. BGA Trace



2.2.3.2 Ground Connections

All lands in the four corners and center are V_{ss} (GND). Thermal analysis requires that each V_{ss} ball connect to an adjacent via which passes through to the solder side of the board, one via per ball, with a trace as wide as the via. Heat will dissipate through these vias to the GND plane as well as to the air on the solder side.

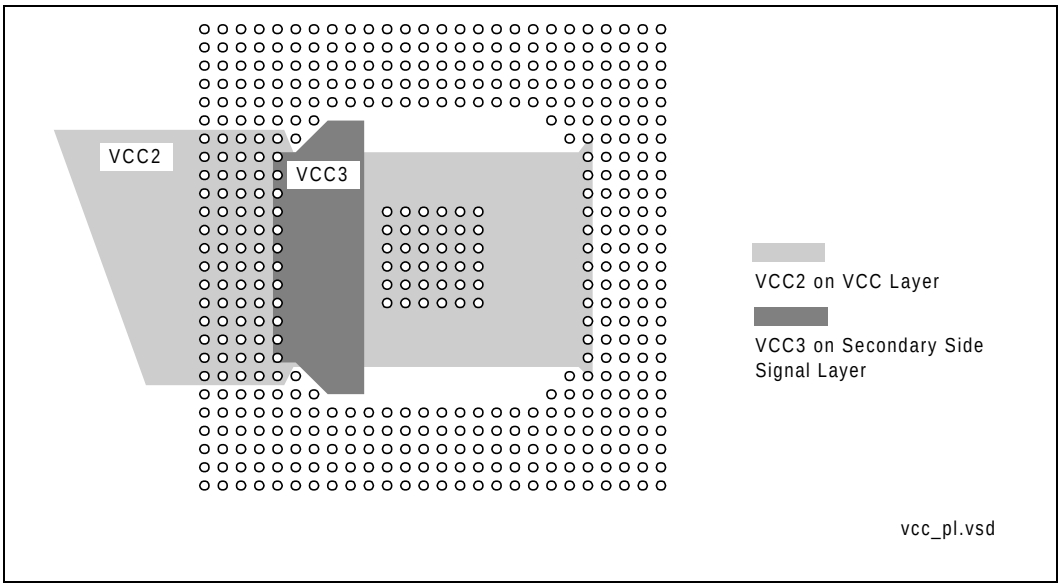
Figure 2-8. Dogbone Via Pattern



2.2.3.3 Power Connections

The VCC2 plane should be as wide as practical for high current-carrying capacity. Because of the interspersing of VCC2 and VCC3 pins on the Intel740™ graphics accelerator, a polygon will be needed on one of the signal layers to extend the VCC3 plane to the isolated VCC3 pins (Figure 2-9). The VCC2 polygon is a separate plane on the VCC Layer; the darker VCC3 polygon is a power flood on the solder side and connects to the VCC3 plane on the VCC Layer through vias.

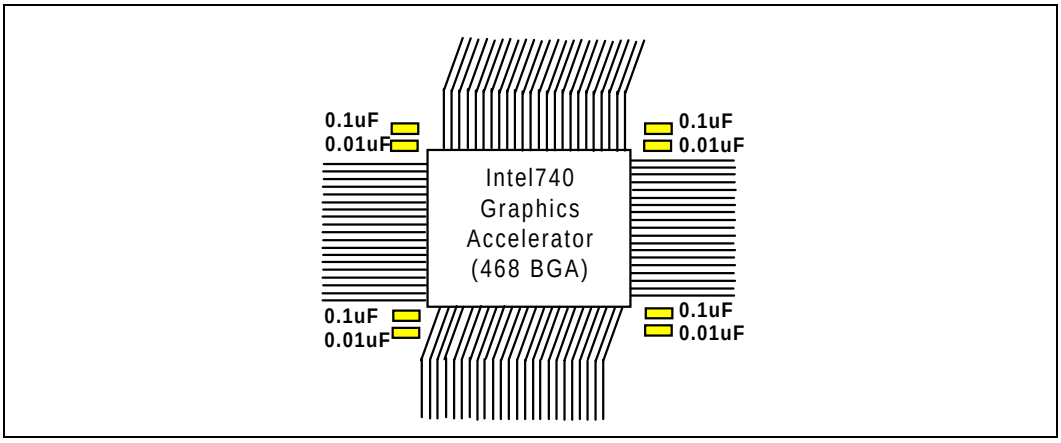
Figure 2-9. Suggested VCC Planes for the Intel740™ Graphics Accelerator



2.2.3.4 Decoupling

Decoupling capacitors should ideally be placed as close as possible to the Intel740 graphics accelerator. This means that the best decoupling will occur if the capacitors are placed directly underneath the component. If a single sided board is required and capacitors cannot be placed underneath the component then decoupling is recommended at the corners of the Intel740 graphics accelerator package. At least a 0.1 µF and 0.01 µF are recommended for each corner. By placing the capacitors in this location all of the traces can “break-out” from the BGA package on all four sides.

Figure 2-10. Intel740™ Graphics Accelerator Decoupling

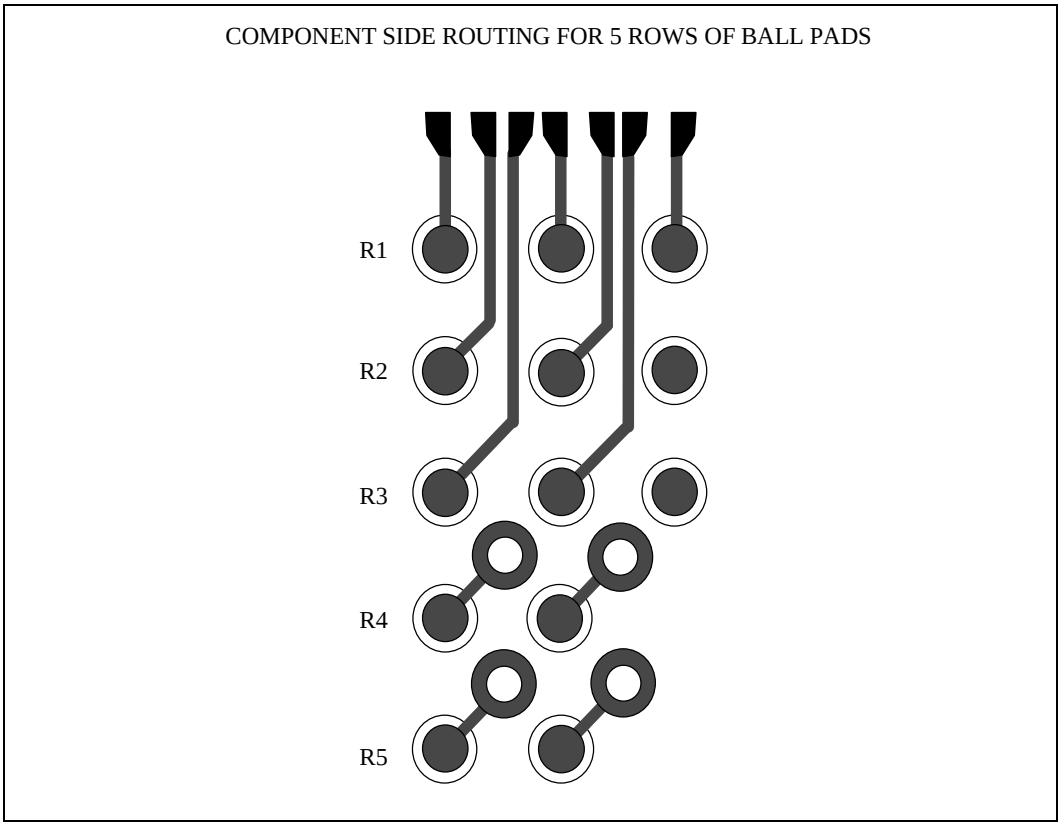


2.2.3.5 General Signal Routing

Figure 2-11 depicts general escape of traces from the five rows of BGA ball pads. The first three ball rows can be routed on the primary layer. The last two must be routed through vias to the secondary layer. Underneath the BGA, trace routing should be 5 on 5 or 6 on 6. Once the traces have left the BGA, however, routing should expand to 5 on 10 or 6 on 12. The ratio should be kept as 1:2.

The signals AD_STB_A, AD_STB_B and SB_STB should have a spacing of 1:4 to other signals. Using this extra spacing between these specific signals will help to keep crosstalk to a minimum.

Figure 2-11. Intel740™ Graphics Accelerator BGA Routing Example



2.2.4 Voltage Regulator

The physical tab (used as a built in heatsink) on the MOSFET package is the drain pin, and will need a tab-shaped pad to solder to.

Note: The resistor/capacitor network between the COMP pin (pin 5) and the GND pin (pin 3) of the LT1575 should be connected directly to the GND pin of the device rather than tied to the ground plane.

2.2.5 Bt829 Video Decoder

Note: Rockwell* Semiconductor should be contacted for up to date layout recommendations.

2.2.5.1 Ground Planes

The Bt829B and associated circuitry have two ground planes, GND and ANALOG_GND (AGND). These are electrically the same plane but should be separated by a fence, as described in Section 2.1.3.2, “Fences” on page 2-4. The schematic illustrates which pins attach to which plane as does Table 2-3. The opening in the fence should be under the Bt829B and be up to 75% of the IC’s width. The AGND plane is the isolated or subset plane, hence GND is the return path for current. The AGND plane should be as small as possible.

Table 2-3. Bt829B GND and AGND Pins

Bt829 Ground Pins	
GND	11, 21, 31, 33, 39, 77, 81, 90, 93, 95, 100
AGND	42, 47, 54, 56, 58, 61, 66, 71, 75

2.2.5.2 Power Planes

The Bt829 and associated circuitry have three power planes, VCC3, VCC and AVCC. The latter two are digital and analog +5V, respectively. As above, these are electrically the same plane but separated by a fence. This fence and the AVCC plane should parallel the AGND fence and plane closely, with the opening in about the same location.

Table 2-4. Bt829B VCC and AVCC Pins

Bt829B 5V Pins	
VCC	10, 38, 76, 88, 96
AVCC	40, 44, 48, 60, 65, 72

2.2.5.3 Passive Components and Signal Routing

All passive components should be placed as near to the Bt829B as possible. These parts include: the 0.1µF and 0.01µF bypass capacitors, the 10µF capacitors, the 75 ohm terminating resistors, and the crystal oscillator circuitry.

Note: There must be NO digital signals routed under or above the analog power and ground planes (AVCC and AGND).

The filter circuits on the four video input signals (TUNER, SV_LUM, SV_CHR, CV_IN) need to be located near the 50-pin connector. Note that other designs not using a 50 pin video connector should have the filter circuits placed as close as possible to the input connectors. The analog traces should not be routed such that they parallel other analog signals at a close spacing for a long length. Wherever analog signals run in parallel, separated by less than 15 mils for longer than 250 mils, run a ground line between them of approximately 12 mils width.

2.2.6 Bt869 Video Encoder

Note: Rockwell Semiconductor should be contacted for up to date layout recommendations.

2.2.6.1 Ground Planes

Only one ground plane is recommended for the Bt869. This ground plane should be formed as a fence underneath the Bt869.

2.2.6.2 Power Planes

The Bt869 and associated circuitry have two power planes, VCC3 and 3VAA_BT869. The 3VAA_BT869 plane is a separate cutout, joined to VCC3 by a ferrite bead. The device should reside entirely above the 3VAA_BT869 plane, as there are no VCC3 connections to the device. So long as the 3VAA_BT869 plane underlies all the analog components, it should be as small as possible.

Table 2-5. Bt869 Digital and Analog Power Pins

Bt869 3V Pins	
3VAA_BT869 (Analog)	69, 71, 73, 80
3VAA_BT869 (Digital)	19, 20, 30, 40, 46, 47, 57, 60, 61

2.2.6.3 Passive Components and Signal Routing

All passive components should be placed as close to the Bt869 device as possible. These devices consist of: the 0.1µF and 0.01µF bypass capacitors, the 10µF capacitors, the crystal oscillator circuitry, and the 0.1µF capacitors and 75 ohm resistors at the VREF, VBIAS and FSADJUST pins as well as the protection diodes.

Note: There must be NO digital signals routed under or above the analog power and ground planes (3VAA_BT869 and AGND).

The filter circuits on the three video output signals (TVOUT_Y, TVOUT_C, TVOUT_CVBS) must be very near the 50-pin connector or other output connectors. Long lengths of closely spaced parallel analog signals should be avoided. Wherever analog signals run in parallel, separated by less than 15 mils for longer than 250 mils, run a ground line between the video input traces of approximately 12 mils width.

2.2.6.4 AGP Layout and Routing Guidelines

This section describes the group of signals that runs between the Intel740 graphics accelerator AGP Interface and the AGP edge connector. For the definition of AGP functionality (protocols, rules and signaling mechanisms, as well as the platform level aspects of AGP functionality), refer to the latest *AGP Interface Specification*. This document focuses only on specific Intel740 graphics accelerator recommendations for the AGP interface. The general length requirements are shown in Table 2-6.

Table 2-6. AGP Signal Lengths

Group	Recommendation
All	≤ 3.0”
CLK	2.6” ± 0.4”

Mismatch between strobe and data traces must be less than 0.5”. Thus the trace length for signals within a group must be within ±0.5” of the corresponding strobe’s trace length, as indicated in Table 2-7.

Table 2-7. Strobes and Corresponding Signal Groups

Group	Strobe	Recommendation
AD[31:16], C/BE[3:2]#	AD_STB_B	$L_{AD\_STB\_B}$ ± 0.5”
AD[15:0], C/BE[1:0]#	AD_STB_A	$L_{AD\_STB\_A}$ ± 0.5”
SBA[7:0]	SB_STB	L_{SB_STB} ± 0.5”

For example, AD29 and AD_STB_B must not be mismatched by more than 0.5”. No such comparison, however, should be enforced between AD29 and AD30, or AD29 and C/BE2#, etc.

Note: AGP strobes must be separated by 2X normal signal spacing (i.e., if normal spacing is 5/10 or 6/12, the strobe signals must be separated from other traces by 20 or 24 mils, respectively).

2.2.6.5 Intel740™ Graphics Accelerator Memory Layout and Routing Guidelines

The Intel740 graphics accelerator integrates a memory controller which supports a 64-bit memory data interface. SGRAM can be used in addition to SDRAM if it is configured to perform as an SDRAM. The Intel740 graphics accelerator generates the Row Address Strobe (SRAS[A:B]#), Chip Selects (CS0[A:B]#, CS1[A:B]#), Column Address Strobe (SCAS[A:B]#), Byte Enables (DQM[0:7]#), Write Enables (WE[A:B]#), and Memory Addresses (MA). The memory controller interface is fully configurable through a set of control registers.

Eleven memory address signals (MAx[10:0]) allow the Intel740™ graphics accelerator to support a variety of commercially available SO-DIMMs and components. Two SRAS# lines permit two 64-bit wide rows of SDRAM. All write operations must be one Quadword (QWord). The Intel740 graphics accelerator supports memory up to 100 MHz.

Rules for populating a Intel740 graphics accelerator Memory:

- Memory can be populated using either an SO-DIMM or components.
- SDRAM and SGRAM components and/or SO-DIMMs can be mixed.
- The DRAM Timing register, which provides the DRAM speed grade control for the entire memory array, must be programmed to use the timings of the slowest memories installed.

Possible DRAM and system options supported by the Intel740 graphics accelerator are shown in Table 2-8.

Table 2-8. Supported Memory Options (Other Memory Options Are Not Supported)

SDRAM/ SGRAM Technology	SDRAM/ SGRAM Density	SDRAM/ SGRAM Width	Addressing	Address Size		Local Memory Size	
				Row	Column	Min	Max
8 Mbit	256K	32	Asymmetric	10	8	2MB	4MB
16Mbit	512K	32	Asymmetric	11	8	4MB	8MB
16Mbit	1M	16	Asymmetric	12	8	8MB	8MB

There are several groups of signals within the memory bus with layout restrictions.

Table 2-9. Memory Layout Restrictions (See Figure 2-12 and Figure 2-13)

Signal	Intel740™ to SO-DIMM		SO-DIMM SGRAM Stub		SGRAM Stub	
	Min	Max	Min	Max	Min	Max
MA[11:0]	n/a	4.0”	0.25”	0.9”	0.25"	0.6”
MD[63:0], DQM[7:0]	n/a	3.0”	0.25”	0.9”	0.25"	0.4”

Figure 2-12. Layout Dimensions (MA[11:0])

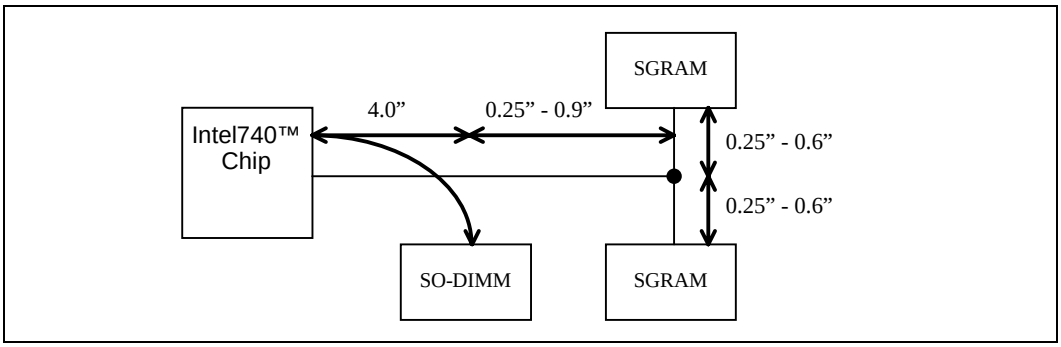


Figure 2-13. Layout Dimensions (MD[63:0], DQM[7:0])

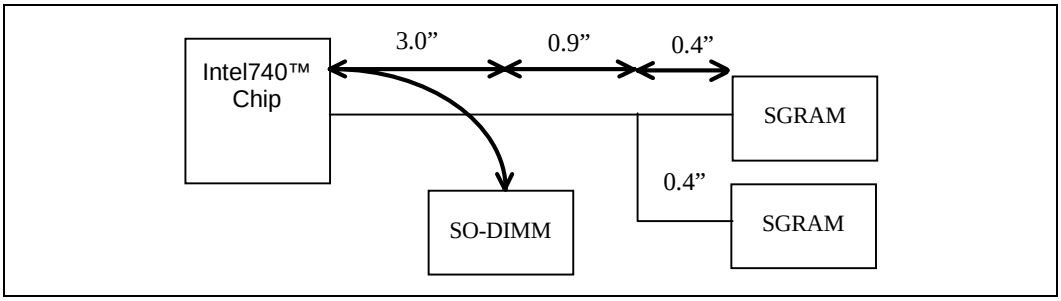


Table 2-10. Memory Layout Restrictions (See Figure 2-14 and Figure 2-15)

Signal	Intel740™ to SO-DIMM		SO-DIMM to SGRAM Stub		SGRAM Stub	
	Min	Max	Min	Max	Min	Max
WEA#, SRASA#, SCASA#, CSA1#, CSB0#	n/a	4.0”	n/a		n/a	
WEB#, SRASB#, SCASB#, CSA0#	n/a	4.0”	0.25”	0.9”	0.25”	0.6”

Figure 2-14. Layout Dimensions (WEA#, SRASA#, SCASA#, CSA1#, CSB0#)

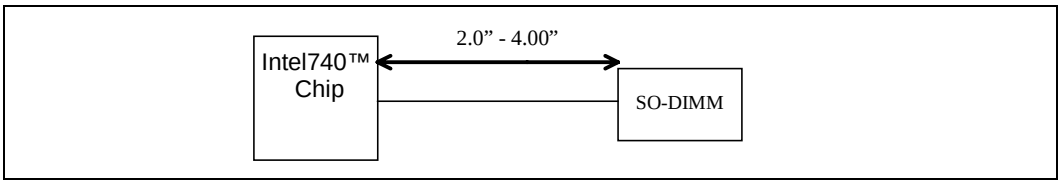


Figure 2-15. Layout Dimensions (WEB#, SRASB#, SCASB#, CSA0#)

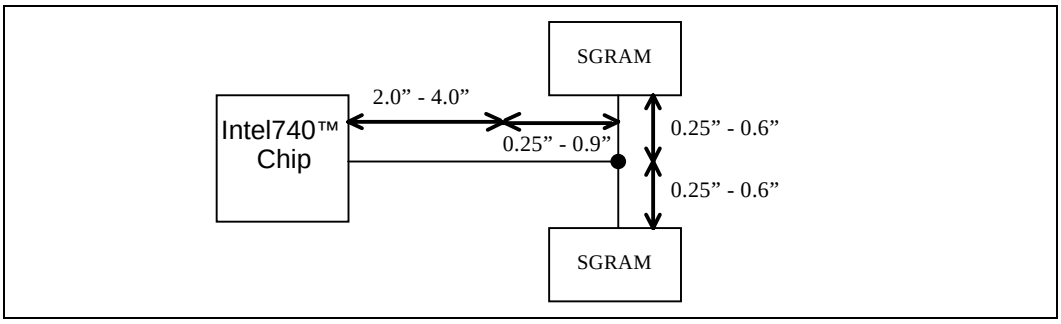


Table 2-11. Memory Layout Restrictions (See Figure 2-16 and Figure 2-17)

Signal	Intel740™ to Resistor	Resistor to SO-DIMM	SO-DIMM to SGRAM Stub	SGRAM Stub	
				Min	Max
TCLK0	0.6”	2.4” ±0.25”	n/a	n/a	n/a
TCLK1	0.6”	2.4” ±0.25”	1.0”	0.4”	0.6”

Figure 2-16. Memory Layout Dimensions (TCLK0)

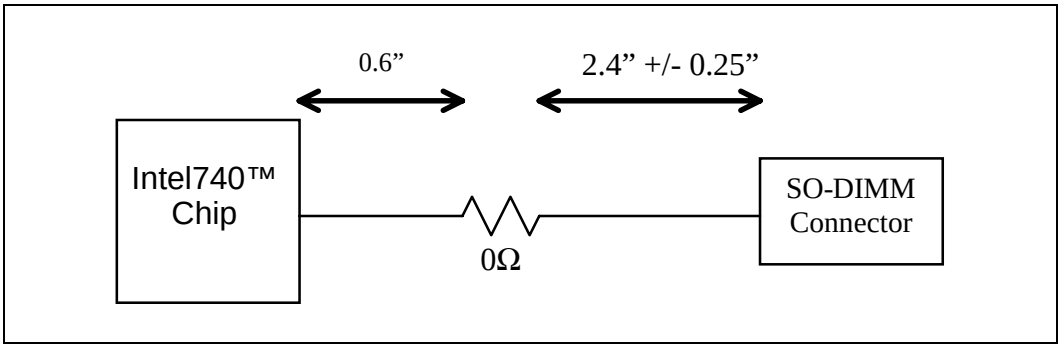
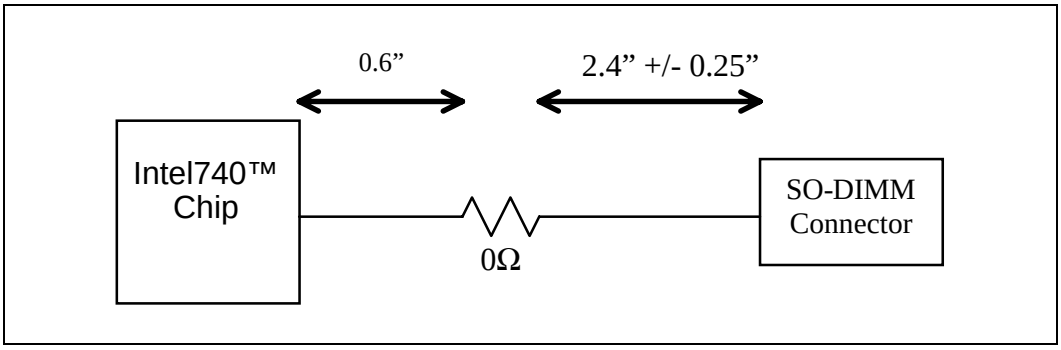


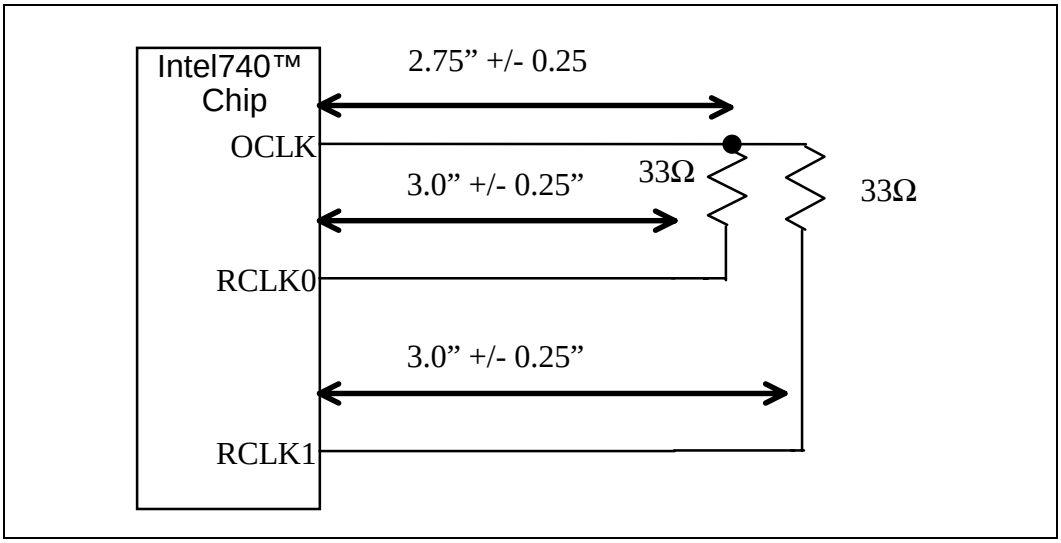
Figure 2-17. Memory Layout Dimensions (TCLK1)



Signal	Intel740™ to Resistor
OCLK to Resistor	2.75” ±0.25
RCLK0, RCLK1	3.0” ±0.25”

Note: It is important to match clock lengths. For example, if the length from OCLK to Resistor is 1.03, then the length from Resistor to RCLK should be 3.03.

Figure 2-18. Memory Layout Dimensions (RCLK and OCLK to RCLK)

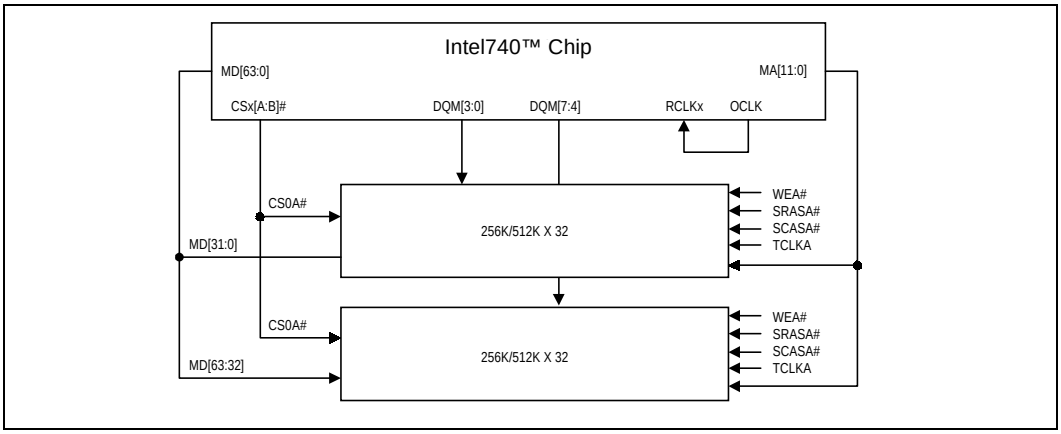


2.2.6.6 Intel740™ Graphics Accelerator Memory Configurations

In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by an SRAS and the CS# signal.

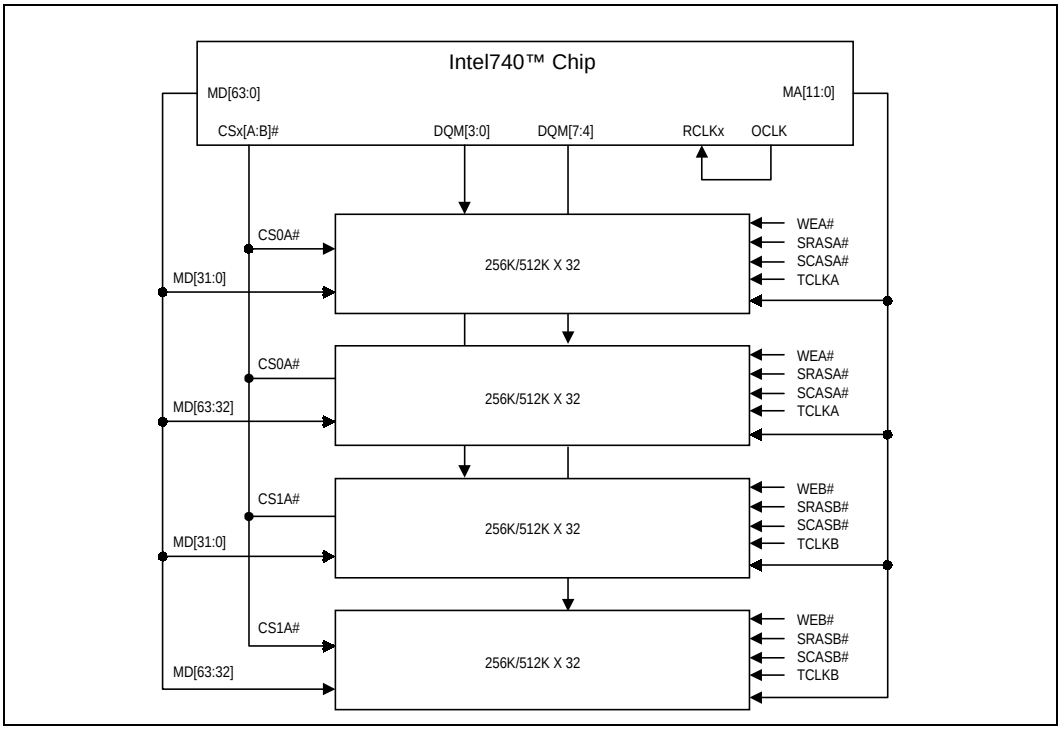
Configuration #1: In this configuration, the minimum amount of memory (2MB) is supported. Note that, the same copy of all control signals goes to each component.

Figure 2-19. 2/4 MB Local Memory Connection (64-bit data path)



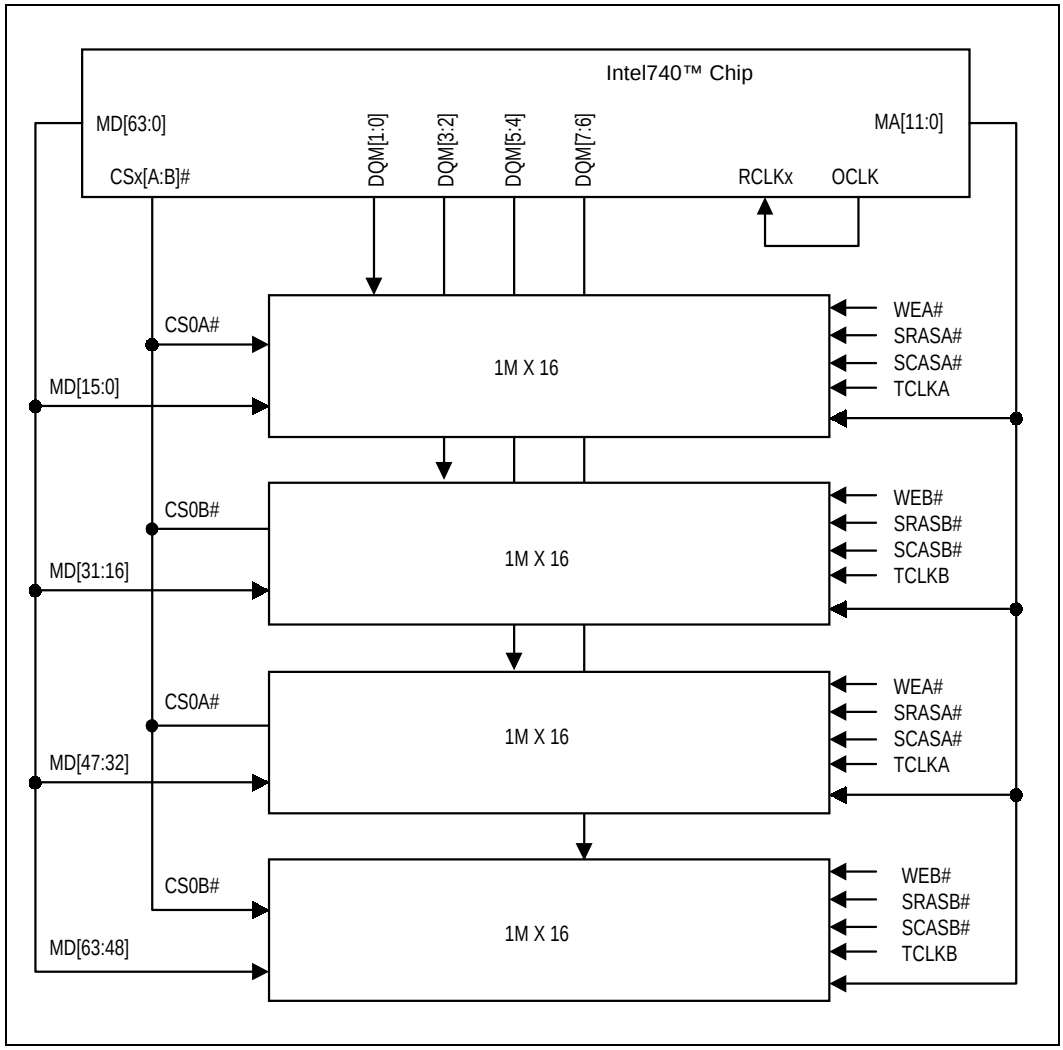
Configuration #2: Two rows of memory are supported in this configuration. If 256Kx32 components are used 4MB of memory is obtainable, if 512Kx32 is used, then 8MB is supported. Note that both rows of memory receive different copies of each control signal, for loading reasons.

Figure 2-20. 4/8 MB Local Memory Connection (64-bit data path)



Configuration #3: One row of memory is supported in this configuration using 1Mx16 SDRAMs. Only the maximum allowable amount of memory (8MB) is supported in this configuration. Note that each copied signal is sent to only two components.

Figure 2-21. 8 MB Local Memory Connection (64-bit data path)



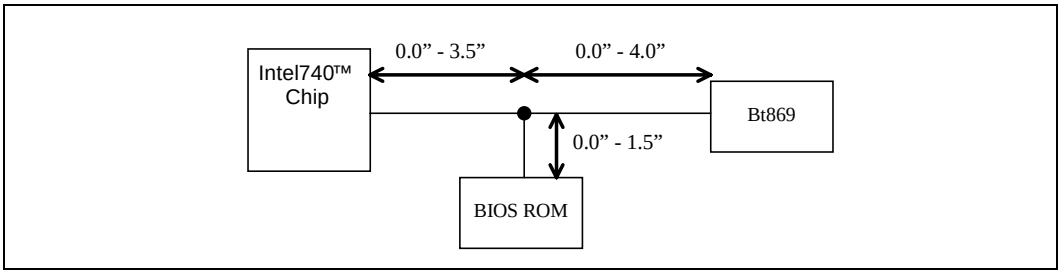
2.2.6.7 TV Out Interface

The TV out bus is the group of signals that carry digitized display data from the Intel740 graphics accelerator to the Bt869 flicker filter TV-out component. This interface is shared with the BIOS interface. Table 2-12 gives the maximum trace lengths between components.

Table 2-12. TV Out/ROMA Trace Lengths (See Figure 2-22)

Signal	Intel740™ to BIOS Stub		BIOS Stub		BIOS to Bt869	
	Min	Max	Min	Max	Min	Max
ROMA[17:0]	0.0”	3.5”	0.0”	1.5”	0.0”	4.0”

Figure 2-22. Layout Dimensions, Digital TV Bus



2.2.6.8 Analog Signals

It is recommended that all analog signal traces be 75Ω ±5%. It is important that these traces not violate the 5x10 mil spacing for the 65Ω traces. Analog traces include the DAC R, G, B traces, all of the inputs to the Bt829B component and outputs from the Bt869 component.

2.2.7 UL and FCC Considerations

Certain precautions should be taken in the design of the of a graphics card to ensure passing safety and EMI tests. These precautions are listed below.

- When a signal can be hot plugged, clamping diodes should be used to limit voltage spikes.
- When a voltage leaves the card, a fuse should be placed in the path to protect from a short circuit.
- Sockets, Fans and Brackets should be grounded.
- Separate Power Planes of the same voltage should be stitched together.

2.3 Addin Card Schematics

This section describes the Intel740™ Graphics Accelerator Reference Design Schematics. Please read this section carefully to observe all design recommendations and requirements.

The description of each schematic page is named by the logic block shown on that page.

Cover Sheet (Schematic Page 1)

The Cover Sheet shows the schematic page titles, page numbers, disclaimers and power pins.

Block Diagram (Schematic Page 2)

This page shows a block diagram overview of the Intel740 AGP card design. Schematic page numbers for each of the major schematic components are shown.

Intel740™ Graphics Accelerator (Schematic Pages 3,4)

This page shows all of the connections to the Intel740 graphics accelerator. Each Intel740 graphics accelerator interface is hooked up in this reference design. Beginning in the upper left hand corner of the page, the video capture port is shown. Internally, the input pins are pulled down. These pins contain a strapping option for subsystem ID. In this case the reference design has an ID of 0100h. Bits that should be a “1” may be pulled up using a 2K pull-up resistor. If the graphics design will not have video, the only concern is pulling the bus up to the correct value for the subsystem ID. The video control signals may be left unconnected. The BIOS interface multiplexes the BIOS, vendor ID, and flicker filter TV encoder. The ROMA lines are internally pulled down and may be pulled up using a 2K pull-up resistor. The video host port connects directly to the VMI header. The section labeled AGP interface connects directly to the AGP connector. The memory interfaces connect to an SO-DIMM connector and memory components. Each of the 9 GPIOs serve a different function in the reference design. Table 2-13 lists the function assigned to the GPIOs.

Table 2-13. GPIO Functions

GPIO	FUNCTION
GPIO0	I^2C Data
GPIO1	I^2C Clock
GPIO2	DDC Data
GPIO3	DDC Clock
GPIO4	Fan Fail
GPIO5	Extra For DVD Control
GPIO6	VP[15:0] Bus Isolation Control
GPIO7	Extra For DVD Control
GPIO8	Power Down

Decoupling for the Intel740 graphics accelerator is shown along the bottom of the schematic page.

Voltage Regulator (Schematic Page 5)

This page shows the circuitry to convert from 3.3 Volts to 2.7 Volts. The regulator used in the reference design does not need any heat sink for the FET. As shown, the FET will be dissipating slightly over 1 watt. If a different voltage regulator solution will be used, calculations will be needed to determine the need for a heatsink. Resistors R50, R44, R42, and R43 are only for the reference card design. These resistors allow different voltage combinations for core and internal Intel740 graphics accelerator PLLs. The table at the top of the page describes the voltage configurations. Core decoupling is shown at the bottom of the page and should be placed close to the Intel740 graphics accelerator.

Bt829B (Schematic Page 6)

The Bt829B component contains analog inputs which require special routing requirements detailed in Section 2.2.5, “Bt829 Video Decoder” on page 2-11. If these analog inputs are not used, then they should be tied to ground as is MUX3 in the reference design. The I2CCS pin is pulled low in the reference design to select an I^2C address of 88h and 89h. This selection becomes important if connecting other I^2C devices like the Bt869.

Note: Care must be taken to ensure that no two devices use the same address.

The QCLK output of the Bt829B obviates the need for connection to the VRDY input on the Intel740 graphics accelerator as this clock “ANDs” the ACTIVE and CLK outputs of the Bt829B together. The reference design is designed to support NTSC, PAL and SECAM. If only NTSC is desired, the circuitry including Y1 can be removed and XT1I should be tied high or low with XT1O left floating. If only PAL mode of operation is desired, XT1I should be tied high or low with XT1O floating and Y2 should be replaced with Y1. Decoupling for the component is shown at the bottom of the page.

Bt869 (Schematic Page 7)

The Bt869 power supply is generated from the VCC3 supply. Decoupling for this supply is shown at the top of the page. The component contains a 24-bit data port. The Intel740 graphics accelerator connects only to 12 of these bits. The functionality of this interface is described in the Intel740 Graphics Accelerator Datasheet. The slave input is tied to ground to place this chip in master mode. If the digital port were to be used as a VMI port, the component should be placed in slave mode. This page contains the only jumper in the design. This jumper selects which mode (PAL or NTSC) the Bt869 will operate in. The *PC ’98* specification recommends this jumper for designs where a TV may be the only output display. The ALTADDR pin is pulled high so that the device responds to an address of 8Ah. This address keeps this device from conflicting with the Bt829B’s I^2C address. Note that ROMA17 is wired to the CLKI pin while ROMA14 is connected to the CLKO pin. ROMA17 is also called CLKOUT and ROMA14 is called CLKIN. The Intel740’s graphics accelerator CLKOUT pin corresponds to the Bt869’s CLKI pin while the CLKIN pin corresponds to the CLKO pin on the Bt869. The DAC lines have special routing requirements detailed in section. These DAC lines allow the component to output S-Video and composite video.

VMI Video Connectors (Schematic Page 8)

The VMI video connectors are used for the attachment of a DVD daughter card or video capture card. The capture port is connected to the 26 pin header while the bi-directional host port is connected to the 40 pin header. The reference design uses a 2A fuse for the 3.3 volt supply to the 40 pin header. The 2A fuse is allowed for the 5 volt supply and 1A is allowed for the 12 volt supply. GPIO5 and GPIO7 come to the header for added DVD daughter card functionality control. GPIO8 is used for power down operation on the card. The I^2C connections on the 26 pin header are 3.3 volt signals. Mechanical dimensions for the placement of the connectors is shown in Section 5.3, “VMI Header Placement” on page 5-2.

AGP Card Edge (Schematic Page 9)

This page details the connections of AGP. All power is derived from this connector. Using the rule of 1A per pin, the 12 volt supply is capable of supplying 1A, the 5 Volt supply is capable of supplying 2A and the 3.3 Volt supply is capable of supplying 8A.

VGA Connector (Schematic Page 10)

The VGA connector provides the RGB output to a monitor. BIOS and hardware provide support for plug-and-play capability.

DDC/I^{2}C (Schematic Page 11)

This page details the 3.3 volt/5 volt signal conversion as well as the DDC/I^{2}C connections. To perform the voltage translation, quick switches are used. The quick switches at the top of the page serve a second function of isolating the VMI port from the Intel740 graphics accelerator. GPIO6 can tri-state this bus to preclude the possibility of contention between something connected to the VMI header and the Bt829B.

SO-DIMM Connector (Schematic Page 12)

The SO-DIMM connector shows a fairly straight forward connection to the Intel740 graphics accelerator memory signals. Note that the primary CS0 connection is tied to the Intel740 graphics accelerator CSA1# signal. The CSB0# signal is connected to CS1 on the connector. The reference design has the first row of memory down on the graphics card. The second row of memory is assumed to be placed in the SO-DIMM connector.

Note: It is important not to have the memory on the graphics card and memory on the SO-DIMM connector connected to the same row.

SGRAMS (Schematic Page 13)

The SGRAMs shown on this page are labeled as 512Kx32. The schematic pinout is actually capable of supporting either the 512Kx32 or 256Kx32 SGRAMs. This dual-support connection is achieved through the following method. The 512Kx32 Jedec standard defines AP on pin 51 which is address 9. BS is on pin 29 and is also labeled as address 10. Address 8 is on pin 30. The Intel740 contains the AP on its address 8 pin and BS on address 9 pin. Since the 256Kx32 has AP with graphics accelerator address 8 and on pin 51 along with BS with address 9 on pin 29 and a no connect on pin 30, either the 512K or the 256K SGRAMs are capable of being supported in the same design (see Figure 2-23).

Note: It is important to disable the special features of SGRAM. This will make the SGRAM operate as an SDRAM, thus making it compatible with the Intel740 graphics accelerator.

Figure 2-23. 512Kx32 and 256Kx32 Pinout Compatibility

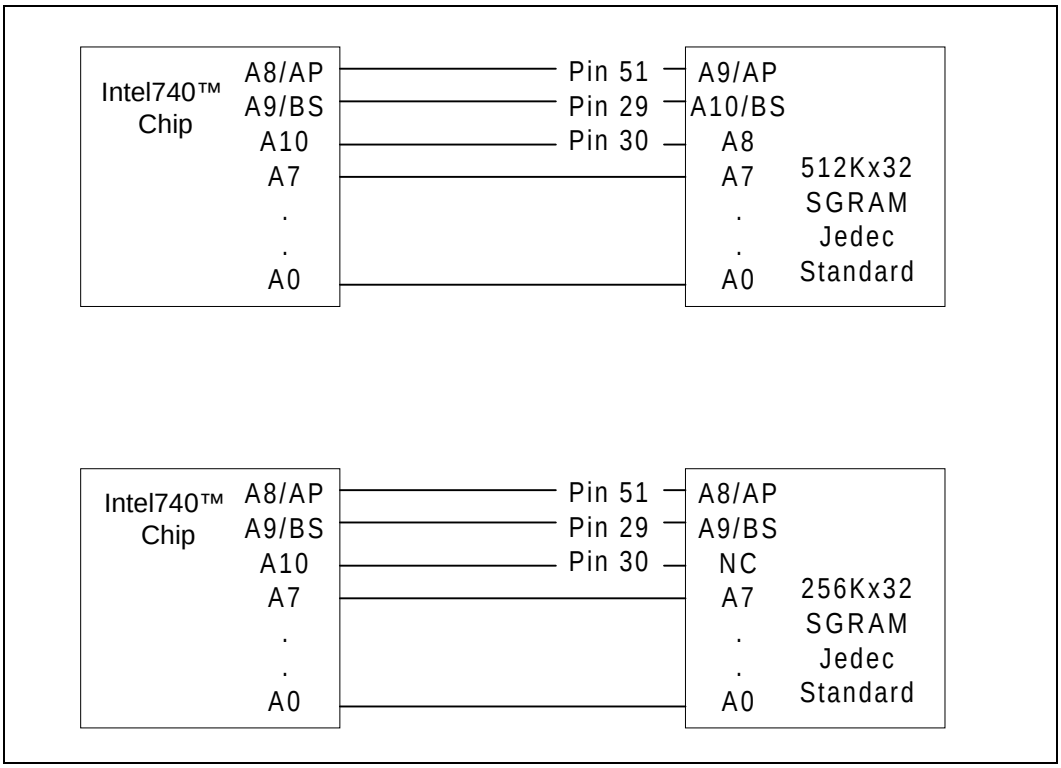
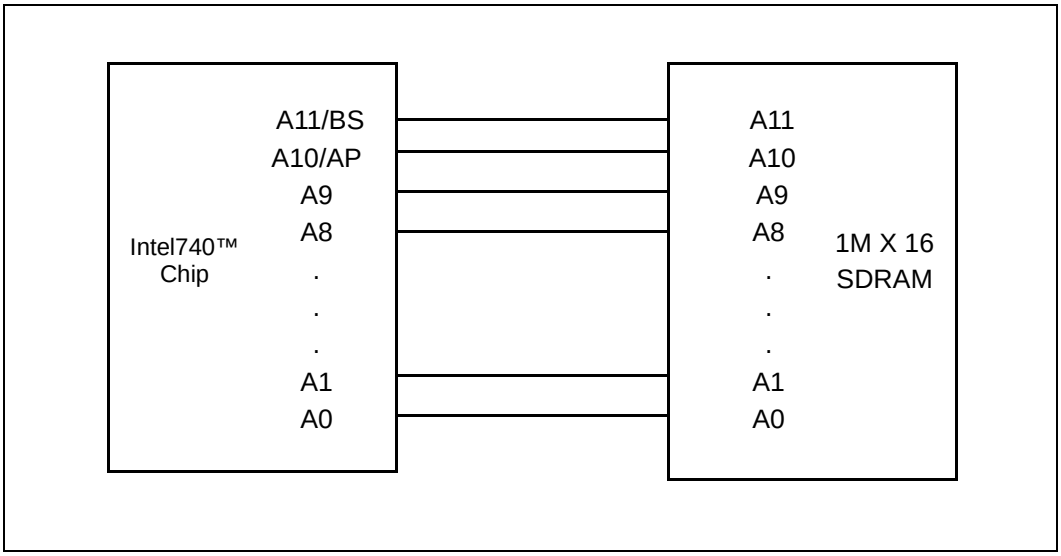


Figure 2-24. 1M X 16 Pinout Compatibility



Video Connector (Schematic Page 14)

This page shows a specially designed solution to the problem of too many connectors and not enough board space. This 50 pin connector allows external hookup for a tuner, S-Video in, S-Video Out, composite video in, and composite video out. The input connections feed to the Bt829B component while the out connections come from the Bt869. Individual designs may or may not have all possible connectors and, therefore, may not need this type of solution.

BIOS/FAN (Schematic Page 15)

This page shows the connections to the flash BIOS and fan power. The BIOS used in this design is a PLCC socket for early debug capabilities. To use less board space a TSOP package may be the preferred component. Since the selected part is a 5 volt part, the data lines are isolated from the Intel740 graphics accelerator by a level shifter.

Note: The Intel740 graphics accelerator does not require a fan for AGP compliant systems. These design features have been added for ease of use if the customer determines a fan is required. Refer to the Thermal Application Note and software to determine the correct thermal solution.

The fan powerdown control is done through the use of a FET. Normal operation of the fan is allowed by the 4.7 KΩ pull-up resistor (R26). If powerdown is desired, the GPIO8 pin will turn the FET off. Pin 3 of the fan header allows the fan to signal the Intel740 graphics accelerator that it has failed.

INTEL740(TM) GRAPHICS ACCELERATOR FULL FEATURED REFERENCE CARD

+12V = 12V ANALOG UNLESS OTHERWISE SPECIFIED

VCC = 5V DIGITAL UNLESS OTHERWISE SPECIFIED

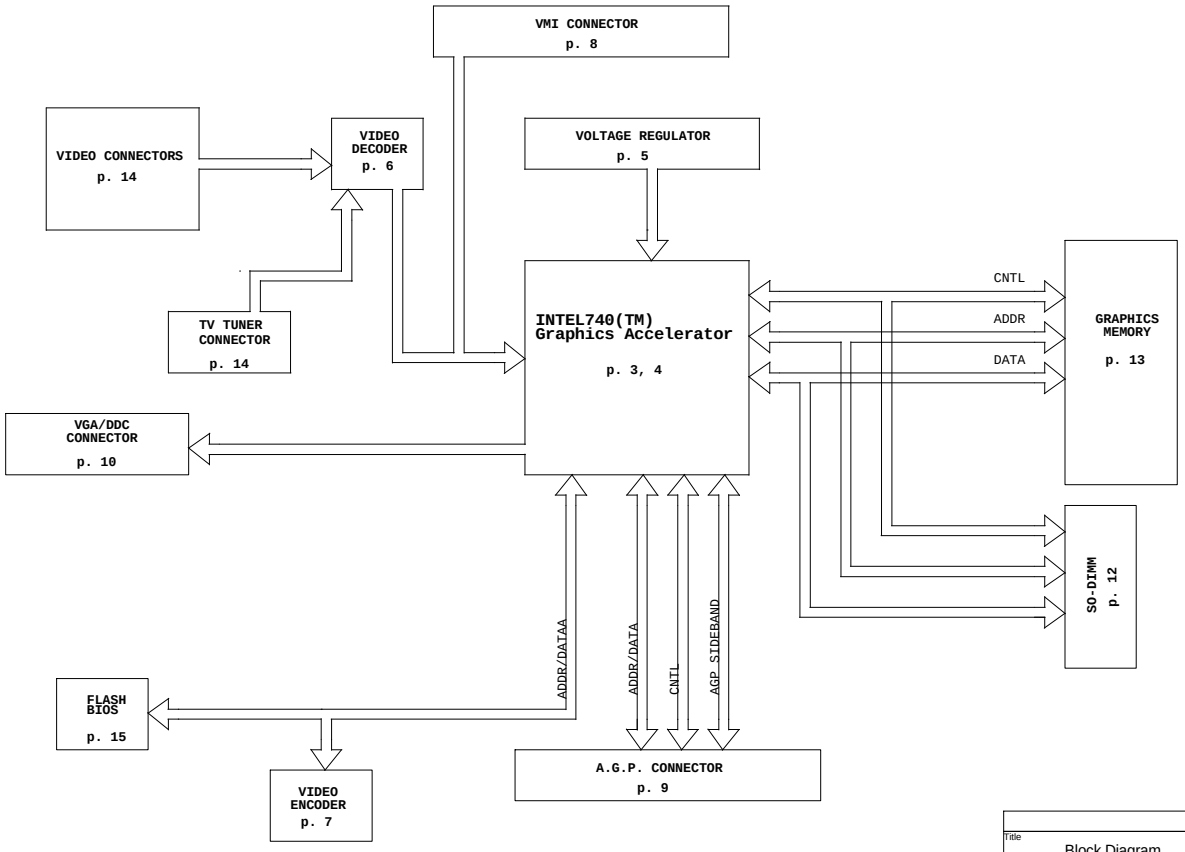
VCC3 = 3.3V DIGITAL UNLESS OTHERWISE SPECIFIED

VDDQ = 3.3V AGP POWER SUPPLY

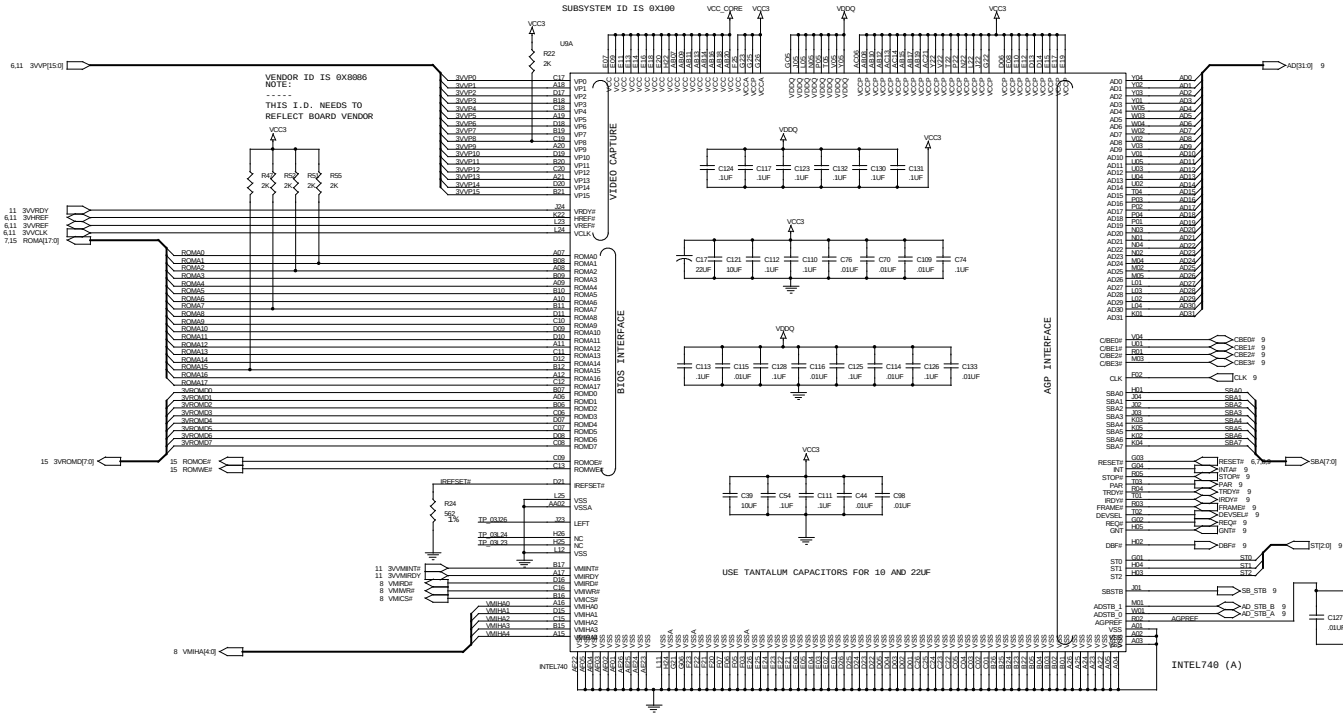
VCC_CORE = VOLTAGE SUPPLIED TO THE INTEL740 CHIP CORE

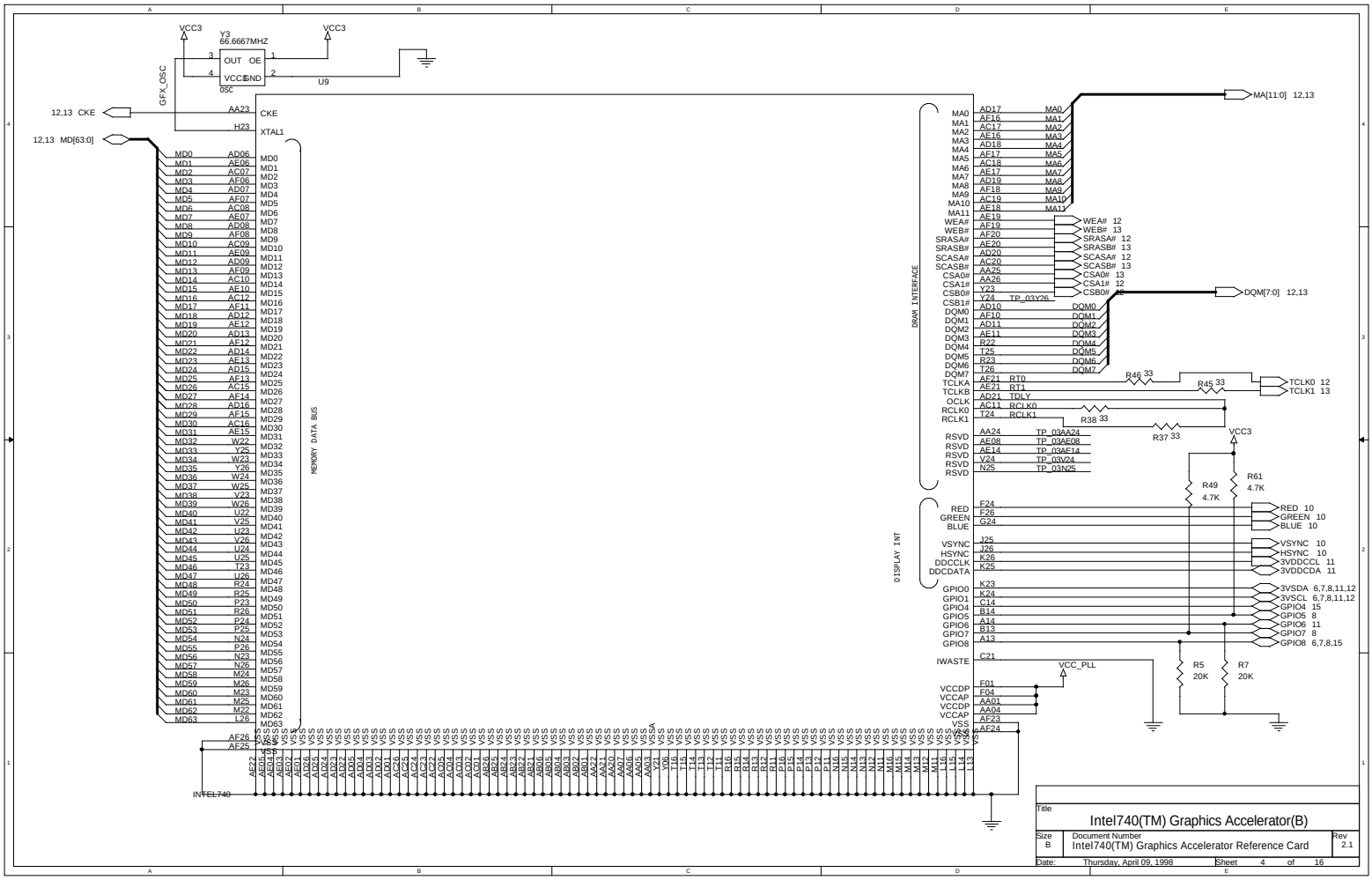
GND = DIGITAL GND

Title: Cover Sheet		
Size: C	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
Date: Thursday, April 09, 1998	Sheet 1 of 16	



Title	Block Diagram	
Size: B	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
Date: Thursday, April 09, 1998	Sheet 2 of 16	


SUBSYSTEM ID IS 0X100
VENDOR ID IS 0X8086
NOTE:
THIS I.D. NEEDS TO
REFLECT BOARD VENDOR
VIDEO CAPTURE
BIOS INTERFACE
AGP INTERFACE
USE TANTALUM CAPACITORS FOR 10 AND 22UF
INTEL740 (A)
Intel740(TM) Graphics Accelerator(A)
Intel740(TM) Graphics Accelerator Reference Card


Y3
66.6667MHZ
OUT
OE
VCC
GND
OSC
U9
VCC3
GFX_OSC
12,13 CKE
12,13 MD[63:0]
CKE
XTAL1
MEMORY DATA BUS
DRAM INTERFACE
DISPLAY INT
MA[11:0] 12,13
DQM[7:0] 12,13
WEA# 12
WEB# 13
SRASA# 12
SRASB# 13
SCASA# 12
SCASB# 13
CSA0# 13
CSA1# 12
CSB0# 12
TCLK0 12
TCLK1 13
RED 10
GREEN 10
BLUE 10
VSYNC 10
HSYNC 10
3VDDCCL 11
3VDDCDA 11
3VSDA 6,7,8,11,12
3VSCL 6,7,8,11,12
GPIO4 15
GPIO5 8
GPIO6 11
GPIO7 8
GPIO8 6,7,8,15
R46 33
R45 33
R38 33
R37 33
R49 4.7K
R61 4.7K
R5 20K
R7 20K
VCC_PLL
IWASTE
INTEL740
Title
Intel740(TM) Graphics Accelerator(B)
Size B
Document Number
Intel740(TM) Graphics Accelerator Reference Card
Rev 2.1
Date: Thursday, April 09, 1998
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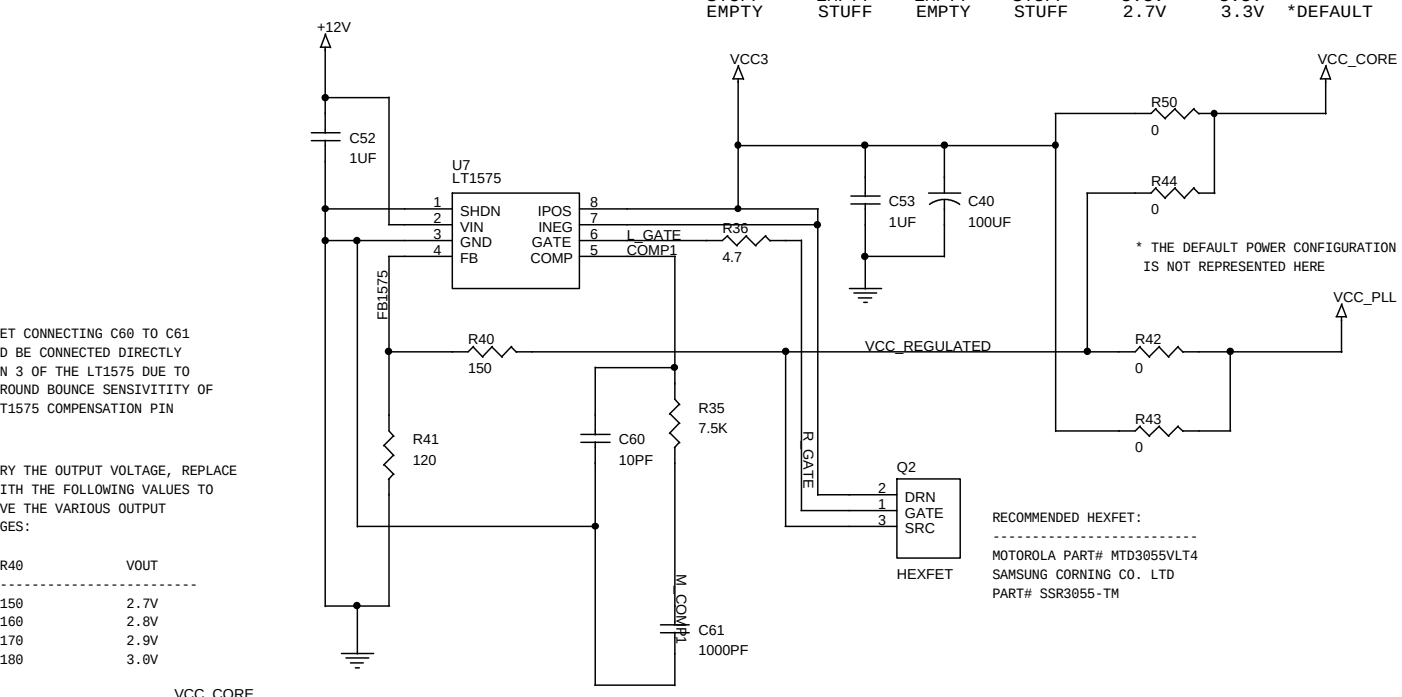
POWER CONFIGURATION*

R50	R44	R42	R43	CORE	PLL	
STUFF	EMPTY	STUFF	EMPTY	3.3V	2.7V	
EMPTY	STUFF	STUFF	EMPTY	2.7V	2.7V	
STUFF	EMPTY	EMPTY	STUFF	3.3V	3.3V	
EMPTY	STUFF	EMPTY	STUFF	2.7V	3.3V	*DEFAULT



NOTE:

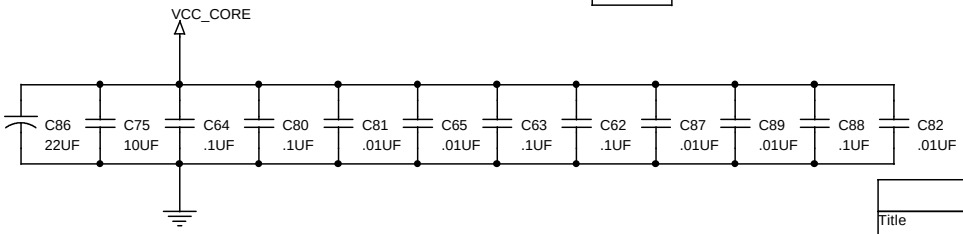
THE NET CONNECTING C60 TO C61
SHOULD BE CONNECTED DIRECTLY
TO PIN 3 OF THE LT1575 DUE TO
THE GROUND BOUNCE SENSIVITITY OF
THE LT1575 COMPENSATION PIN

TO VARY THE OUTPUT VOLTAGE, REPLACE
R40 WITH THE FOLLOWING VALUES TO
ACHIEVE THE VARIOUS OUTPUT
VOLTAGES:

R40	VOUT
150	2.7V
160	2.8V
170	2.9V
180	3.0V

RECOMMENDED HEXFET:

MOTOROLA PART# MTD3055VLT4
SAMSUNG CORNING CO. LTD
PART# SSR3055-TM



Title: Voltage Regulator

Size: A | Document Number: Intel740(TM) Graphics Accelerator Reference Card | Rev: 2.1

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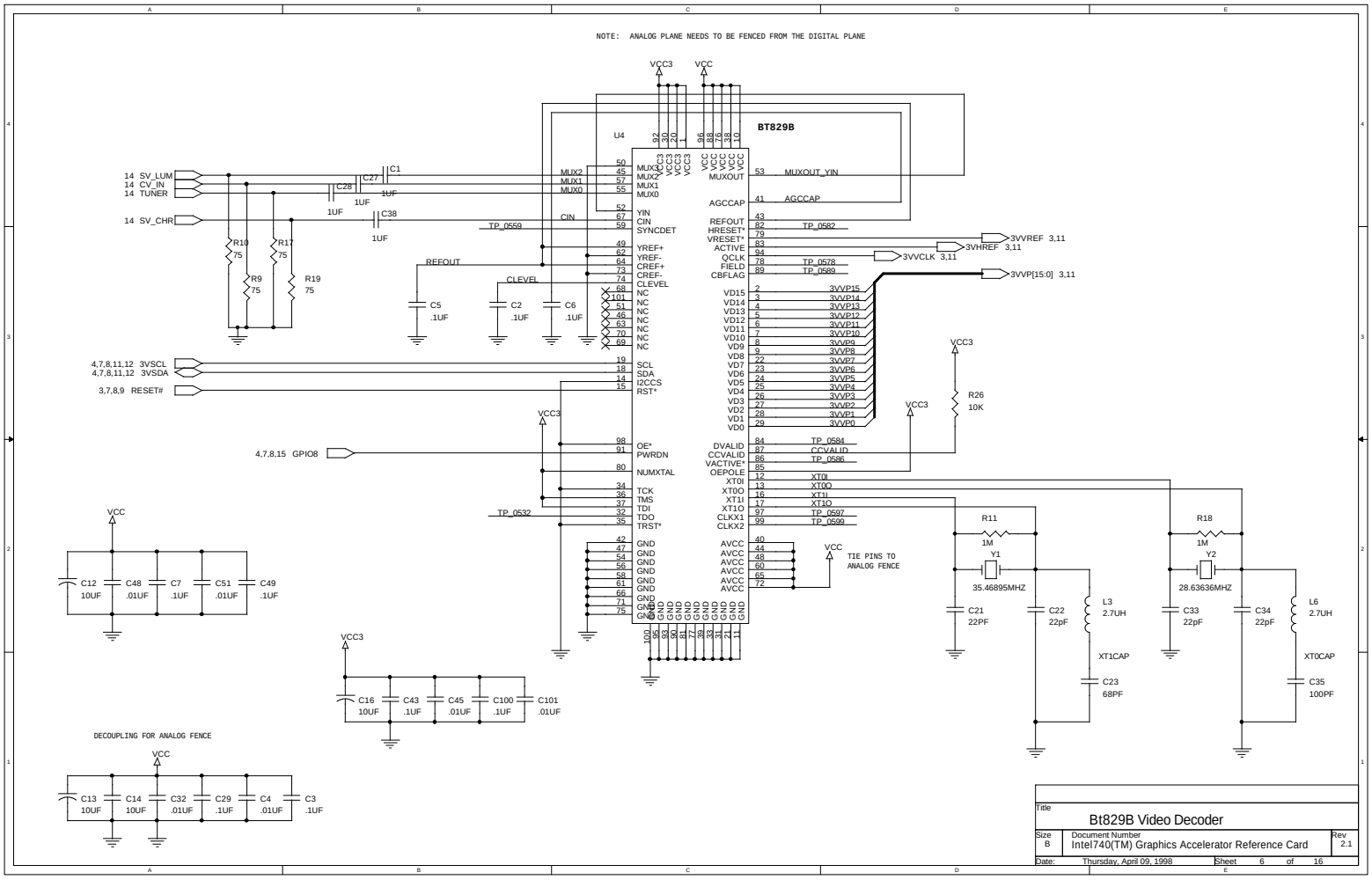

Title	Bt829B Video Decoder	
Size: B	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
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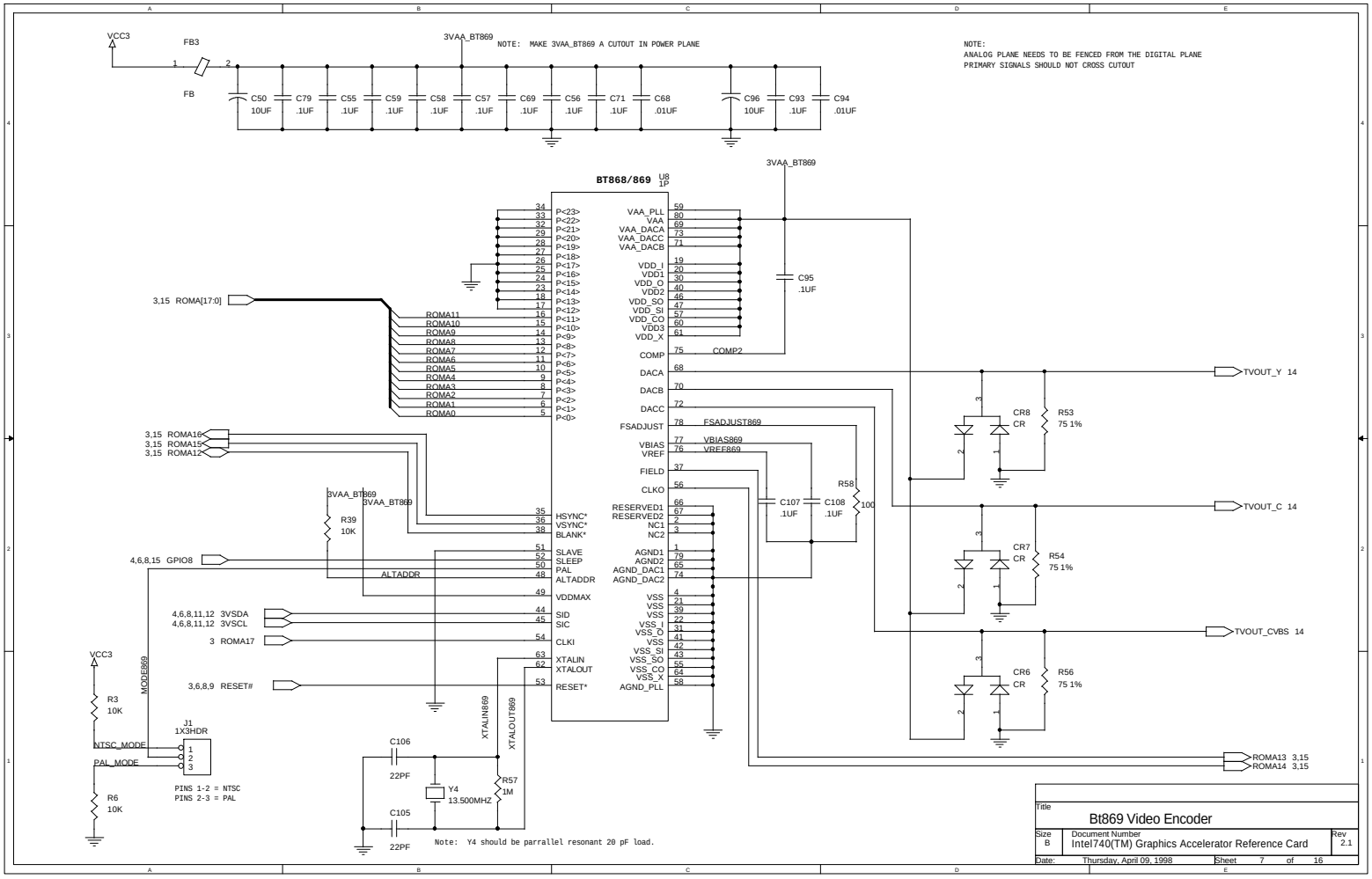
VCC3
FB3
FB
3VAA_BT869
NOTE: MAKE 3VAA_BT869 A CUTOUT IN POWER PLANE
NOTE:
ANALOG PLANE NEEDS TO BE FENCED FROM THE DIGITAL PLANE
PRIMARY SIGNALS SHOULD NOT CROSS CUTOUT
C50 10UF
C79 .1UF
C55 .1UF
C59 .1UF
C58 .1UF
C57 .1UF
C69 .1UF
C56 .1UF
C71 .1UF
C68 .01UF
C96 10UF
C93 .1UF
C94 .01UF
BT868/869 U8 1P
C95 .1UF
3,15 ROMA[17:0]
ROMA11
ROMA10
ROMA9
ROMA8
ROMA7
ROMA6
ROMA5
ROMA4
ROMA3
ROMA2
ROMA1
ROMA0
3,15 ROMA16
3,15 ROMA15
3,15 ROMA12
COMP2
FSADJUST869
VBIAS869
VREF869
C107 .1UF
C108 .1UF
R58
TVOUT_Y 14
TVOUT_C 14
TVOUT_CVBS 14
CR8
CR7
CR6
R53 75 1%
R54 75 1%
R56 75 1%
ROMA13 3,15
ROMA14 3,15
R39 10K
4,6,8,15 GPIO8
ALTADDR
4,6,8,11,12 3VSDA
4,6,8,11,12 3VSCL
3 ROMA17
3,6,8,9 RESET#
MODE869
R3 10K
R6 10K
J1 1X3HDR
NTSC_MODE
PAL_MODE
PINS 1-2 = NTSC
PINS 2-3 = PAL
C106 22PF
C105 22PF
Y4 13.500MHZ
R57 1M
XTALIN869
XTALOUT869
Note: Y4 should be parrallel resonant 20 pF load.
Title
Bt869 Video Encoder
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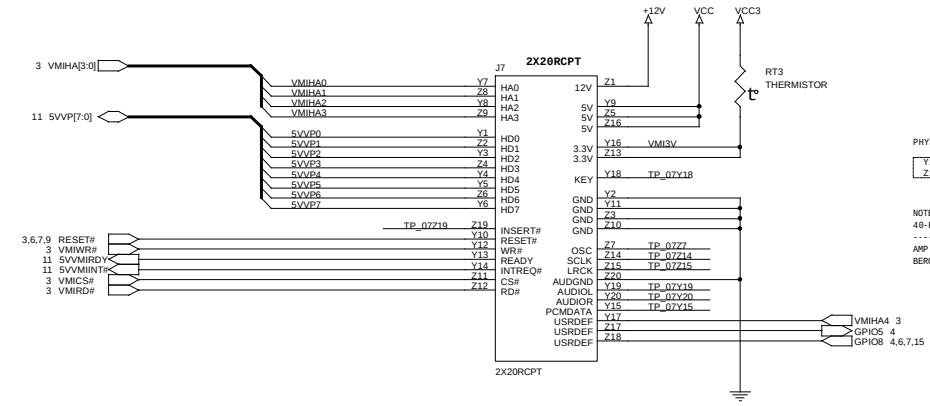
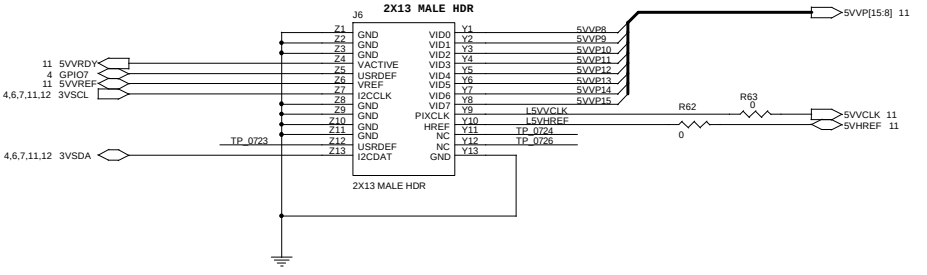


PHYSICAL PINOUT VIEW OF THE 40 PIN HEADER (COMPONENT SIDE)

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y20
Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13	Z14	Z15	Z16	Z17	Z18	Z19	Z20

NOTE:
40-PIN FEMALE HEADER RECOMMENDED PARTS

AMP PART# 2-535598-3
BERG PART# 68683-320



PHYSICAL PINOUT VIEW OF THE 26 PIN HEADER (COMPONENT SIDE)

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13
Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13

NOTE:
26-PIN MALE HEADER RECOMMENDED PARTS

AMP PART# 1-103186-3
BERG PART# 67997-426

Title	VMI Video Connectors	
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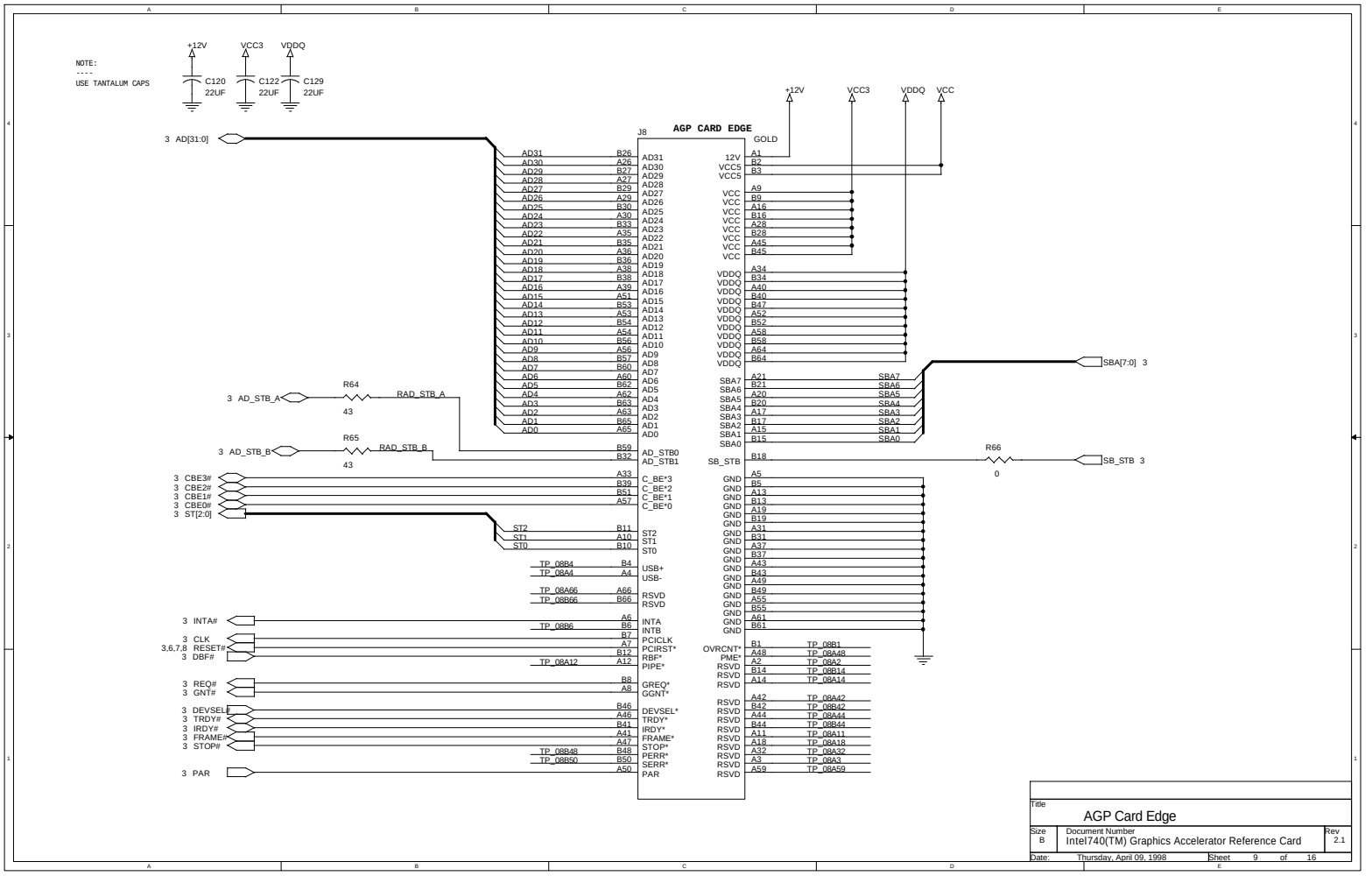
NOTE:

USE TANTALUM CAPS
+12V
VCC3
VDDQ
C120
22UF
C122
22UF
C129
22UF
J8
AGP CARD EDGE
GOLD
3 AD[31:0]
3 AD_STB_A
R64
43
RAD_STB_A
3 AD_STB_B
R65
43
RAD_STB_B
3 CBE3#
3 CBE2#
3 CBE1#
3 CBE0#
3 ST[2:0]
3 INTA#
3 CLK
3,6,7,8 RESET#
3 DBF#
3 REQ#
3 GNT#
3 DEVSEL#
3 TRDY#
3 IRDY#
3 FRAME#
3 STOP#
3 PAR
SBA[7:0] 3
SB_STB 3
R66
0
AD_STB0
AD_STB1
C_BE*3
C_BE*2
C_BE*1
C_BE*0
ST2
ST1
ST0
USB+
USB-
RSVD
INTA
INTB
PCICLK
PCIRST*
RBF*
PIPE*
GREQ*
GGNT*
DEVSEL*
TRDY*
IRDY*
FRAME*
STOP*
PERR*
SERR*
PAR
OVRCNT*
PME*
SBA7
SBA6
SBA5
SBA4
SBA3
SBA2
SBA1
SBA0
SB_STB
12V
VCC5
VCC
VDDQ
GND
TP_08B4
TP_08A4
TP_08A66
TP_08B66
TP_08B6
TP_08A12
TP_08B48
TP_08B50
TP_08B1
TP_08A48
TP_08A2
TP_08B14
TP_08A14
TP_08A42
TP_08B42
TP_08A44
TP_08B44
TP_08A11
TP_08A18
TP_08A32
TP_08A3
TP_08A59
Title
AGP Card Edge
Size
B
Document Number
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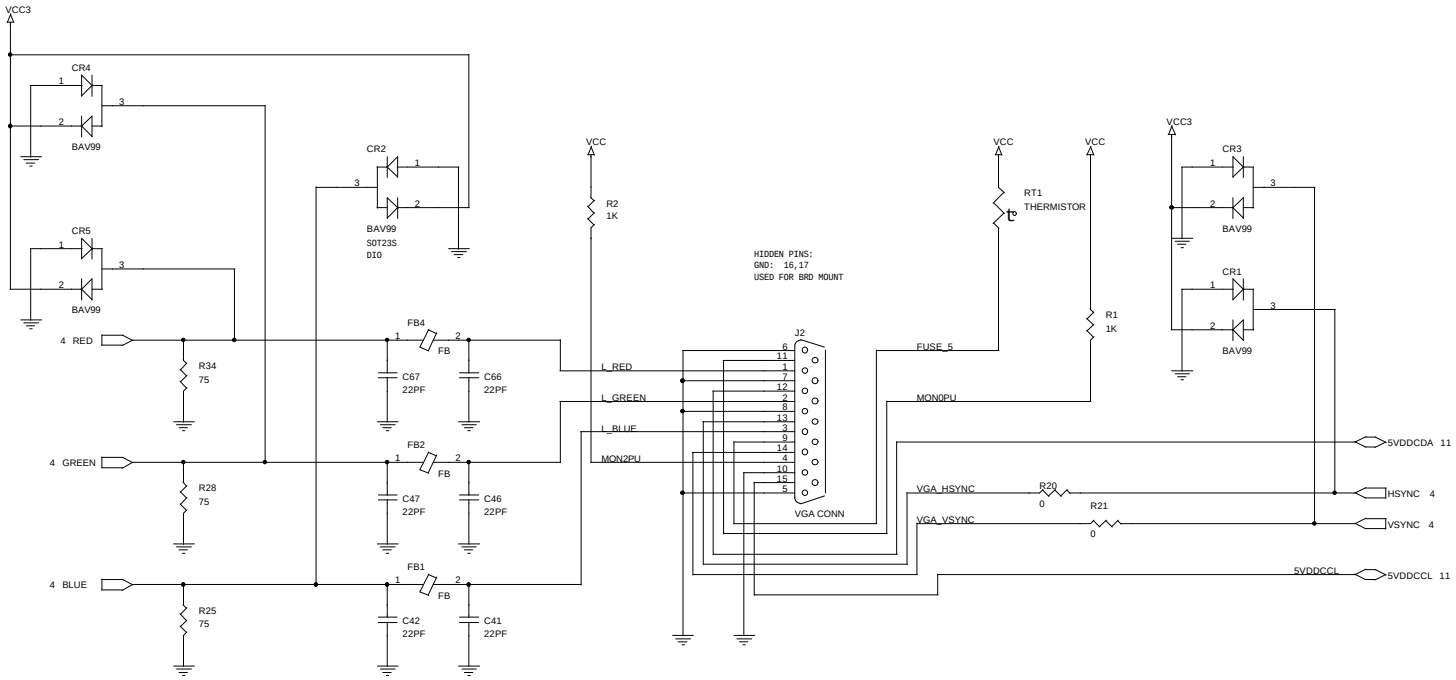

Title	VGA Connector	
Size: B	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
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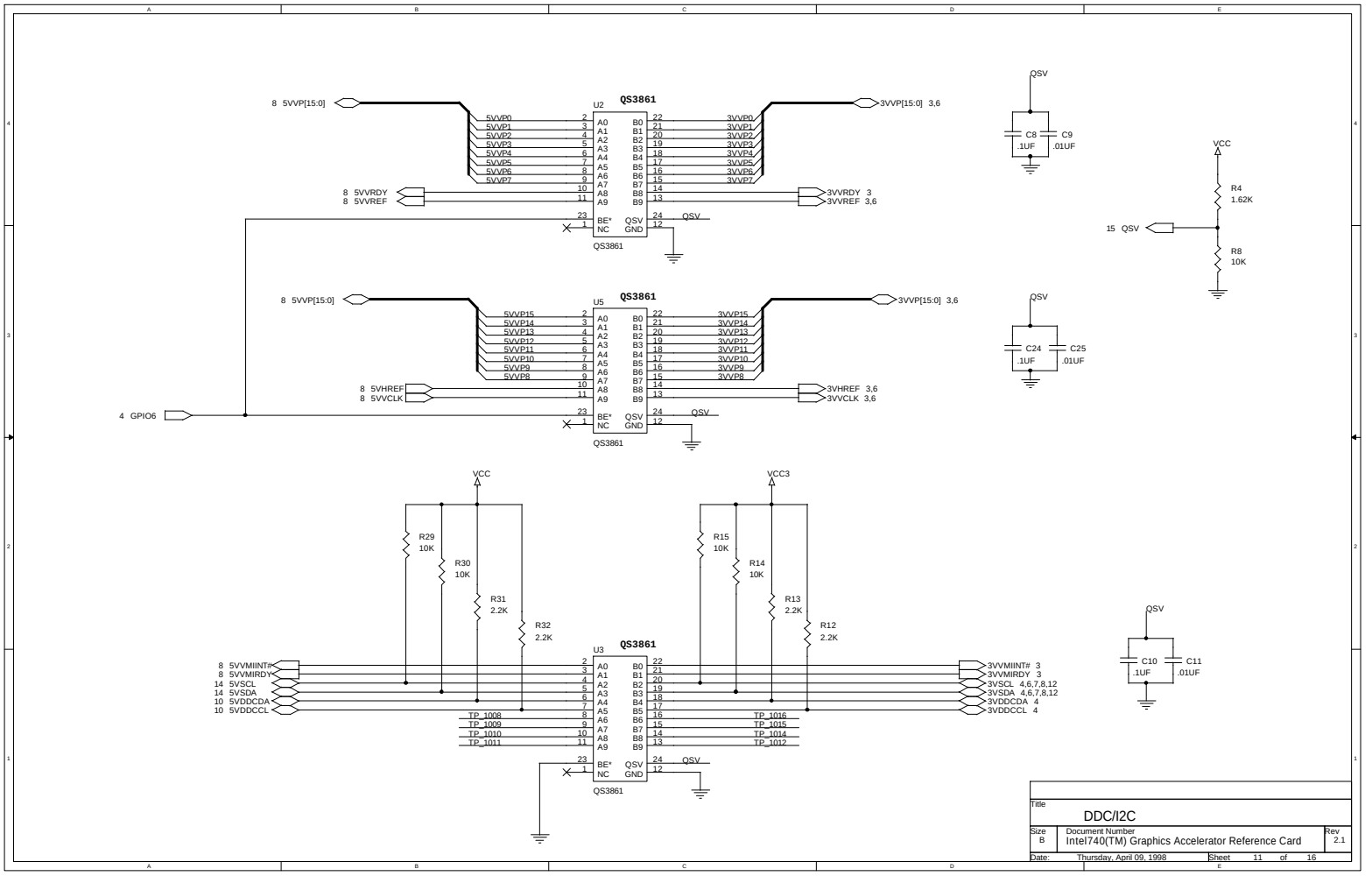
U2
QS3861
8 5VVP[15:0]
5VVP0
5VVP1
5VVP2
5VVP3
5VVP4
5VVP5
5VVP6
5VVP7
3VVP0
3VVP1
3VVP2
3VVP3
3VVP4
3VVP5
3VVP6
3VVP7
3VVP[15:0] 3,6
8 5VVRDY
8 5VVREF
3VVRDY 3
3VVREF 3,6
BE*
NC
QSV
GND
QS3861
U5
QS3861
8 5VVP[15:0]
5VVP15
5VVP14
5VVP13
5VVP12
5VVP11
5VVP10
5VVP9
5VVP8
3VVP15
3VVP14
3VVP13
3VVP12
3VVP11
3VVP10
3VVP9
3VVP8
3VVP[15:0] 3,6
8 5VHREF
8 5VVCLK
3VHREF 3,6
3VVCLK 3,6
4 GPIO6
QS3861
U3
QS3861
8 5VVMIINT#
8 5VVMIIRDY
14 5VSCL
14 5VSDA
10 5VDDCDA
10 5VDDCCL
TP_1008
TP_1009
TP_1010
TP_1011
TP_1016
TP_1015
TP_1014
TP_1012
3VVMIINT# 3
3VVMIIRDY 3
3VSCL 4,6,7,8,12
3VSDA 4,6,7,8,12
3VDDCDA 4
3VDDCCL 4
QS3861
QSV
C8
C9
.1UF
.01UF
C24
C25
.1UF
.01UF
C10
C11
.1UF
.01UF
VCC
R4
1.62K
15 QSV
R8
10K
VCC
R29
10K
R30
10K
R31
2.2K
R32
2.2K
VCC3
R15
10K
R14
10K
R13
2.2K
R12
2.2K
Title
DDC/I2C
Size
B
Document Number
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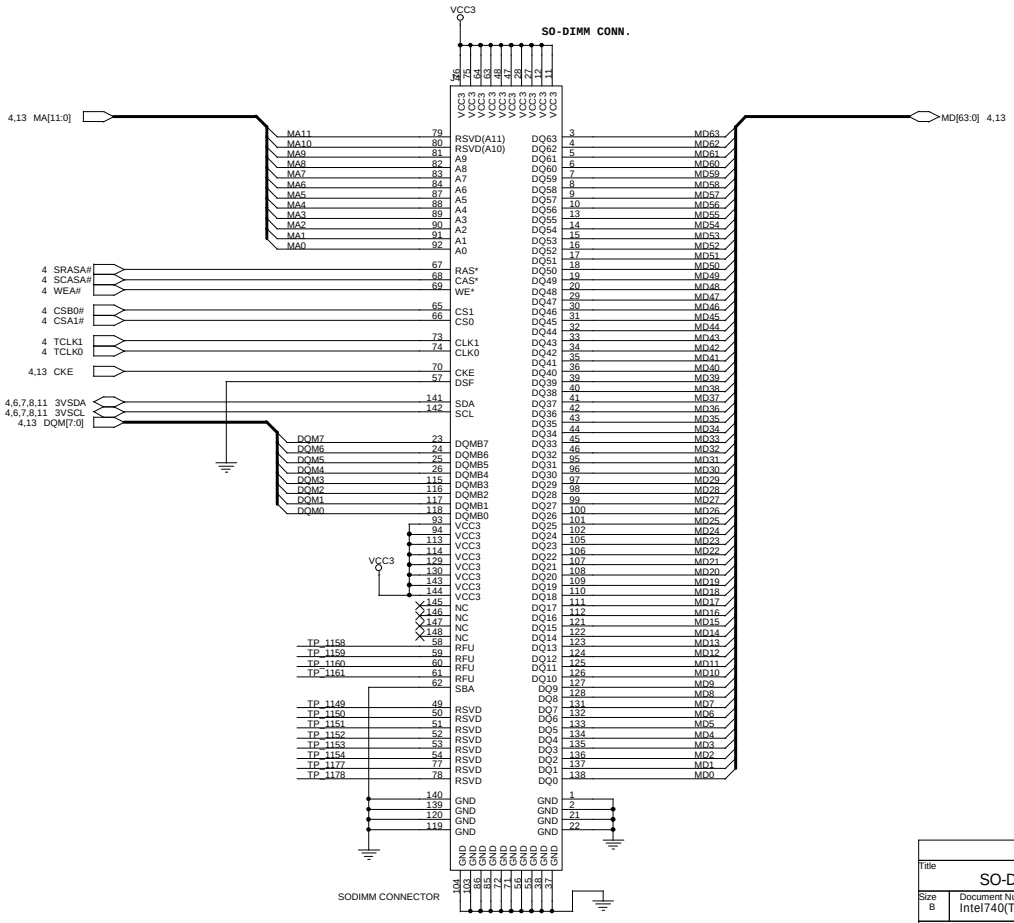

Title	SO-DIMM Connector	
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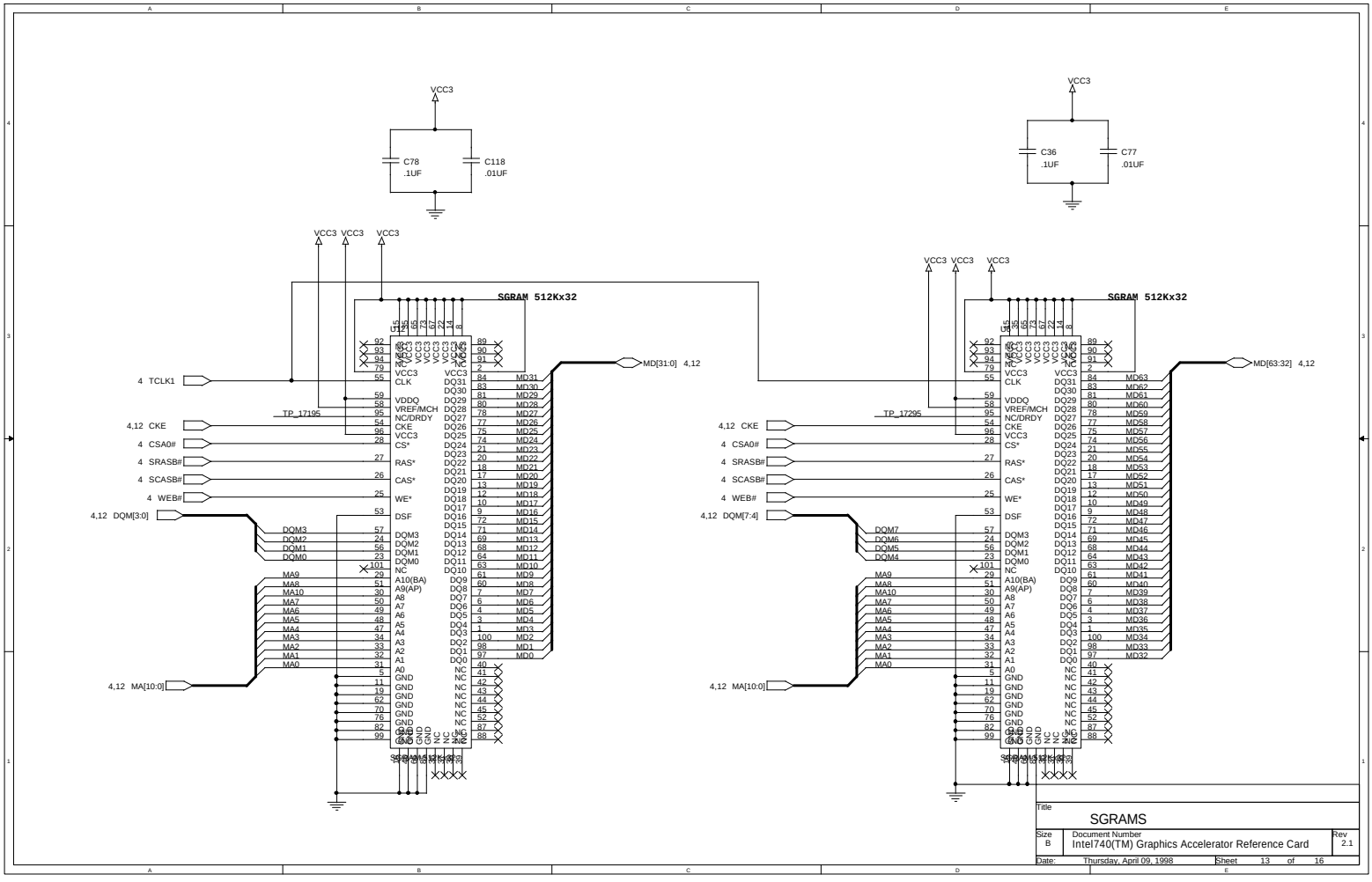

Title	SGRAMS	
Size: B	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
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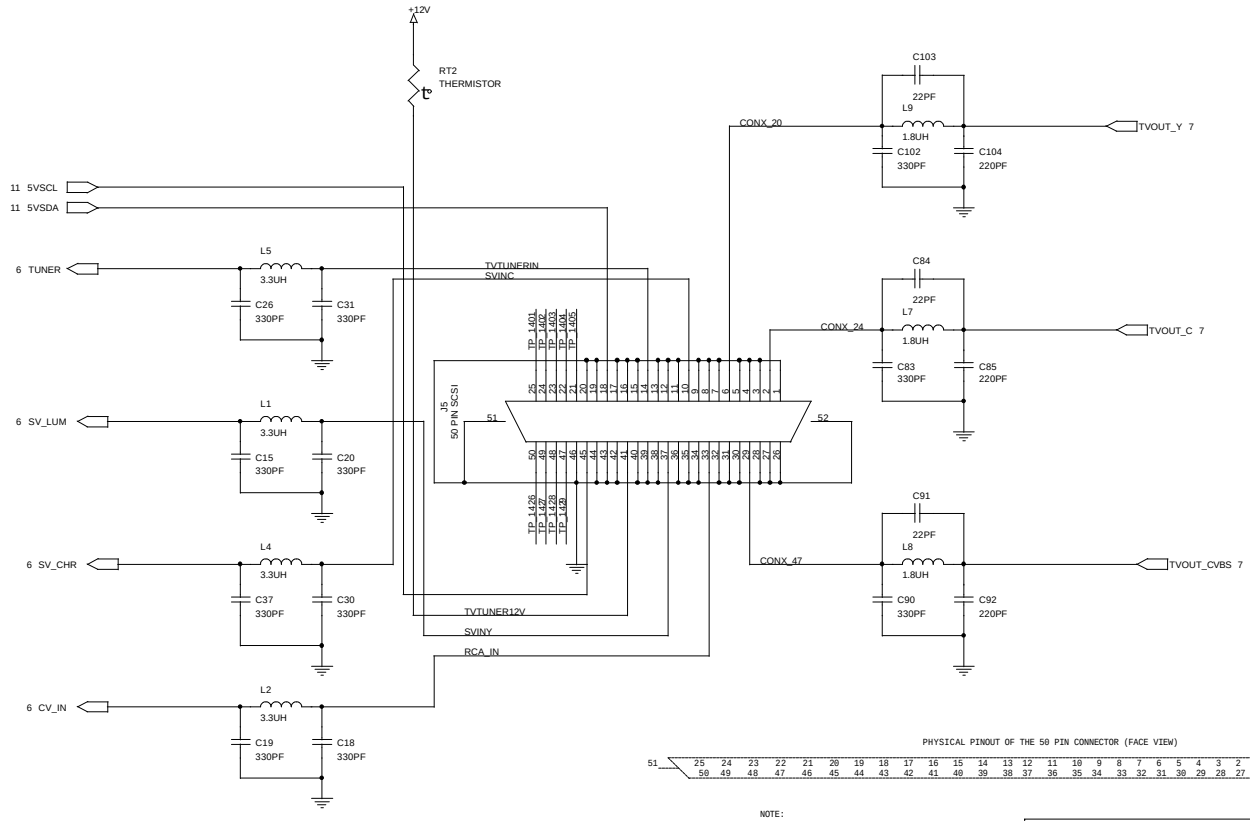

PHYSICAL PINOUT OF THE 50 PIN CONNECTOR (FACE VIEW)

NOTE:
50-PIN FEMALEL SCSI CONNECTOR RECOMMENDED PART

AMP PART# 787170-5

Title: Video Connector		
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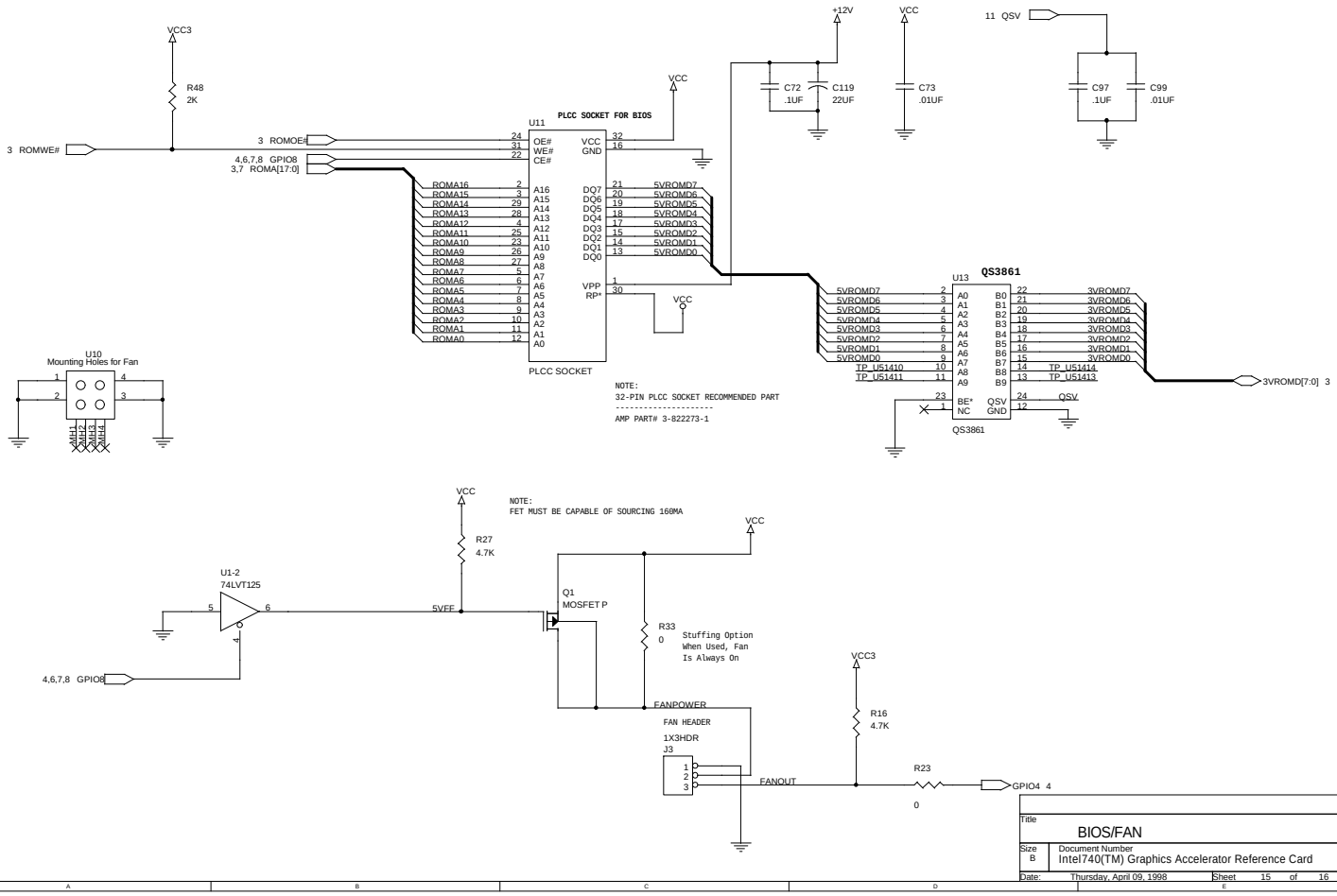

Title	BIOS/FAN	
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1.1 REVISIONS

PULL-DOWN REISITOR ON GPIO4 REMOVED
SIGNAL GPI05 ADDED TO VMI 2X20 HEADER ON PIN Z18
FAN FAIL SIGNAL REMOVED FROM QSWITCH
OE# ON INTEL740(TM) GRAPHICS ACCELERATOR OSCILLATOR PULLED HI TO 3.3V
MEMORY ADDRESSES 8,9 AND 10 FROM INTEL740 CONNTECTED TO 9,10 AND 8 OF SODIMM CONNECTOR, RESPECTIVELY
GPIO4 PULLED UP TO 3.3V THRU 4.7K RESISTOR

1.2 REVISIONS

MEMORY ADDRESSES 8,9 AND 10 FROM INTEL740(TM) GRAPHICS ACCELERATOR CONNECTED TO 8,9 AND 10 OF
SODIMM CONNECTOR, RESPECTIVELY
POWER SUPPLY VDDQ3 CHANGED TO VDD

1.3 REVISIONS

REMOVED 1UF CAP BETWEEN PIN 1 AND GND OF LT1575 ON P.4
ADDED 1UF CAP TO VCC3 NEAR PIN 1 OF HEXFET ON P.4
REPLACED 220UF CAP WITH 100UF CAP ON P.4
LAYOUT NOTE ADDED TO P.4

1.4 REVISIONS

SIGNAL NAMES L_RED, L_GREEN, L_BLUE CHANGED TO L_RED, L_GREEN AND L_BLUE, RESPECTIVELY, ON P.9
SIGNAL NAMES VGA_SHYNC AND VGA_VSYNC CHANGED TO VGA_HSYNC AND VGA_VSYNCE ON P.9
NET NAMES CONX 20, CONX 24 AND CONX 47 ADDED TO P.13
MOUNTING HOLES FOR FAN ADDED TO P.14
FOR HIDDEN PINS OF FAN MOUNTING HJOLES ADDED TO P.1
AGND CHANGED TO GND GLOBALLY
AVCC CHANGED TO VCC GLOBALLY
ON HIDDEN PINS OF BT829ALV REMOVED FROM P.5
PROPERTY OF BT829ALV ADDED, HIDDEN PINS DESIGNATED AS ANALOG_GND CONNECT TO GND
POWER NOTES CHANGED ON P.1 TO REFLECT AGND AND AVCC REMOVAL

1.41

THE 4 GND RINGS OF FAN MOUNTING HOLES BROUGHT OUT EXTERNALLY P.14
THE 4 NC MOUNTING HOLES ARE STILL LEFT AS HIDDEN

1.42

0 OHM RESISTOR ADDED TO GPIO4 LINE ON P.14
UNSTUFFED 0 OHM RESISTOR ADDED BETWEEN DRAIN AND SOURCE OF PMOSFET ON P.14
PINOUT CHANGED ON INTEL740(TM) GRAPHICS ACCELERATOR ON PINS SPARE2, SPARE1, LEFT, VSYNC,
HSYNC, VREF, AND VCLK.
NEW PIN'S ARE H25, H26, J23, J25, J26, L23, & L24 RESPECTIVELY ON P.3.
NO OTHER PINS AFFECTED.

1.43

ADDED DISCLAIMERS TO P.1
ADDED NOTE REGARDING HIDDEN PINS OF VGA CONNECTOR ON P.1
AGP NOTE CHANGED TO A.G.P. ON P.8
COMPATIBILITY NOTE REMOVED FROM TITLE ON P.10
512X32 SGRAMS NOTE CHANGED TO JUST SGRAMS
BUTEO TV ENCODER NOTE CHANED TO BT869 VIDEO ENCODER
POWER PINS NOTE CHANGED TO HIDDEN POWER PINS ON P.1
BT829B NOTE CHANGED TO BT829ALV VIDEO DECODER ON P.1 & 5
ADDED NOTE ON P.4 REGARDING VARYING THE OUTPUT VOLTAGE OF REGULATOR
SIGNAL NAME XTL1 CHANGED TO XT1I ONP.5, PIN16 OF BT829ALV
SIGNAL NAME XT10 CHANGED TO XT1O ON P.5, PIN17 OF BT829ALV

1.44

NOTE ON HIDDEN VCC PINS FOR BT829ALV CHANGED, PIN 28 TO 38 ON P.1
POWER PLANE VDD CHANGED TO 3VAA_BT829 FOR 3 PROTECTION DIODES ON P.6
SIGNAL NAMES L_GATE, R_GATE, COMP1 M_COMP1 ADN FB1575 ADDED TO P.4
SIGNAL NAMES XT1CAP AND XT0CAP ADDED TO NETS ON P.5
SIGNAL NAMES XTALIN869, XTALOUT869, M_COMP2, COMP2, FSADJUST869, VBIAS869 AND VREF869 ADDED TO NETS ONP.6
SIGNAL NAME VM1SV ADDED TO NET ON P.7
SIGNAL NAME FANPOWER ADDED TO NET ON P.14

1.45

SIGNAL NAME CCVALID ADDED TO P.5

1.46

SIGNAL NAME GFX_OSC ADDED TO P.3
SIGNAL NAME MODE869 ADDED TO P.6, PIN 50 OF BT869
SIGNAL NAME PAL_MODE ADDED TO 1X3HDR ON P.6
SIGNAL NAME NTSC_MODE ADDED TO 1X3HDR ON P.6

1.46

NOTE STATING NEED A 10% VERSION CREATED REMOVED FROM P.8
POWER SUPLY VCC3 CHNAGED TO VCC ON C123 ON P.14
POWER SUPPLY VCC3 CHANGED TO VCC ON BIOS SKT ON P.14
SIGNAL NAME 5VSDA CHANEGD TO 3VSDA ON U9.Z13 ON P.7
AGP CONNECTOR NOTES ON PINS CHANGED ON P.8, NO SIGNAL NAMES WERE CHANGED ON THE CONNECTOR
NAMES GAD[31:0] CHANGED TO AD[31:0], SMB1 AND SMB0 CHANGED TO RSVD
GAD_STB0 AND GAD_STB1 CHANGED TO AD_STB0 AND AD_STB1, RESPECTIVELY
GC-BE*3,2,1,0 CHANGED TO CBE*3,2,1,0 RESPECTIVELY
GSTOP*, GPERR*, AND GPAR CHANGED TO STOP*, PERR*, SERR* AND PAR, RESPECTIVELY

1.5 REVISIONS

C39, C41, C42, & C44 CHANGED TO 15PF ON P.5, NO PACKAGE SIZE CHANGE NEEDED
SIGNALS XT1CAP AND XT0CAP RELOCATED SINCE XTAL FILTERS CHANGED ON P.5
L3 AND L4 ON P.5 CHANGED TO 4.7UH NAD LOCATION IN XTAL FILTER CIRCUIT CHANGED
PIN 36, 37, 80, & 85 CONNECTED TO VCC3 INSTEAD OF VCC ON THE BT829ALV ON P.5
R20 ON P.5 NOW CONNECTS TO VCC3 INSTEAD OF VCC
C20, C22, C23 AND C26 ON P.5 CHANGED FROM 0.1UF TO 1UF. THESE ARE THE AC CAPS TO MUX INPUTS.
THIS REQUIRED A PACKAGE SIZE CHANGED FROM 0805 TO 1206.
VCC CONNECTION TO PIN 59 OF BT829B (P.5) DELETED. WIRE LEFT OPEN AND RENAMED TP_0559.
REMOVED NOTE NEAR PIN 59 OF BT829B (P.5) WHICH STATED TIE TO ANALOG FENCE
DELETED R13, R18 & R19 FROM P.5 OF SCHEMATICS.
REPLACED C38 ON P.5 WITH A SHORT. THE SIGNALS MUXOUT AND YIN WERE THUS REMOVED AND RENAMED
AS ONE SIGNAL MUXOUT_YIN
SIGNAL NAME BROMWE# REMOVED FROM P.14
GPIO7 SIGNAL NAME AND NET REMOVED FROM P.14 AND CONNECTED TO PIN Z5 OF THE 2X13 HDR ON P.7
ROMWE# SIGNAL NO LONGER USES 74LVT125 ON P.14 BUT CONNECTS DIRECTLY TO BIOS PIN 31
PULL-UP RESISTOR TO VCC3, R13, ADDED ON P.14 AND CONNECTED TO THE ROMWE# SIGNAL
SIGNAL NAME TP_0709 REMOVED FROM 2X13 HDR ON P.7 AND CHANGED TO GPOI7
R63 ON P.6 CHANGED FROM 75 TO 100 OHMS
R62 REMOVED AND REPLACED BY A SHORT ON P.6
SIGNAL NAME M_COMP2 REMOVED FROM P.6
C112 REMOVED FROM P.6
BT829ALV NAME CHANGED TO BT829B ON P.1 AT 2 PLACES AND P.5 AT 2 PLACES
BT868, 869 TV OUT NOTE ON P.2 CHANGED TO VIDEO ENCODER
AGP CONNECTOR NOTE ON P.2 CHANGED TO A.G.P. CONNECTOR

1.6 REVISIONS

ALL REFERENCE DESIGNATORS CHANGED
HIDDEN POWER PINS NOTATION ON P.1 CHANGED

1.61 REVISIONS

50 PIN VIDEO PINOUT CHANGED ON P.13, PIN 1 NEEDED TO CHANGE DUE TO PAD PATTERN DEFINITION
DIAGRAM SHOWING THE PHYSICAL PINOUT OF THE 50 PIN VIDEO CHANGED ACCORDINGLY ON P.13
NOTE ON P.4 WHICH STATED ...R10 WITH THE ... CHANGED TO ...R35 WITH THE...
NOTE ON P.4 WHICH STATED ...R10 VOUT... CHANGED TO ...R35 VOUT...
NOTE ON P.4 WHICH STATED ...C12 TO C11... CHANGED TO ...C60 TO C61...
C21, C22, C33, & C34 ON P.5 CHANGD TO 22PF CAPS, SAME PACKAGE SIZE
L3 AND L6 ON P.5 CHANGED TO 2.7UH, SAME PACKAGE SIZE
C23 ON P.5 CHANGED TO 68PF, SAME PACKAGE SIZE
C35 ON P.5 CHANGED TO 100PF, SAME PACKAGE SIZE
REF DESIGNATOR FOR C16 ON P.4 CHANGED TO C40
REF DESIGNATOR FOR C40 ON P.5 CHANGED TO C16

1.7 REVISIONS

0 OHM RESISTOR TO GND ADDED TO GPIO8 SIGNAL ON P.3
PINS F01, AA01, F04 & AA04 REMOVED FROM HIDDEN PINS OF INTEL740(TM) GRAPHICS ACCELERATOR CONNECTED TO VCC3 ON P.1
PINS F01, AA01, F04 & AA04 ADDED TO INTEL740(TM) GRAPHICS ACCELERATOR SYMBOL AND CONNECTED TO SIGNAL VCC_PLL ON P.3
VCC2 NOTES ON P.1 CHANGED TO VCC_CORE TO REFLECT THE CORE POWER SUPPLY CHANGED ON P.4
HIDDEN INTEL740(TM) GRAPHICS ACCELERATOR PINS WHICH WERE CONNECTED TO VCC2 CHANGED TO CONNECT TO VCC_CORE
THE FOLLOWING ARE HIDDEN PINS WHICH WERE CONNECTED TO VCC2 CHANGED TO CONNECT TO VCC_CORE
E07, E09, E11, E13, E14, E16, E18, H22, AB07, AB09, AB11, AB13, AB14, AB16, AB18, AB20
OUTPUT OF REGULATOR SIGNAL NAME CHANGED TO VCC_REGULATED FROM VCC2 ON P.4
TWO 0 OHM RESISTORS ADDED, BOTH CONNECTED TO VCC_CORE, ONE CONNECTED TO VCC_REGULATED,
THE OTHER VCC3 ON P.4
ANOTHER TWO 0 OHM RESISTORS ADDED, SMALLER PACKAGE, BOTH CONNECTED TO VCC_PLL
ONE CONNECTED TO VCC_REGULATED, THE OTEHR VCC3 ON P.4
ADDED ON P.4 TO DESCRIBE THE RESISTOR STUFFING OPTIONS FOR CORE AND PLL POWER
CHANGED PMOSFET ON P.14 FROM A 3 PIN DEVICE TO A 4 PIN DEVICE, THE MIDDLE PIN (2) AND THE
TAB (4) ON TEH PHYSICAL DEVICE ARE ELECTRICALLY THE SAME, BOTH ARE DRAINS
VCC2 POWER SYMBOL CONNECTED TO DECOUPLING CAPACITORS ON P.4 CHANGED TO VCC_CORE'
VCC2 NO LONGER EXISTS

1.8 REVISIONS

REFERENCE DESIGNATORS CHNAGED ACCORDING TO PHYSCIAL LOCATION ON BOARD BY LAYOUT COMPANY

1.9 REVISIONS

NOTES ON REFERENCE DESIGNATORS ON PAGE 1 UPDATED
NOTE REGARDING 0 OHM STUFFING OPTIONS ON P.4 CHANGED
NOTE REGARDING DEFAULT POWER CONFIGURATION ADDED TO P.4
HIDDEN RULE ON AD<31:0> CHANGED TO HIDDEN

2.0 REVISIONS

OSC Y3 VALUE CHANGED TO 66.6667MHz (p.4)

2.1 REVISIONS

Made Power Pins Visible and changed names to match the Datasheet,
Swapped pin numbers for WEA# and WEB# (p.3,4)

Made power pins visible (p.6)

Changed VCC3 voltages on part to 3VAA_BT869,
Changed R58 to 100 ohms (p.7)
Pin A3 on AGP connector disconnected from Ground,
changed VDD to VDDQ (p.9)
Made power pins visible (p.11)

Made power pins visible, Changed Clock Routing (p.12)

Made power pins visible (p.13)

Added descriptive text to Fan control, made
power pins visible (p.15)

Title: Revision History		
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3

Intel740™ Graphics Accelerator 3 Device AGP Motherboard Design

3 Device AGP MotherBoard Design 3

3.1 Introduction

This chapter provides design guidelines for developing a 3 device AGP motherboard based on the Pentium II® processor, Intel® 440BX AGPset, and the Intel740™ graphics accelerator. The main focus of this chapter is the guidelines for developing a 3-point AGP solution with the Intel740 graphics accelerator. The configuration for the 3-point AGP is to have an 82443BX (Target) with two AGP masters.

- One AGP master is located on the motherboard (Intel740 Graphics Accelerator) along with the target, and
- Another AGP master is located on an add-in card that connects to the motherboard through a standard AGP connector.

Only one AGP master is enabled at any one time. When the add-in card is installed in the system, the AGP master on the add-in card is the only one that may be enabled. The Intel740 graphics accelerator on the motherboard may be enabled only when the add-in card is removed from the system. The desire for a 3-point AGP solution is to allow an upgrade path from the master device on the motherboard to a master device on an add-in card.

This section contains references to sections already discussed in the reference card section of this design guide. Since the focus of this section is only the 3-point AGP implementation with the Intel740 graphics accelerator, many of the layout and routing guidelines for the motherbaord are referenced to the *Intel® 440BX AGPset Design Guide*.

3.1.1 Overview

The reference 3 device AGP motherboard design described in this document contains the following features.

- Full support for a Pentium® II processor (DS1P), with system bus frequencies of 100/66 MHz
- Intel 440BX AGPset
  - 82443BX Host Bridge Controller
  - 8237EB PCI ISA IDE Accelerator (PIIX4E)
- 100/66 Mhz Memory Interface: A wide range of DRAM support including
  - 64-bit memory data interface plus 8 ECC bits and hardware scrubbing
  - SDRAM (Synchronous) DRAM Support only for desktop and server applications
  - 16Mbit, 64Mbit DRAM Technologies
- 2 PCI Add-in Slots
  - PCI Specification Rev. 2.1 Compliant
- 1 Shared PCI/ISA Add-in Slot
- 1 AGP Slot
  - AGP Interface Specification Rev 1.0 Compliant
  - AGP 66/133 MHz, 3.3V device support

- Intergrated IDE Controller with Ultra DMA/33 support
  - — PIO mode 4 transfers
  - — PCI IDE Bus Master Support
- Intergrated Universal Serial Bus (USB) Controller with 2 USB ports
- Intergrated System Power Management Support
- On-board Floppy, Serial, Parallel Ports,
- Intel 740 Graphics Accelerator
  - — Accelerated Graphics Port (AGP) Interface
  - — Memory
    100 MHz SDRAM or SGRAM Support
    2,4 MB Solder-Down Option

3.1.2 About This Chapter

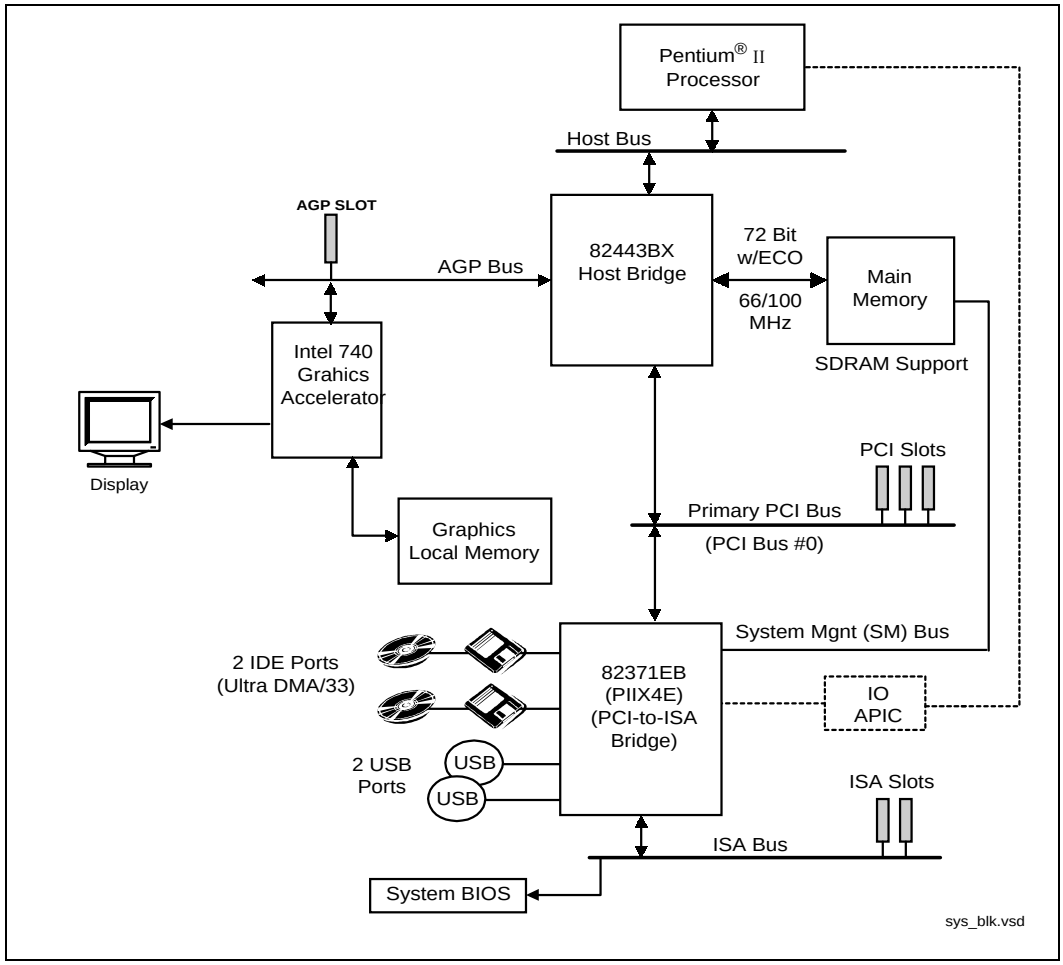
This chapter is intended for hardware design engineers who are experienced in the design of PC motherboards or memory subsystem. This document is organized as follows:

- Section 1, "Introduction"—This section provides an overview of the features of a 3-point AGP reference design (DS1P/440BX/I740). Chapter 1 also provides a general component overview of the Pentium II processor, Intel 440BX AGPset, and the Intel 740 graphics accelerator. This section also provides implementation issues associated with a 3-point AGP design and design recommendations which Intel feels will provide flexibility to cover a broader range of products within a market segment.
- Section 3.2, "3 Device AGP Motherboard Layout and Routing Guidelines"—This section provides detailed layout, routing, and placement guidelines for the AGP bus and local memory subsystem. Design guidelines for other buses (Host GTL+, PCI, and DRAM) are covered in the Intel 440BX AGPset design guidelines.
- Section 3.3, "3 Device AGP Motherboard Reference Design Schematics"—This chapter provides the schematics used in the reference design.

3.1.3 Block Diagram

Figure 3-1 shows a block diagram of a typical platform based on the Intel 440BX AGPset with the Intel740 graphics accelerator. The 82443BX system bus interface supports up to two Pentium II processors at the maximum bus frequency of 100 MHz. The physical interface design is based on the GTL+ specification and is compatible with the Intel 440BX AGPset solution. The 82443BX provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3V DRAM technologies.

Figure 3-1. Pentium® II Processor / Intel® 440BX AGPset/Intel 740 Graphics Accelerator System Block Diagram



3.1.4 Implementation Issues

The following are design issues involved in implementing a 3-load AGP bus. These issues must be studied and implemented carefully in order to produce a functional design.

3.1.4.1 Disabling A Master Device

There are two master devices that must each have the ability to be disabled in a logical point-to-point bus. These devices are the master graphics controller on the motherboard and the master graphics controller on the AGP add-in card. Several issues effect the ability to, and the way in which, a master graphics controller is disabled.

One issue concerns the add-in card and the other concerns the graphics controller components themselves. Since the current AGP specification has made no provision for a general method of disabling a master device, this function must be defined for on an individual basis depending on the operating characteristics of each master device. The graphics controller that is used as the down device on the motherboard must have a mechanism that disables the device in a manner acceptable to the implementation of a logical point-to-point bus. The Intel 740 has such a mechanism that

allows it to be put in a low power state. In this low power state, the Intel740 chip is disabled and will not initiate or respond to cycles on the AGP bus. In addition, the power consumption of this device in this state is less than 1 Watt. To put the Intel740 chip into the low power mode, the following sequence of events must occur in the order stated.

1. ROMA16 must be asserted (high) at the trailing edge of the Intel740 chip RESET#
2. At least one AGP/Core clock before TEST is asserted the following signals must driven to the state listed in Table 3-1

Table 3-1. State of Signals to be Driven After System Reset but at Least One Clock Prior to Asserting TEST

Signal	State
WEB#	0
SCASB#	1
SRASB#	0
CS0B#	0
CS1B#	0

3. TEST is asserted (asserted =high = 1)

3.1.4.2 Low Power Logic Implementation

Two signals, GPO27# and GPO 28#, from the PIIX4E are used in this design. GPO28 in conjunction with ROMA16 and PCIRST# are used to put the Intel740 chip in low power mode (see Figure 3-2). The additional logic for driving WEB#, SCASB#, SRASB#, CS0B#, CS1B# and TEST is illustrated in Figure 3-2.

A hardware reset to the Intel740 chip takes the device out of the low power state. Since the PCIRST# signal is used to disable the device, it can not be used for this purpose. GPO27 serves as the hardware reset to reset the Intel740 chip. At the trailing edge of GPO27, the Intel740 chip will be functional.

Figure 3-2. The Schematic Diagram for GPO27#, PCIRST# (System Reset), RESET#, ROMA16 Signals

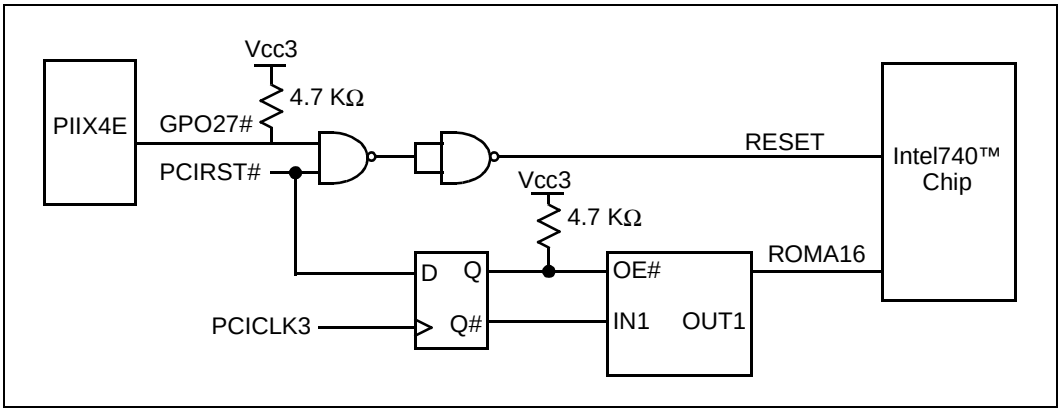
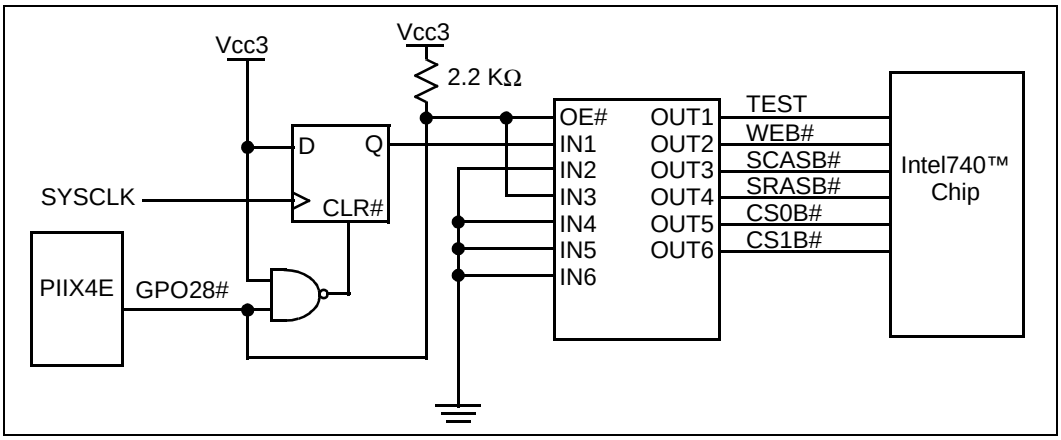


Figure 3-3. The Schematic Diagram for the WEB#, SCASB#, SRASB#, CS0B#, CS1B# and TEST



3.1.4.3 GPO27# and GPO28# Signal Duration

Table 3-2. Signal Duration of the GPO Signals from PIIX4

Signal	Active	Minimum Duration	Actual Duration[1]
GPO27 from PIIX4	Low (0)	1ms	1ms
GPO28 from PIIX4	Low (0)	see note [2]	1ms

NOTE:
1. 1ms is the smallest system BIOS increment of time
2. This is the propagation delay from when GPO28# is asserted to valid output at TEST.

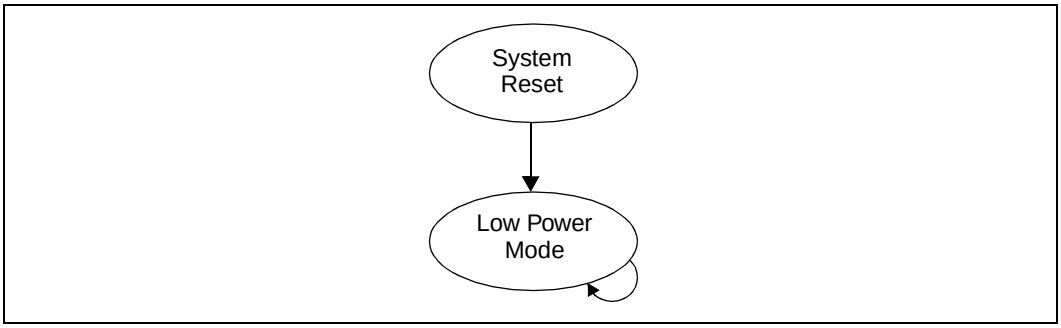
Controls Signals From the PIIX4

GPO27 takes the device out of low power mode and puts it into functional mode. The duration of the GPO27 signal should be the minimum of 1ms (see Table 3-2). This requirement is set by the minimum reset time defined in the Accelerated Graphics Port Interface Specification, Revision 1.0.

GPO28 puts the device into low power mode and should be a minimum duration of the sum of the propagation delay for logic depicted in Figure 3-2.

3.1.5 State Diagrams

Figure 3-4. Intel740™ Graphics Controller (On Board Device) Remains in Low Power Mode

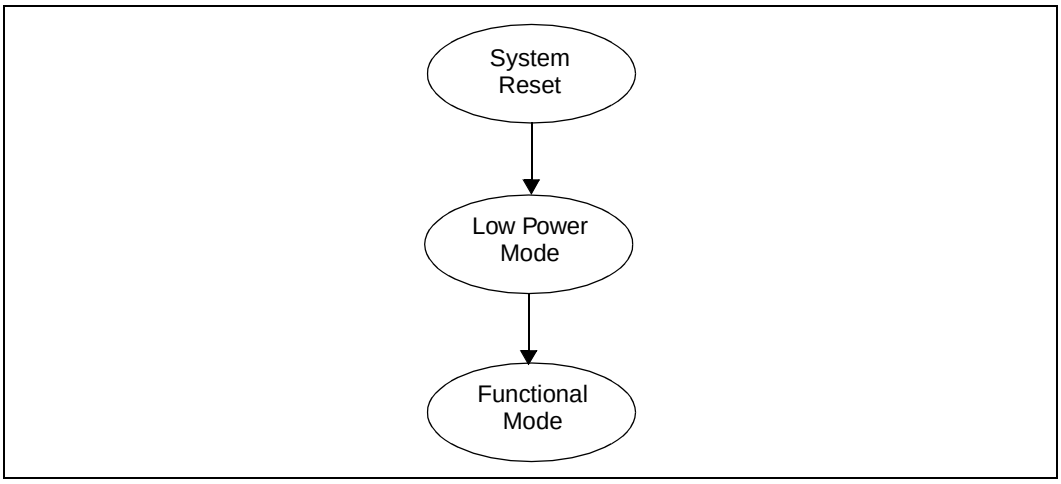


At system RESET, the Intel740™ graphics controller on the motherboard is always put into the low power state. The following are examples in which the on board device shall remain in low power state:

- AGP add-in card is present
- PCI or ISA graphics device is the primary and only graphics device desired
- Multimonitor configurations not utilizing the on board graphics device.

Note: When not in use, both GPO27 and GPO28 should be driven high (1).

Figure 3-5. Intel740™ Graphics Controller (On Board Device) State Diagram



The Intel740 graphics controller down on the motherboard enters the low power mode at system reset. If an enabling event occurs, the device enters the functional mode from the low power mode (See Figure 3-5).

The following are examples in which functional mode would be invoked:

- Intel740™ graphics accelerator as the primary and only graphics device
- Multimonitor configurations utilizing the Intel740™ graphics controller

3.1.5.1 Signal Quality and Timing Issues

There are two modes of operation for the AGP bus, each with it's own signal quality and timing issues. These two operating modes are 1X mode and 2X mode. Because 1X mode is a common clock mode, flight time of the signal is of the most importance. Both minimum and maximum flight time must be verified. The quality of the signal will also effect the flight time and therefore must also be taken into consideration.

In AGP 2X mode operation the two major areas of concern for signaling are timing skew between the data group signals and their associated strobe signals, and the signal quality of these signals. The skew in a AGP 2X mode bus is comprised of elements that include crosstalk, settling time, component loading differences, and line length differences. Bus topology effects all the above mentioned factors of signal skew except component loading differences.

Signal quality issues may also arise from the nature of the 3-load bus topology. These signal quality issues are caused by the loading and reflections inherent in this topology. Signal quality problems can effect timing and skew by violating edge quality, ringback, and overshoot criteria.

The topology of the logical point-to-point bus only makes these signal quality and timing issues worse since this type of bus contains signal loading from the third device located somewhere in the middle of the bus and the addition of trace stubs in the bus. The loading and trace stubs create a complex allowable routing topology with regard to trace length and component placement. Careful simulation of the bus topology is mandatory to verify proper operation of the AGP system. Both the case where an add-in card is present in the system and the case where the add-in card is not in the system must be evaluated for a complete solution. Depending on how the system is designed the bus will become balanced or unbalanced depending on the add-in card being in or out of the system. Specific design issues faced in implementing a logical point-to-point bus will be discussed in detail in the following sections of this document.

3.1.5.2 Strobe Edge Quality Issues

Due to the high speed nature of 2X mode AGP transfers, an AGP bus design must take into account all aspects of edge and signal quality. Areas of signal quality concern are edge quality, ringback, overshoot, and settling time.

Since the strobe signals act like clocks in 2X mode, their edge signal quality is paramount. Any nonmonotonic signal edges or ledges (steps) occurring in the switching region may cause double clocking or erratic behavior in the input buffer. Nonmonotonic edges and steps in the signal edge while not in the switching region will add to the flight time on the strobe signal and may increase the strobe to data group skew. This added skew may cause the system to fail. The switching region for 2X mode ranges from Vil (0.3Vddq) to Vih (0.5Vddq) centered around a switch point of 0.4Vddq.

Rising and falling edge ringback may also cause double clocking on strobe signals if these ringback levels are large enough. Ringback is analogous to Noise margins. When a noise margin is negative the signal requirements are not met and double clocking could occur. The violation criteria for strobe signal ringback is the same as the above edge quality region. Rising edge ringback may not go below Vih (0.5Vddq), and falling edge ringback may not exceed Vil (0.3Vddq).

See the section on Sensitivity Analysis later in this document for a full explanation of signals quality measurements.

3.1.5.3 Clock Issues

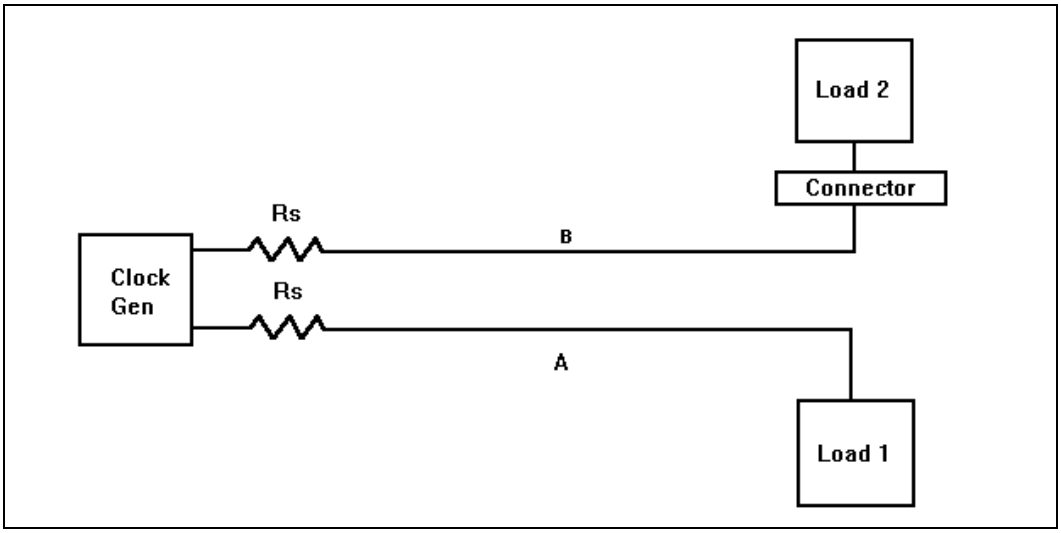
Supplying a clock to both AGP master devices raises issues that must be considered when implementing a logical point-to-point bus. Among these issues are clock signal quality, routing, and clock skew. Signal quality and routing are of a major concern since the clock now must be routed to both master components.

A separate clock driver was used to drive the AGP clocks on this design. The topology for each clock is point-to-point and no segment tuning between master devices is required. However, each clock length must still be tuned to the target clock for clock skew reasons. Since separate clock drivers are used, the skew between clock driver outputs must be taken into account in the overall clock skew budget. The output to output skew for the clock chip was 0.25 ns.

Skew between each AGP master clock input and the AGP target (chipset) must be within the 1ns limit called out in the AGP specification, Since we had a driver skew of 0.25ns due to the clock drivers, this meant that our propagation delays and settling times skews could not exceed 0.75 ns. This means that for a single clock driver solution not only must each of the two clock trace segments be balanced in such a way that signal quality is acceptable, but the trace segments must be tuned in such a way as to meet the AGP specified skew requirements.

The clock topologies used are shown in Figure 3-6. This figure shows the clock topology if three clock outputs are available. Each clock is a direct connection to it's respective load. Here the trace segments A and B must be balanced with respect to the target device clock trace in such a way as to meet system clock skew requirements. As mentioned previously, the clock generator output to output skew must also be factored into the overall system clock skew budget. In this topology the AGP target device is assumed to have a separate clock driver and is not shown here.

Figure 3-6. Point-to-Point Topology



3.1.6 Design Recommendations

3.1.6.1 Voltage Definitions

For the purposes of this document the following nominal voltage definitions are used:

Vcc	5.0V
$Vcc_{3.3}$	3.3V
Vcc_{CORE}	Voltage is dependent on the five bit VID setting
$Vcc_{2.5}$	2.5V
V_{TT}	1.5V
V_{REF}	1.0V
$AGPV_{REF}$	3.3V
+2_7	2.7V
VDDQ3	3.3V

3.1.6.2 General Design Recommendation

For general design recommendations, refer to the *Intel 440BX AGPset Design Guide* sections 1.4.2 and 1.4.3.

3.2 3 Device AGP Motherboard Layout and Routing Guidelines

This section describes layout and routing recommendations to insure a robust design. Follow these guidelines as closely as possible. Any deviations from the guidelines listed should be simulated to insure adequate margin is still maintained in the design. Since the concentration of this section is mainly 3 Device AGP implementation, refer to the *Intel 440BX AGPset Design Guide* for the remaining design guidelines. It would be beneficial to have that design guide before tying to read this section. Sections that are referred to the *Intel 440BX AGPset Design Guide* are:

- Routing Guidelines
  - GTL+ Description
  - GTL+ Layout Recommendations
  - Single Processor Design
  - Additional Guidelines
  - Design Methodology
  - Performance Requirements
  - Topology Definition
  - Pre-Layout Simulation (Sensitivity Analysis)
  - Placement & Layout
- Placement & Layout
- Post-Layout Simulation
- Validation
  - Flight Time Measurement
  - Signal Quality Measurement

- Timing Analysis
- 82443BX Memory Subsystem Layout and Routing Guidelines
  - — 100/66 MHz 82443BX Memory Array Considerations
  - — 3 DIMM Memory Layout & Routing Considerations
  - — PCI BUS Routing Guidelines
  - — Decoupling Guidelines for an Intel 440BX AGPset Platform
  - — Intel 440BX AGPset Clock Layout Recommendations
- Design Checklist
- Debug Recommendations

3.2.1 BGA Quadrant Assignment

The ball connections on the Intel740™ graphics accelerator have been assigned to simplify routing and keep board fabrication costs down by enabling a 4-layer design. Figure 3-7 shows the four signal quadrants of the Intel740 graphics accelerator. Component placement should be done with this general flow in mind. This will simplify routing and minimize the number of signals which must cross. The individual signals within the respective groups have also been optimized to be routed using only 2 PCB layers.

A complete list of signals and ball assignments can be found in the Intel740™ Graphics Accelerator Datasheet.

Figure 3-7. Major Signal Sections

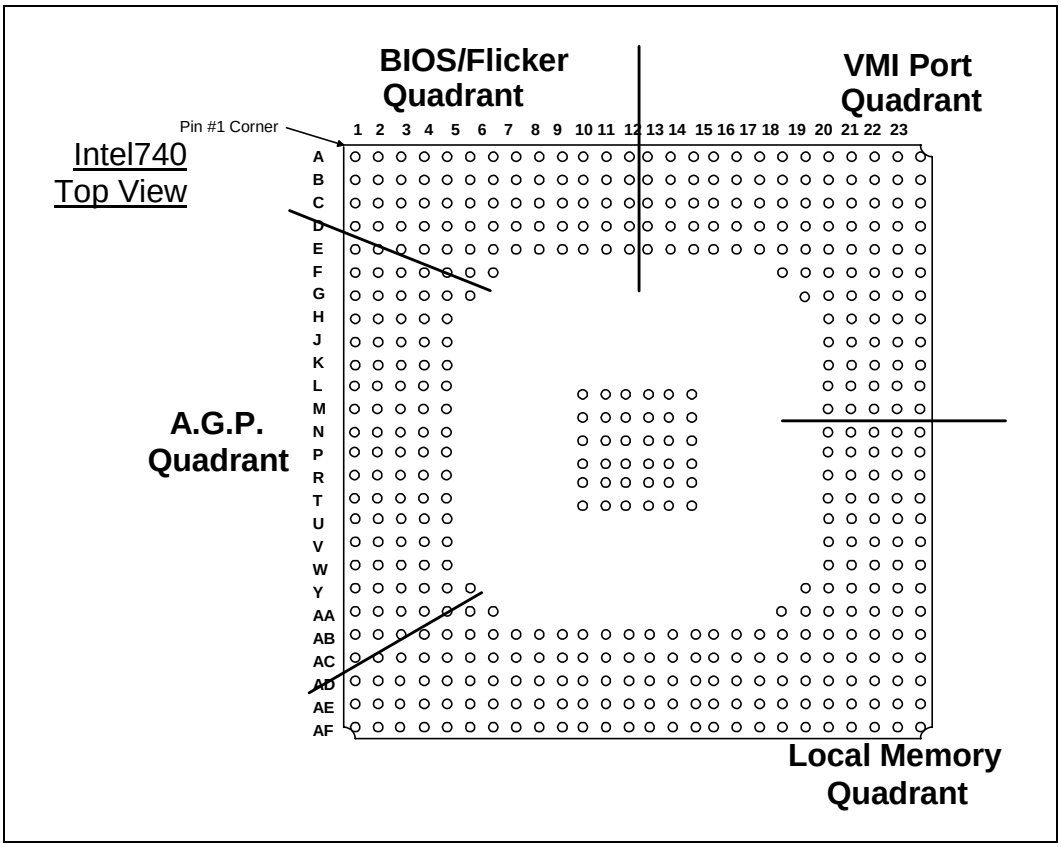
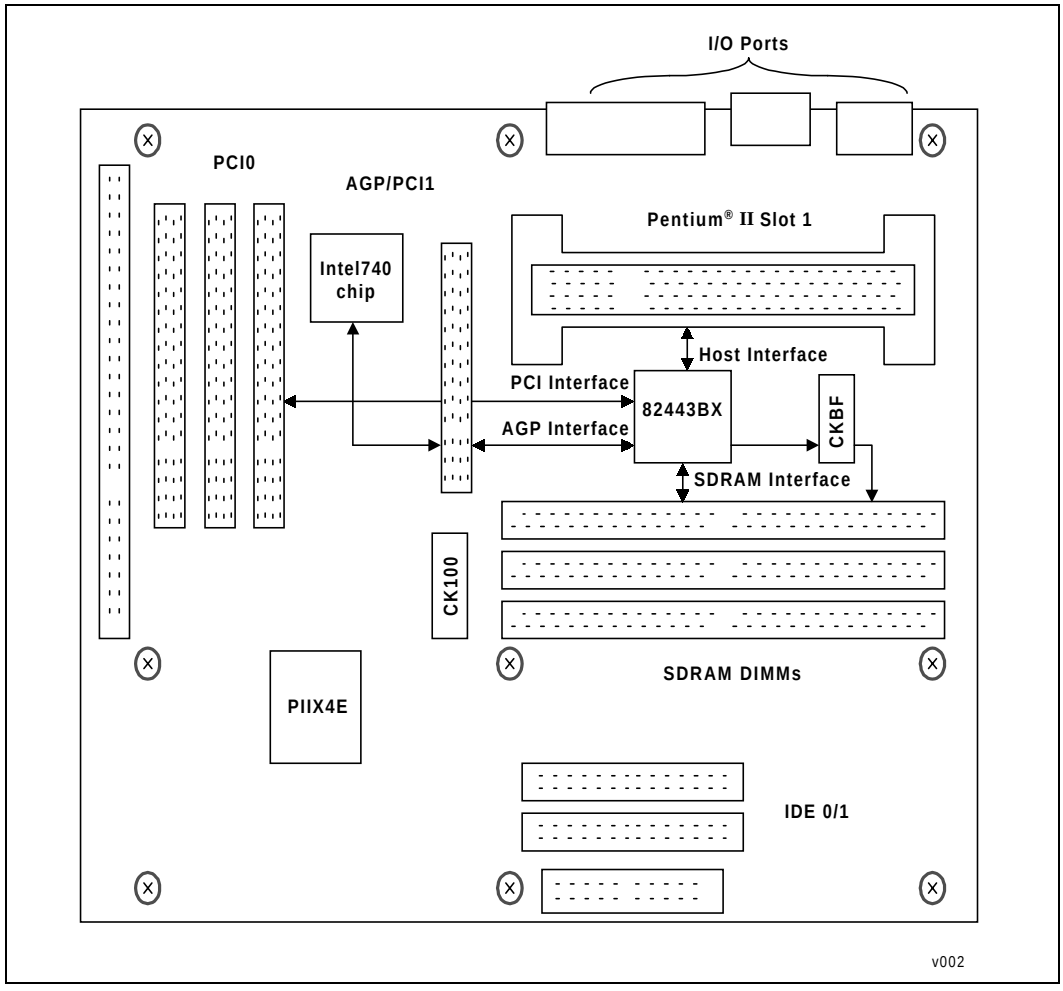


Figure 3-8 shows the proposed component placement for a single Pentium II processor for the ATX form factor design.

ATX Form Factor

1. The ATX placement and layout below is recommended for single (UP) Pentium II Processor / Intel 440BX AGPset/ Intel740 Graphics Accelerator system design.
2. The example placement below shows 1 Slot 1 connector, 2 PCI slots, 1 Shared slot, 3 DIMM sockets, and one AGP connector.
3. For an ATX form factor design, the AGP compliant graphics device can be either on the motherboard (device down option), or on an AGP connector (up option).
4. The trace length limitation between critical connections will be addressed later in this document.
5. Figure 3-8 is for ***reference only*** and the trade-off between the number of PCI and ISA slots, number of DIMM sockets, and other motherboard peripherals need to be evaluated for each design

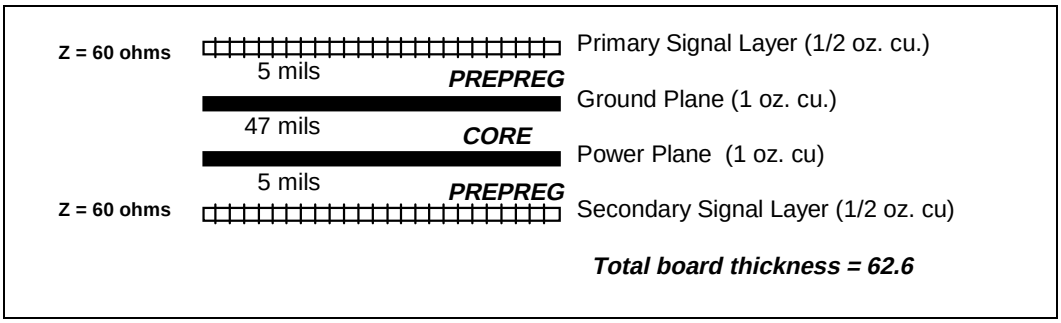
Figure 3-8. Example ATX Placement for a UP Pentium® II Processor / Intel® 440BX AGPset / Intel 740 Graphics Accelerator Design



3.2.2 Board Description

For a single Pentium II / Intel 440BX AGPset /Intel 740 Graphics Accelerator motherboard design, a 4 layer stack-up arrangement is recommended. The stack up of the board is shown in Figure 3-9. The impedance of all the signal layers are to be 65 Ω ±15%. Lower trace impedance reduces signal edge rates, overshoot & undershoot, and have less cross-talk than a higher trace impedance. A higher trace impedance increases edge rates and may slightly decrease signal flight times.

Figure 3-9. Four Layer Board Stack-up



Note that the top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will end up about 1 oz. cu. Check with your fabrication vendor on the exact trace impedance and PCB signal velocity value and insure that any signal simulation accounts for this.

Note: A thicker core may help reduce board warpage issues.

Additional guidelines on board buildup, placement and layout include:

- For a 4-layer single processor design, double ended termination is recommended for GTL+ signals. One termination resistor is present on the Pentium II processor, and the other termination resistor is needed on the motherboard. It may be possible to use single-ended termination, if the trace lengths can be tightly controlled to a 1.5” minimum and 4.0” maximum.
- The termination resistors on the GTL+ bus should be 56 ohms ±5%.
- The board impedance (Z) should be 65 ohms ± 15%.
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on a VCC plane, not the ground plane.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

3.2.3 3-point AGP Design Guidelines

3.2.3.1 Layout and Routing

With signal quality, timing, and clock issues in mind, a suitable bus layout and routing must be found. Careful simulation as described in the Sensitivity Analysis section of this document is essential. The nature of the logical point-to-point bus makes it a much harder topology to implement than a physical point-to-point bus. The following discussion will focus on some layout and routing issues associated with a logical point-to-point bus. The layout and routing for a logical point-to-point bus is determined either from simulation results or are verified from simulation

results. The benefit to the former method is that a solution space can be determined before any placement and routing is attempted. This saves time and effort over the method of route, simulate, adjust.

It is, therefore, recommended that the simulation results for the 3-load bus drive the layout and routing. The simulation results will produce a solution space for a particular set of buffer and board conditions. This solution space will give the lengths and conditions for all segments of the 3-load bus. It may be found that the given lengths and/or conditions governing the segments may not be able to be routed for the placement needed on a given board. If this is the case, several options may be pursued. The first is possible modifications to board placement of components. Placement may be adjusted so that the solution space is now able to be routed.

If placement changes are not achievable, tradeoffs in the solution space may be tried. As will be seen later in the Sensitivity Analysis section, changes in length requirements to a particular segment of the topology will result in changes to other segments allowable length and constraints. For example, the maximum allowed length of one segment may be to short to route but the maximum allowed length of another segment may not be needed. By shortening one segment's maximum allowable length, additional length may be gained in another segment to enable routing of the bus. In another case the solution space found may allow a particular routing mismatch between data and strobe lines on the motherboard. By routing with no mismatch between data and strobe lines on the motherboard, length may be gained in one or more segments.

Another option to change the solution space can be to change the board parameters. These parameters include trace width and space, impedance and variation, and/or dielectric thickness. All of these parameters may have an effect on the solution space which could allow the bus to be routed. Note that is has been shown that moving to a wider trace and space ratio has increased the segment length for the 3-load bus. The length gained to enable routing the bus comes at the cost of increased routing area required by the increased trace and space ratios.

Flight time and skew constraints as well as electrical characteristics set forth in the AGP specification must be followed when designing a logical point-to-point bus. The trace lengths, and allowable trace routing skew lengths may be different than in the case of a physical point-to-point bus, but the actual time allotted for flight time and signal skew must be the same in both cases.

It should be noted that not all implementations of a logical point-to-point bus will yield the same routing solution space. Issues that effect the trace length and routing mismatch allowed in a particular implementation include board impedance range, impedance variations due to crosstalk, and buffer characteristics for both the target (chipset) and master graphics controller down on the motherboard. Variations in all of these areas will yield different simulation results and thus different routing solution spaces. Because of this potential difference in each individual solution, each implementation of a point-to-point bus should be carefully simulated.

3.2.3.2 Data and strobe definitions

Throughout this document, the term "data" refers to AD[31:0], C/BE[3:0]# and SAB[7:0]. The term "strobe" refers to AD_STB[1:0] and SB_STB. When the term data is used it is referring to one of three groups of data as seen in Table 3-3. When the term strobe is used it is referring to one of the three strobes as it relates to the data in its associated group.

Table 3-3. Data and Associated Strobe

Data	Associated Strobe
AD[15:0] and C/BE[1:0]#	AD_STB0
AD[31:16] and C/BE[3:2]#	AD_STB1
SBA[7:0]	SB_STB

3.2.3.3 Assumptions for Board Design Guidelines

These guidelines are primarily for Accelerated Graphics Port (AGP) designs that use an Intel740 graphics controllers on a 82443BX motherboard and an AGP-compliant add-in card. They assume certain requirements in order to produce an AGP compliant placement and routing solution. These assumptions were used for the initial pre-route analysis of the design.

3.2.3.4 Add-in Card guideline assumptions:

Table 3-4. Data Signal and Strobe Guideline Assumptions

Width:Space	Zo	Trace	Line Length	Line Length Matching
1:2	50Ω to 85Ω	Data / Strobe	0.0in < line length < 3.0 in	Strobe ±0.5 in of group

All of the data line lengths within a group of signals needed to be within ±0.5 inches of their associated strobe. The board impedance needed to be in the range of 50Ω to 85Ω. This range is used to cover design targets and manufacturing tolerances.

Because crosstalk is a large component of skew, it was necessary to specify board routing. All traces needed to be routed with a separation of two times the trace width (6:12). Additionally, all lines within a group needed to be of the same type (microstrip or stripline). This is because microstrip (surface traces) and striplines (buried traces) have different propagation velocities, and mixing these can increase the flight time skew beyond acceptable limits. All the traces on the plugin card provided to us were routed as microstrip.

Table 3-5. Control and Clock Signal Guideline Assumptions

Trace	Width:Space	Line length
Control signals	1:2	0 < line length < 3.0
Clock	1:4	0.6ns ± 0.1ns *

* The clock trace on the add-in card shall be routed to achieve an interconnect delay of 0.6ns ± 0.1ns as determined from trace length and trace velocity.

3.2.3.5 Motherboard Guideline Assumptions

Data Signal and Strobe Requirements

Table 3-6. Data signal and strobe requirements

Width:Space	Zo	Trace	Line Length	Line Length Matching
1:2	50Ω to 80Ω	Data / Strobe	follow topologies	strobe longest signal of group

The motherboard needed to have an impedance range of 50Ω to 80Ω (as recommended by the 82443BX design guide). This range was used to cover design targets and manufacturing tolerances. The maximum line lengths are dependent on the type of trace and the amount of coupling.

The maximum line length was dependent on the routing rules used on the motherboard. These routing rules were created to give freedom for designs by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules assumed trace spacings of 1:2 (5:10 mils). Trace spacing refers to the distance between the traces as being the twice the width of the trace.

Longer lines have more crosstalk, therefore longer line lengths require a greater amount of spacing between traces to maintain skew timings

We assumed a 4 layer boardstackup as described earlier.

Control Signal and Clock Requirements

Table 3-7. Control Signal Line Length Requirements

Trace	Board	Width:Space	Line length
Control signals	Motherboard	1:2	Follow lengths and topology for the data and strobe signals.
Clock	Motherboard	1:4	Length determined by clock skew matching.

Some of the control signals require pull-up resistors to be installed on the motherboard. The stub to these pull-up resistors needs to be controlled. Stubs to pull-up resistors need to be kept as short as possible to avoid signal quality issues.

The clock lines on both the motherboard and the add-in card can couple with other traces. It is recommended that the clock spacing (air gap) be at least two times the trace width to any other traces. It is also strongly recommended that the clock spacing be at least four times the trace width to any strobes. The motherboard needs to be designed to the type of clock driver that is being used and motherboard trace topology.

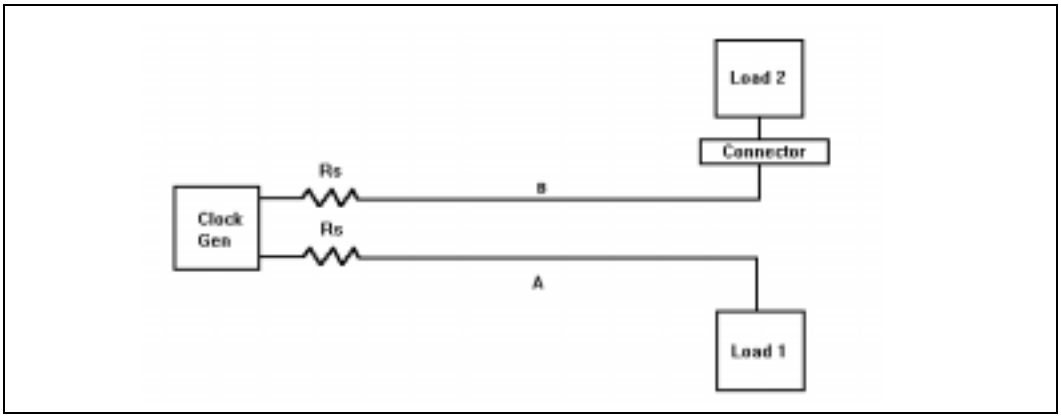
Clock Line Matching

Skew between each AGP master clock input and the AGP target (chipset) must be within the 1ns limit called out in the AGP specification. The driver use on this design can have up to 0.25ns of skew from output to output. This means that propagation delays and settling time skews cannot exceed 0.75 ns. Thus, for a single clock driver solution not only must each of the two clock trace segments be balanced in such a way that signal quality is acceptable, but the trace segments must be tuned in such a way as to meet the AGP specified skew requirements.

The clock topology used are shown in Figure 3-10.

Figure 3-10 shows the clock topology if three clock outputs are available. Each clock is a direct connection to it's respective load. Here the trace segments A and B must be balanced with respect to the target device clock trace in such a way as to meet system clock skew requirements.

Figure 3-10. Point-to-Point Topology



3.2.3.6 3-Load AGP Topology

Figure 3-11 and Figure 3-12 show the topologies for a 3-load AGP bus. The motherboard is divided into 2 trace segments as shown. These are referred to as segment A and B. The motherboard contains one AGP connector and one AGP master device. In the case of the strobe signals, a 3rd segment was added to represent the stub lengths of the pull up resistors. This segment is referred to as segment D. The net scheduling for this topology is segment A to connector, connector to segment B.

Figure 3-11. 3 Device Data Load Topology

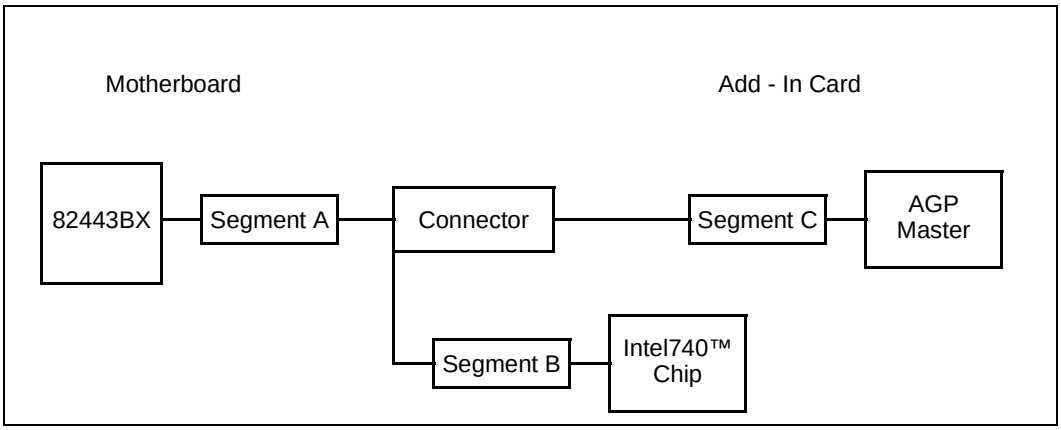
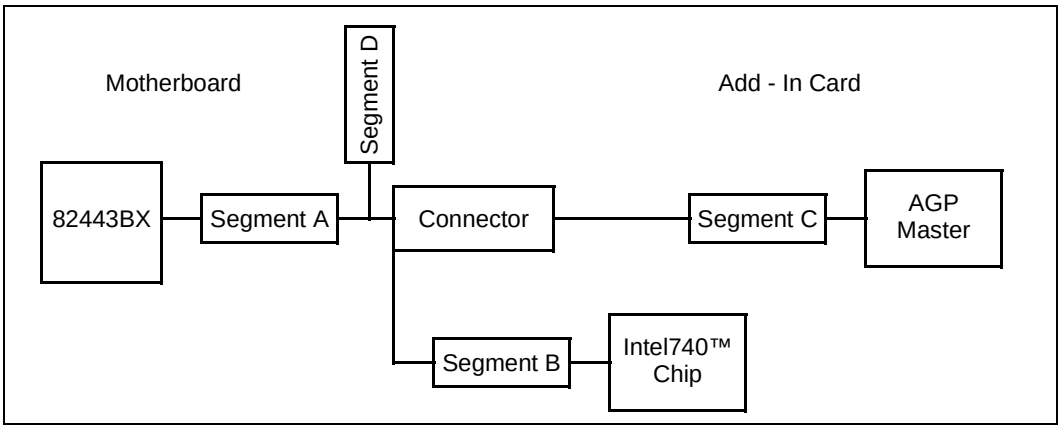


Figure 3-12. 3 Device Strobe Load Topology



3.2.3.7 Overall Solution Space

Two solution spaces were found. Selecting the appropriate solutions is dependent on the 82443BX placement relative to the AGP connector. Solution 1 was implemented on this design.

Table 3-8. Strobe and Data Segment Solution Space

Solution	segment A	Segment B	Segment D
solution 1	3.5” - 5.5” *	2.0” - 3.0”	0.4” - 0.9”

Solution 1. Note that A + B within a group must be matched by 0.5”. Example:

Assume: GAD1 segment A=4.1" segment B=2.7" (A+B=6.8") and GAD2 segment A=3.5" and segment B=3.0" (A+B=6.5"). Notice that GAD1 A and GAD2 have more than 0.5" difference, but A+B is only 0.3" difference. Also, the strobes should be the longest signal in the group.

Figure 3-13. 3 Device Data Load Topology (Solution 1 is Shown)

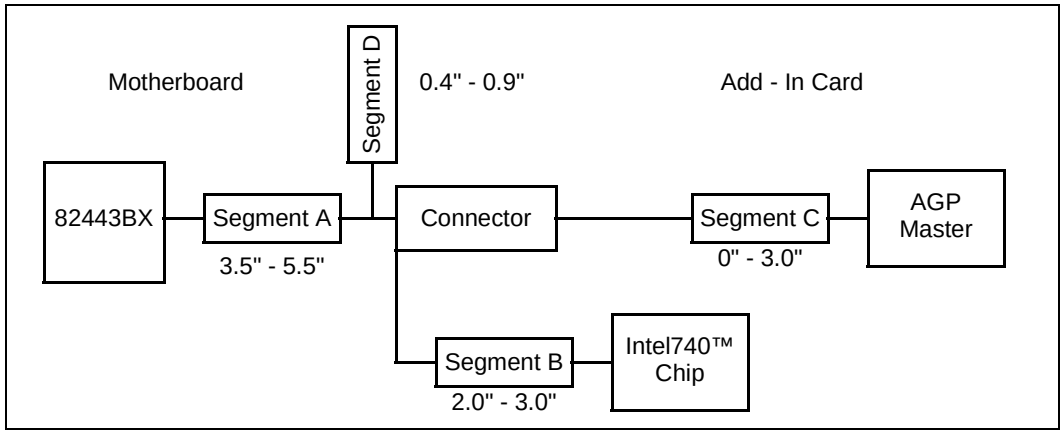
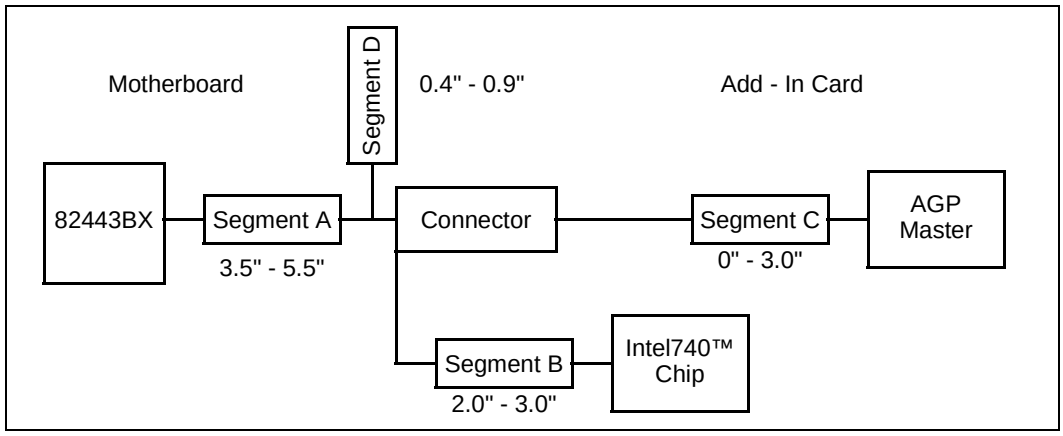


Figure 3-14. 3 Device Strobe Load Topology (Solution 1 is shown)



Clock Solutions

Figure 3-15. Clock Topology and Matching

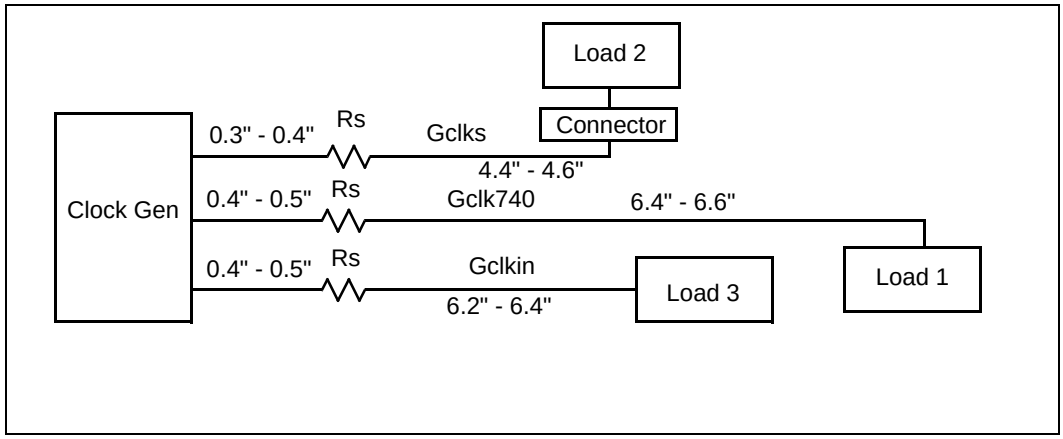


Table 3-9. Clock Segment Solution Space

Clock Net	Driver to resistor lengths	Resistor to Load lengths
Gclkin	0.4-0.5 Inches	6.2-6.4 Inches
Gclks	0.3-0.4 Inches	4.4-4.6 Inches
Gclk740	0.4-0.5 Inches	6.4-6.6 Inches

The clock lines were tuned as detailed in table Table 3-9 to ensure that no clock skew exceeding 0.75 ns occurred. Note that in the case of gclks, the load is the AGP connector.

3.2.4 Intel740™ Graphics Accelerator Memory Layout and Routing Guidelines

The Intel740 graphics accelerator integrates a memory controller that supports a 64-bit memory data interface. SGRAM can be used in addition to SDRAM, if it is configured to perform as an SDRAM. The Intel740 graphics accelerator generates the Row Address Strobe (SRAS[A:B]#), Chip Selects (CS0[A:B]#, CS1[A:B]#), Column Address Strobe (SCAS[A:B]#), Byte Enables (DQM[0:7]#), Write Enables (WE[A:B]#), and Memory Addresses (MA). The memory controller interface is fully configurable through a set of control registers.

Eleven memory address signals (MAx[10:0]) allow the Intel740™ graphics accelerator to support a variety of commercially available components. Two SRAS# lines permit two 64-bit wide rows of SDRAM. All write operations must be one Quadword (QWord). The Intel740 graphics accelerator supports memory up to 100 MHz.

Rules for populating a Intel740 graphics accelerator Memory:

- SDRAM and SGRAM components can be mixed.
- The DRAM Timing register, which provides the DRAM speed grade control for the entire memory array, must be programmed to use the timings of the slowest memories installed.

Possible DRAM and system options supported by the Intel740 graphics accelerator are shown in Table 3-10.

Table 3-10. Supported Memory Options (Other Memory Options Are Not Supported)

SDRAM/ SGRAM Technology	SDRAM/ SGRAM Density	SDRAM/ SGRAM Width	Addressing	Address Size		Local Memory Size	
				Row	Column	Min	Max
8 Mbit	256K	32	Asymmetric	10	8	2MB	4MB
16Mbit	512K	32	Asymmetric	11	8	4MB	8MB
16Mbit	1M	16	Asymmetric	12	8	8MB	8MB

There are several groups of signals within the memory bus with layout restrictions.

Table 3-11. Memory Layout Restrictions (See Figure 3-16 and Figure 3-17)

Signal	Intel740™ to SGRAM Stub		SGRAM Stub	
	Min	Max	Min	Max
MA[11:0]	.25”	4.9”	0.25"	0.6”
MD[63:0], DQM[7:0]	.25”	3.9”	0.25"	0.4”

Figure 3-16. Layout Dimensions (MA[11:0])

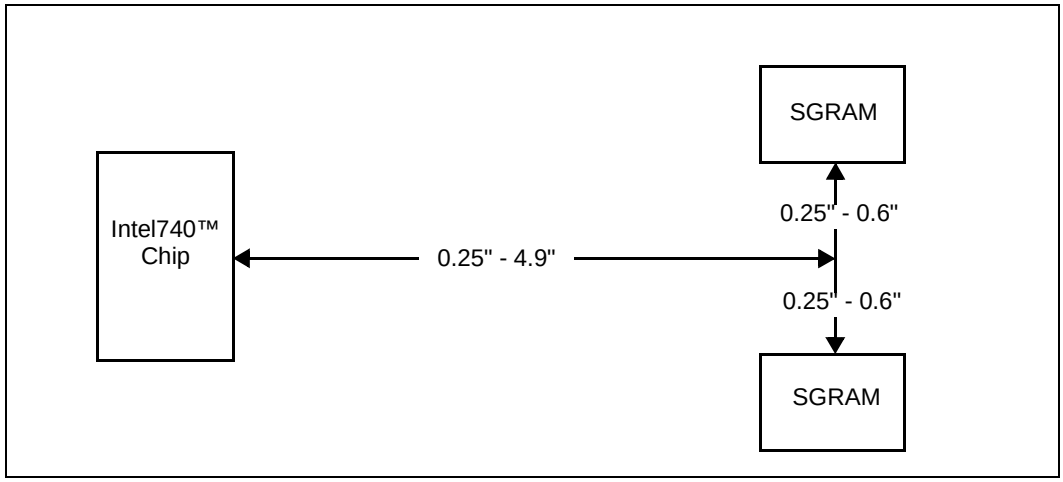


Figure 3-17. Layout Dimensions (MD[63:0], DQM[7:0])

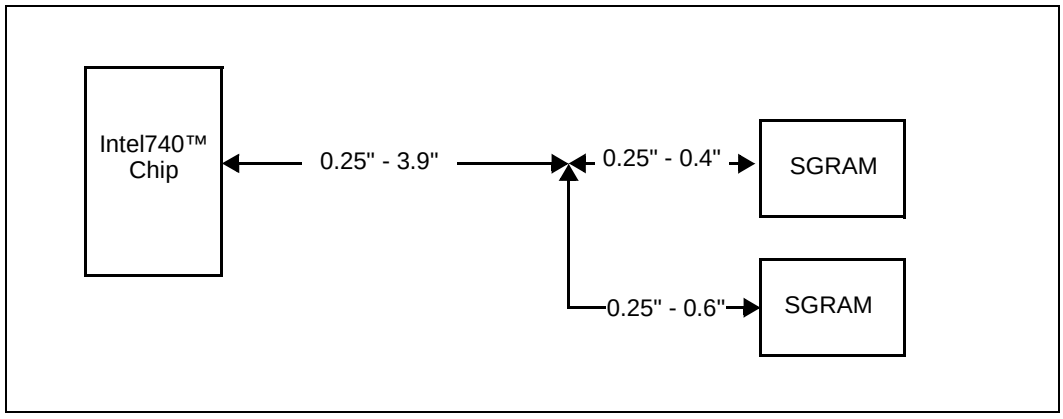


Table 3-12. Memory Layout Restrictions (See Table 3-16 and Table 3-17)

Signal	Intel740™ to SGRAM Stub		SGRAM Stub	
	Min	Max	Min	Max
WEA#, SRASA#, SCASA#, CSA0#	2.25’’	4.9”	0.25’’	0.6’’

Figure 3-18. Layout Dimensions (WEA#, SRASA#, SCASA#, CSA0#)

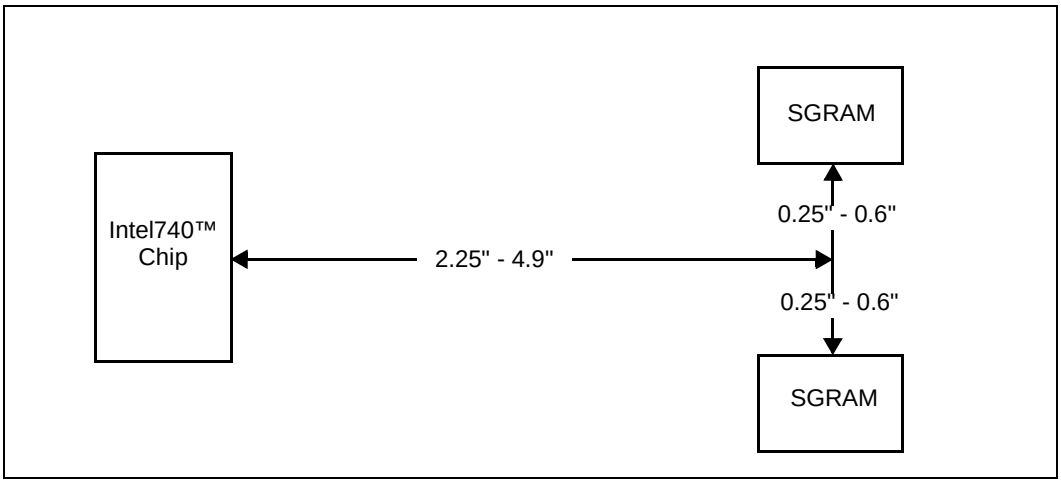


Table 3-13. Memory Layout Restrictions (See Figure 3-19)

Signal	Intel740™ to Resistor	Resistor to SGRAM Stub	SGRAM Stub	
			Min	Max
TCLK1	0.6”	3.4” ±0.25”	0.4”	0.6”

Figure 3-19. Memory Layout Dimensions (TCLK1)

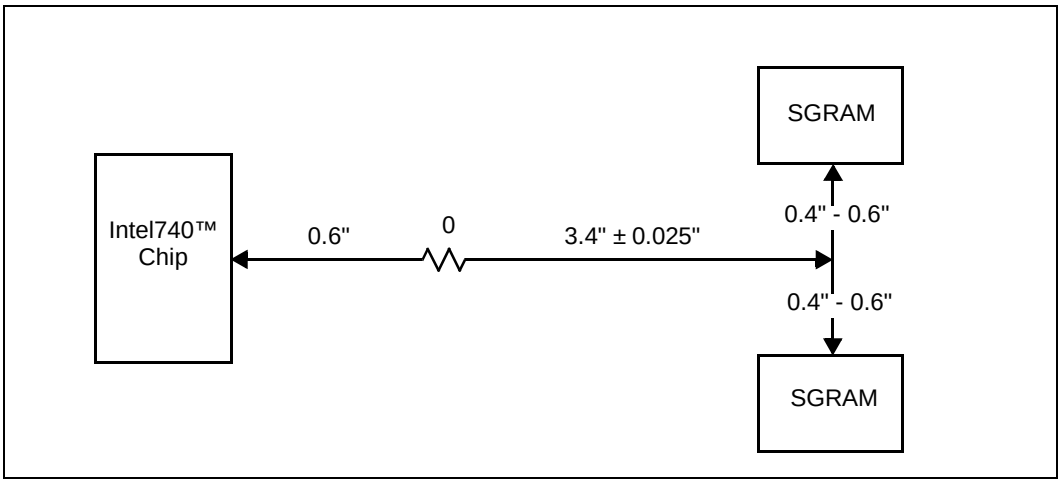
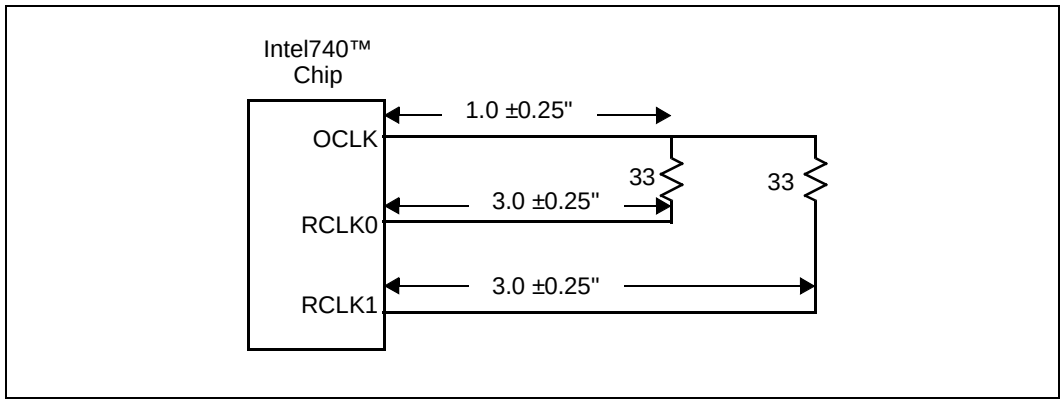


Table 3-14. Memory Layout Restrictions (See Figure 3-19)

Signal	Intel740™ to Resistor
OCLK to Resistor	1.0” ±0.25
RCLK0, RCLK1	3.0” ±0.25”

Note: It is important to match clock lengths. For example, if the length from OCLK to Resistor is 1.03, then the length from Resistor to RCLK should be 3.03 (OCLOCK to Resistor + 2’’).

Figure 3-20. Memory Layout Dimensions (RCLK and OCLK to RCLK)

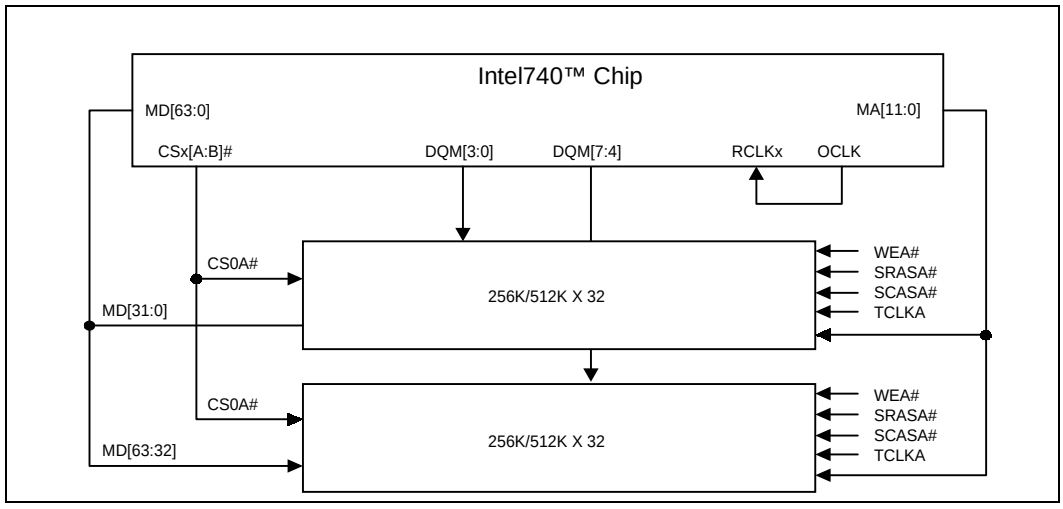


3.2.4.1 3 Device AGP Intel740™ Graphics Accelerator Memory Configurations

In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by an SRAS and the CS# signal.

Configuration #1: In this configuration, the minimum amount of memory (2MB) is supported. Note that, the same copy of all control signals goes to each component.

Figure 3-21. 2/4 MB Local Memory Connection (64-bit data path)



3.3 3 Device AGP Motherboard Reference Design Schematics

This section provides schematics for the 3-point AGP reference design. The description of each schematic page is named by the logic block shown on that page.

Cover Sheet **P-1**

The Cover Sheet shows the Schematic page titles, page numbers and disclaimers.

Block Diagram **P-2**

This page shows a block diagram overview of the Pentium® II / Intel® 440BX AGPset/ Intel® 740 system design. Also included are page numbers for every major component in the design.

Pentium® II Slot 1 processor connector (part 1) **P-3**

This page shows the first part of the DS1P connector (up to the key). SLP# connection comes directly from the PIIX4E. Intel recommends placing 0 ohm resistors on the EMI signals. A thermal sensor (the MAX 1617 ME) which connects to an internal processor diode has been included to monitor processor temperature.

Pentium® II Slot 1 processor connector (part 2) **P-4**

This page shows the remaining part DS1P connector. Also shown are the optional connections for overriding the VID pins from the processor.

Clock Synthesizer and ITP connector **P-5**

This page shows the new clock synthesizer component the CK100 plus recommended decoupling. The clock synthesizer components must meet all of the system bus, PCI and other system clock requirements. Several vendors offer components that can be used in this design.

This page also shows the In Target Probe (ITP) Connector. The ITP connector is recommended in order to use the In Target Probe tool available from Intel and other tool vendors for Pentium II processor based platform debug.

Note: Some logic analyzer vendors also support the use of the ITP connector. This connector is optional. **It is recommended to design these headers into the system for initial system debug and development, and leave the connector footprints unpopulated for production.**

82443BX Component (System bus and DRAM Interfaces)P-6

This page shows the 82443BX component, System bus and DRAM Interfaces. The 82443BX connects to the lower 32 bits of the CPU address bus and the CPU control signals, and generates DRAM control signals for the memory interface. In this design, the 82443BX is configured to interface to a memory array of 3 DIMMs.

The CKBF is also shown on this page. The 82443BX delivers a single SDRAM clock to the CKBF which is a 18 output buffer, with an I2C interface which may be used to disable unused clock outputs for EMI reduction. It outputs 4 clocks to each DIMM socket, and 1 back to the 82443BX for data timings.

82443BX Component (PCI and AGP Interfaces) P-7

This page shows the 82443BX component, PCI and AGP Interfaces. The definition of pin AF3 has been changed from SUSCLK to BX-PWROK. Like PIIX4E PWROK, it is connected to the PWROK logic from the Power Connector page (P-26). Note the GCLKIN and GCLKOUT trace length requirements on the AGP interface.

82443BX Component (Memory and System Data Bus Interfaces) P-8

This page shows the 82443BX component, Memory and System Data Bus Interfaces. GTL_REF signal are also shown on this page. Ideally, the GTL_REF signals should be decoupled separately, and as close as possible to the 82443BX component, but this is not a requirement.

DIMM Connectors 0, 1, 2 P- 9-11

These three pages show the DRAM interface connections from the 82443BX to the DRAM array.

The serial presence detect pins are addressed as 1010-000,001,010 respectively. The 82443BX strap pull-up/pull-downs will be located on selected MAB# lines. REGE (pin 147) on each DIMM socket should be pulled high to enable registered DIMMs,

PIIX4E Component P-12

This page shows the PIIX4E component. The PIIX4E component connects to the PCI bus, dual IDE connectors, and the ISA bus. This reference design supports a subset of the power management features of the PIIX4E.

PIIX4E Component P-13

This page shows the PIIX4E component Interrupts, USB, DMA, power management, X-Bus, and GPIO interfaces. Also shown is the CLOCKRUN# pull-down and the external logic needed to handle a power loss condition.

Ultra I/O Component P-14

This page shows the Ultra I/O component. The RTC may optionally be used. An Infra Red Header Port is also optional.

AGP Connector P-15

This page shows the AGP connector. In this design, AGP INTA and INTB are connected to the PCI INTA and INTB through a buffer/driver. The interrupt signals are open-collector, and pulled up to $V_{CC3.3.}$

PCI Connectors P-16/17

These pages show the PCI connectors. In this design, three PCI connectors are used. AD[26, 27, 29, 31] are the preferred lines for the PCI slot IDSELs.

ISA Connectors P-18

This page shows the ISA connectors.

PCI IDE Connectors P-19

This page shows the IDE Connectors. No special logic is required to support Ultra DMA/33 hard drives.

USB Headers **P-20**

This page shows the USB Headers. Note, the voltage divider on the open circuit signals provides logic level transitions for the PIIX4E. Note the placement requirements for the capacitors and series resistors at the bottom left.

Flash BIOS Component **P-21**

This page shows the 28F002BC-T Flash BIOS component which provides 128K bytes of BIOS memory. A jumper is used to provide the option for allowing the BIOS to be programmed in the system for BIOS upgrades and/or for programming plug and play information into the Flash device.

Note that a 2Meg Flash device may be required for certain applications (motherboard devices such as graphics, SCSI or LAN). An optional 34 pin header has been added to allow for BIOS emulation.

Parallel Port/ Serial and Floppy/ Keyboard & Mouse **P-23-25**

Nothing new here.

VRM **P-25**

The top of this page shows the voltage regulator modules (VRM 8.2) connector(s). The VRM 8.2 module provides 5V to VCCcore voltage conversion for the Pentium II processor. The bottom of this page shows two voltage regulators, one for generating the 1.5V GTL+ terminating voltage (V_{TT}), the other is a 2.5V regulator. The V_{TT} generation circuit must be able to provide about 5.0 amps of current under worst case conditions.

Note that the 5.0 amps of current will normally be supplied from two linear regulator devices (about 2.5 amps each), one located at each end of the GTL+ bus traces. However, one linear regulator device (such as the LT1585A-1.5 supplying the entire 5.0 amps) can be used if both ends of the GTL+ bus traces are near each other. For dual processors, two LT1587-1.5s (@ 3A) are recommended.

Power Connectors Front Panel Jumpers **P-26**

This page shows the system ATX power connector, hardware reset logic, and standard chassis connectors for the hard disk, power LEDs, and speaker output. New to this page are the dual-color LED circuit required to indicate the system state (either ON, OFF, or any of the suspend states), the 6-pin optional ATX connector, and the Wake-On-LAN header.

Note: A CPU Fan Header is required for the Intel Boxed Pentium II processor. The dual-color LED circuit is also used to reduce the voltage going to the power supply fan, thus decreasing its speed and quieting the system.

GTL+ Bus Termination Resistors **P-27**

This page shows the GTL+ bus termination resistors. The components shown are flat chip resistor array devices. These components are available in both four and eight resistors per package options. These packages have been chosen for their small size to reduce board space required. Discrete, SIP or SOJ resistor packages can also be used but will require more board area. Resistor packs with a corner power pin are not recommended. A decoupling cap per resistor pack is also recommended. Each GTL+ signal that connects between the 82443BX and the Slot 1 must be dual terminated to insure proper GTL+ signaling. Each GTL+ signal should be routed using a daisy chain methodology as described in the GTL+ layout guidelines section of this document. The termination resistors for each net must be located at the ends of the nets. Connect the V_{TT} side of the resistor

packs to as short of a trace as possible before routing to the V_{TT} plane. If the V_{TT} plane is on an inner layer, keep the trace distance to the via as short as possible by placing the via between pins 6 and 7 for each resistor package. Where this is not possible, use multiple vias to the V_{TT} plane for each group of 4 signals. Refer to the GTL+ Specification for more complete details on GTL+ signaling.

Pull-up and Pull-down Resistors **P-28/29**

These pages show pull-up and pull-down resistors for PCI signals, PIIX4E, Slot 1(CMOS), ISA, and AGP signals. Also shown are spare gates.

Decoupling Capacitors **P-30/31**

Decoupling Caps **P-32**

These pages show de-coupling capacitance used in the schematics as well as the voltage dividers used to provide the GTL reference voltage.

Hardware system manager **P-33**

The LM79 is a hardware system monitor. It monitors voltage regulation, fan RPM and stores POST codes. The device can be accessed via the X-Bus bus or through the PIIX4E SMBus interface. Note the voltage level translation circuitry between the 5-Volt LM79 and the rest of the 3.3-Volt SMBus.

Intel740™ Graphics Accelerator **P-34/35**

This page shows all of the connections to the Intel740 graphics accelerator. Each Intel740 graphics accelerator interface is hooked up in this reference design. Beginning in the upper left hand corner of the page, the video capture port is shown. Internally, the input pins are pulled down. These pins contain a strapping option for subsystem ID. In this case, the reference design has an ID of 0100h. Bits that should be a “1” may be pulled up using a 2K pull-up resistor. Since this graphics design will not have video, the only concern is pulling the bus up to the correct value for the subsystem ID. The video control signals may be left unconnected. The BIOS interface contains the vendor ID. The section labeled AGP interface connects directly to the AGP connector. The memory interfaces connect to memory components. Decoupling for the Intel740 graphics accelerator is shown in the middle of the schematic page.

VGA Connector **P-36**

The VGA connector provides the RGB output to a monitor. BIOS and hardware provide support for plug-and-play capability.

SGRAMS **P-37**

The SGRAMs shown on this page are labeled as 512Kx32. The schematic pinout is actually capable of supporting either the 512Kx32 or 256Kx32 SGRAMs. This dual-support connection is achieved through the following method. The 512Kx32 Jedec standard defines AP on pin 51 which is address 9. BS is on pin 29 and is also labeled as address 10. Address 8 is on pin 30. The Intel740 contains the AP on its address 8 pin and BS on address 9 pin. Since the 256Kx32 has AP with graphics accelerator address 8 and on pin 51 along with BS with address 9 on pin 29 and a no connect on pin 30, either the 512K or the 256K SGRAMs are capable of being supported in the same design (see Figure 3-22).

Note: It is important to disable the special features of SGRAM. This will make the SGRAM operate as an SDRAM; thus, making it compatible with the Intel740 graphics accelerator.

Figure 3-22. 512Kx32 and 256Kx32 Pinout Compatibility

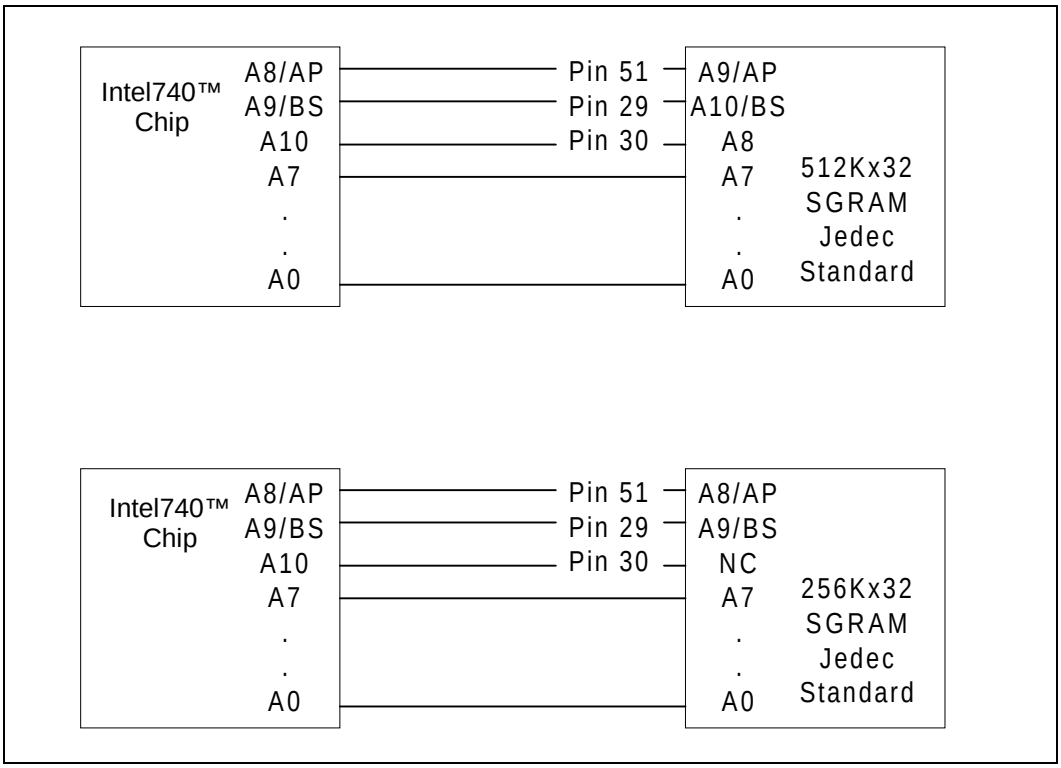
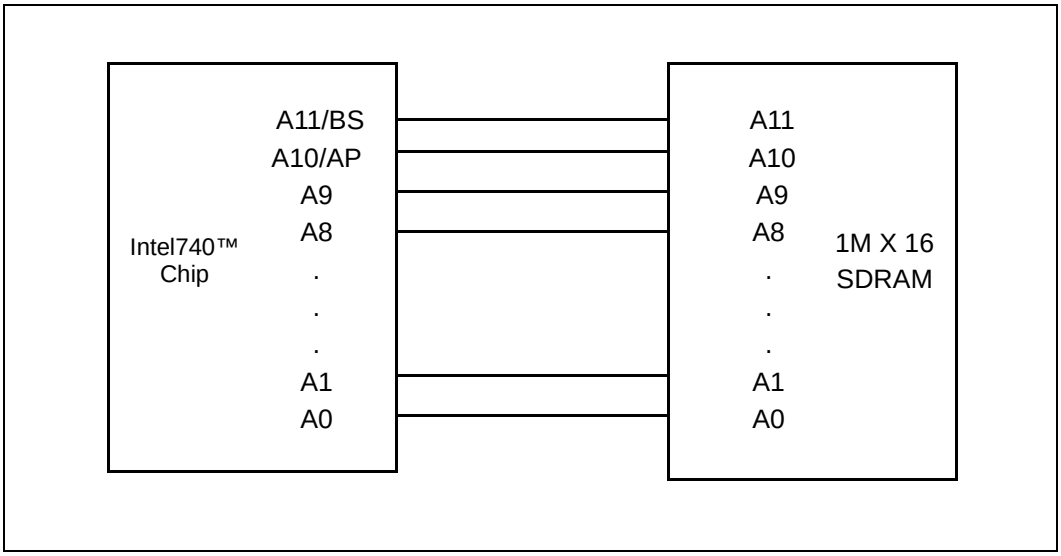


Figure 3-23. 1M X 16 Pinout Compatibility



Low Power Logic **P-38**

This page show the logic needed to put the Intel 740 graphics accelerator into a low power state when a video add-in card is installed into the system. In low power mode, the Intel 740 chip is disabled and will not initiate or respond to cycles on the AGP bus.

DDC/I^{2}C **P-39**

This page details the 3.3 volt/5 volt signal conversion as well as the DDC/I^{2}C connections. To perform the voltage translation, quick switches are used.

Voltage Regulator **P-40**

This page shows the circuitry to convert from 3.3 Volts to 2.7 Volts. The regulator used in the reference design does not need any heatsink for the FET. As shown, the FET will be dissipating slightly over 1 watt. If a different voltage regulator solution will be used, calculations will be needed to determine the need for a heatsink. Core decoupling is shown at the bottom of the page and should be placed close to the Intel740 graphics accelerator.

Revision History **P-41**

Changes made to the schematics are listed here underneath the revision where they first appeared and by page number.

3 Device AGP Refrence Schematics

Revision 1.0

**** Please note that these schematics are subject to change.**

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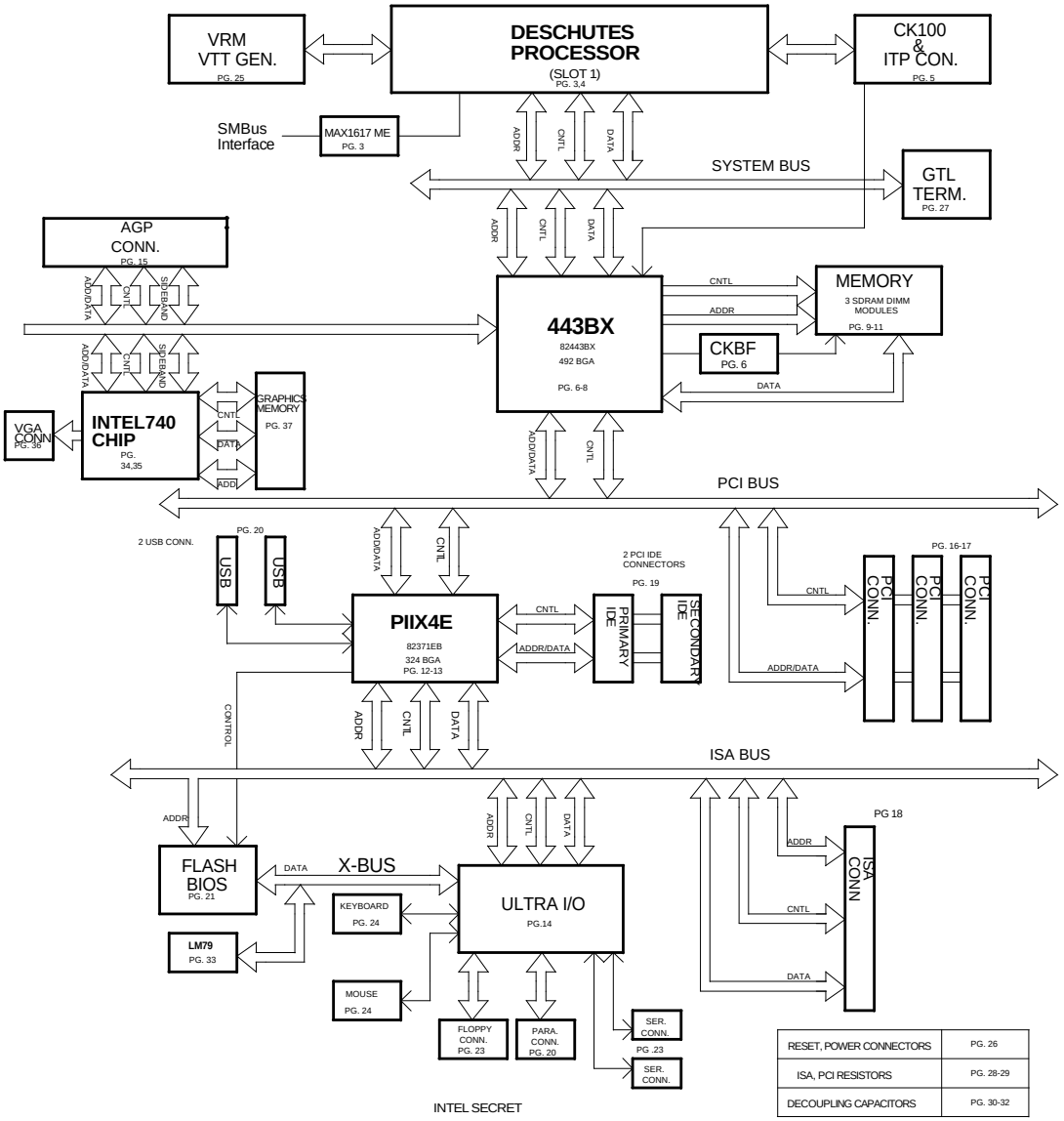
Date: 22:16:57	Sheet 1 of 41	



RESET, POWER CONNECTORS	PG. 26
ISA, PCI RESISTORS	PG. 28-29
DECOUPLING CAPACITORS	PG. 30-32

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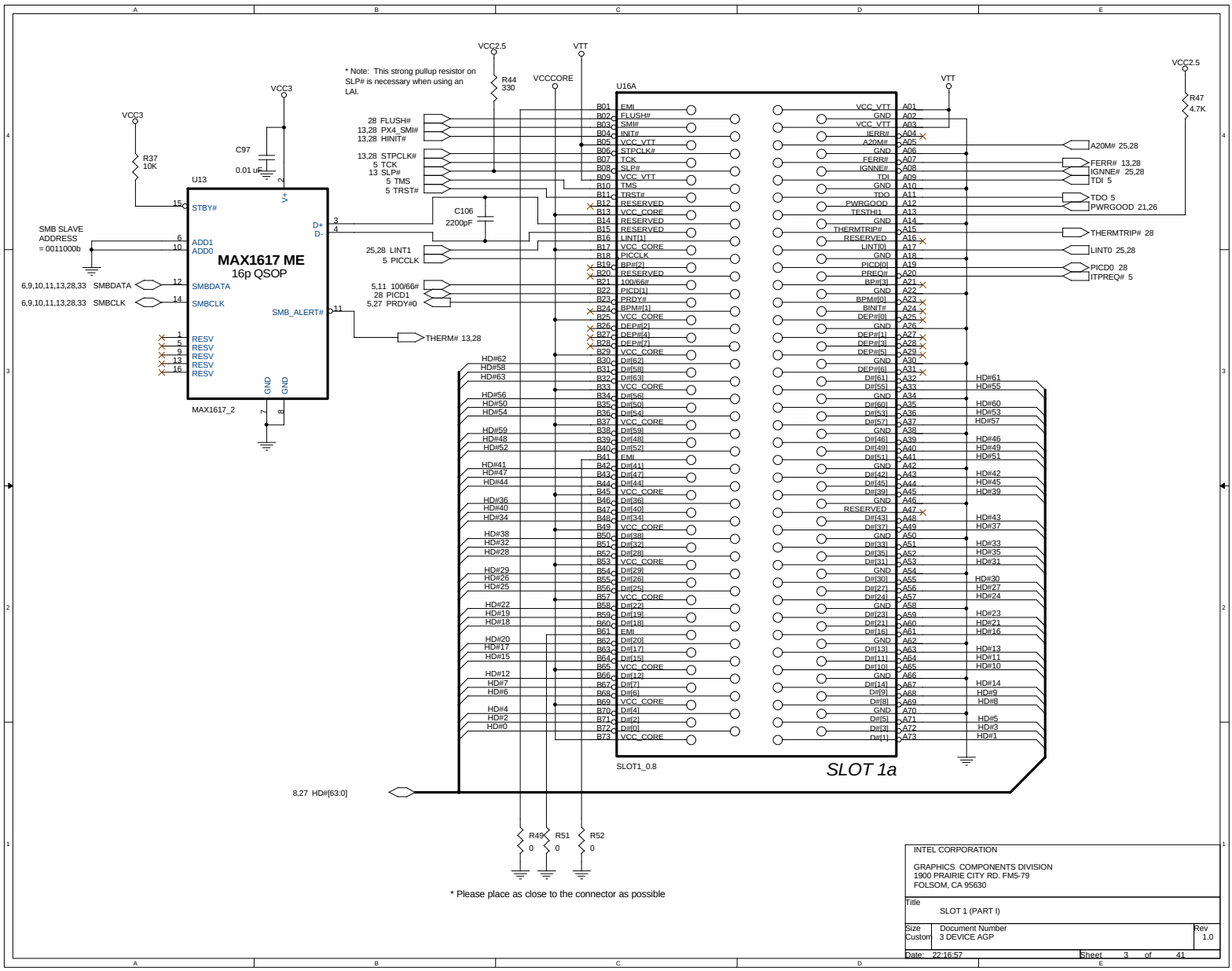

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Title	SLOT 1 (PART I)
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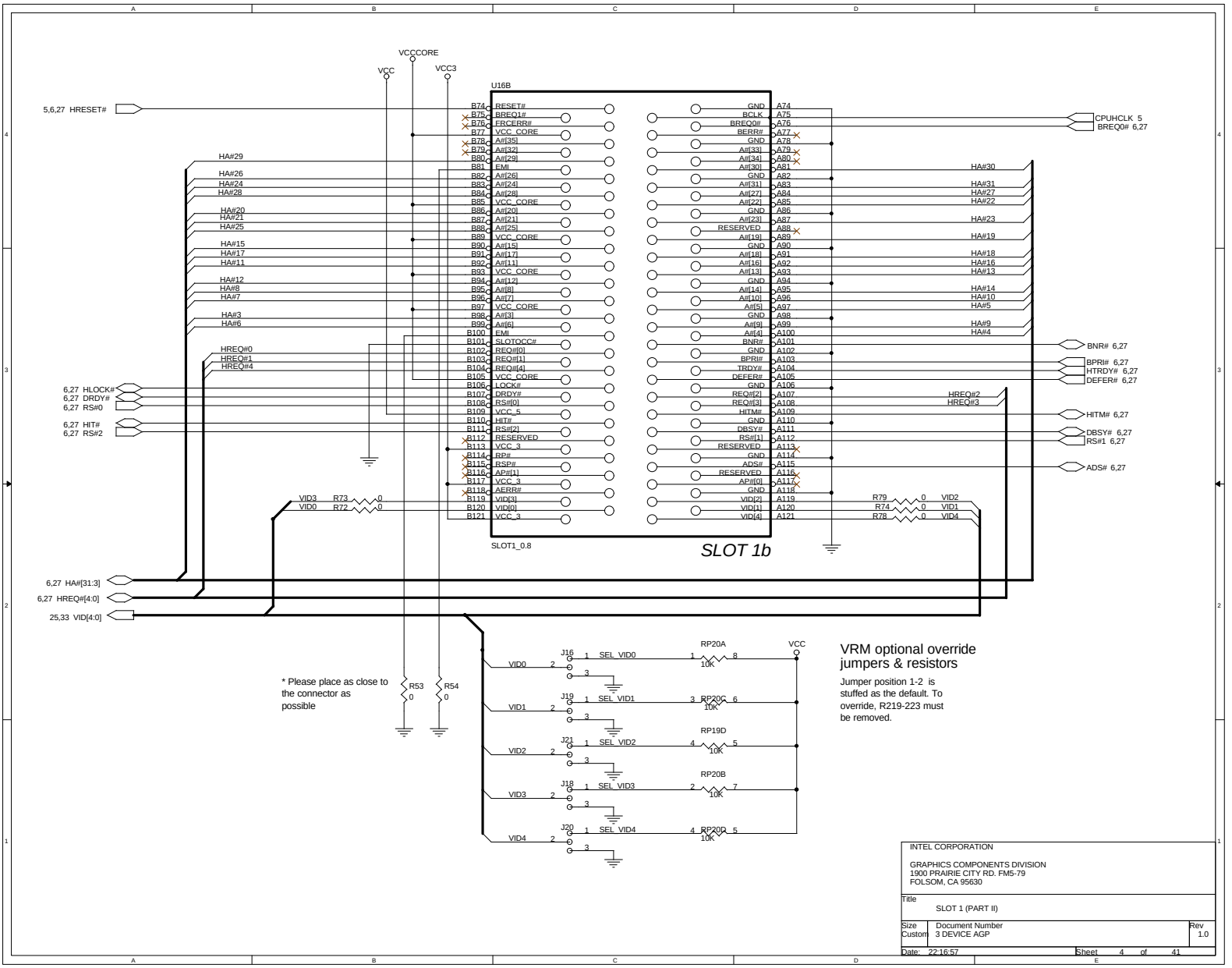

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Title: SLOT 1 (PART II)

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Custom	3 DEVICE AGP	1.0

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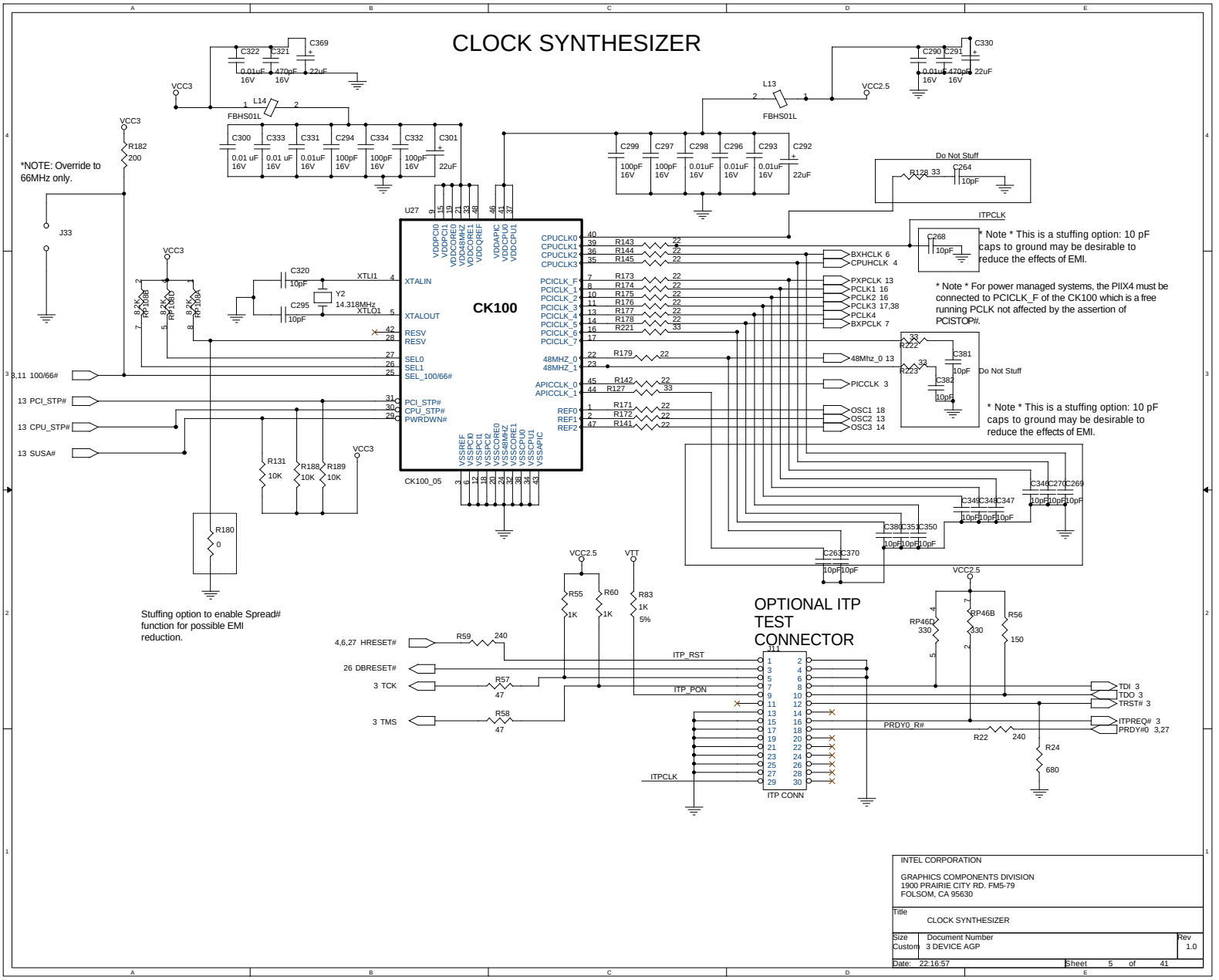
CLOCK SYNTHESIZER



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Title	CLOCK SYNTHESIZER
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Rev: 1.0	
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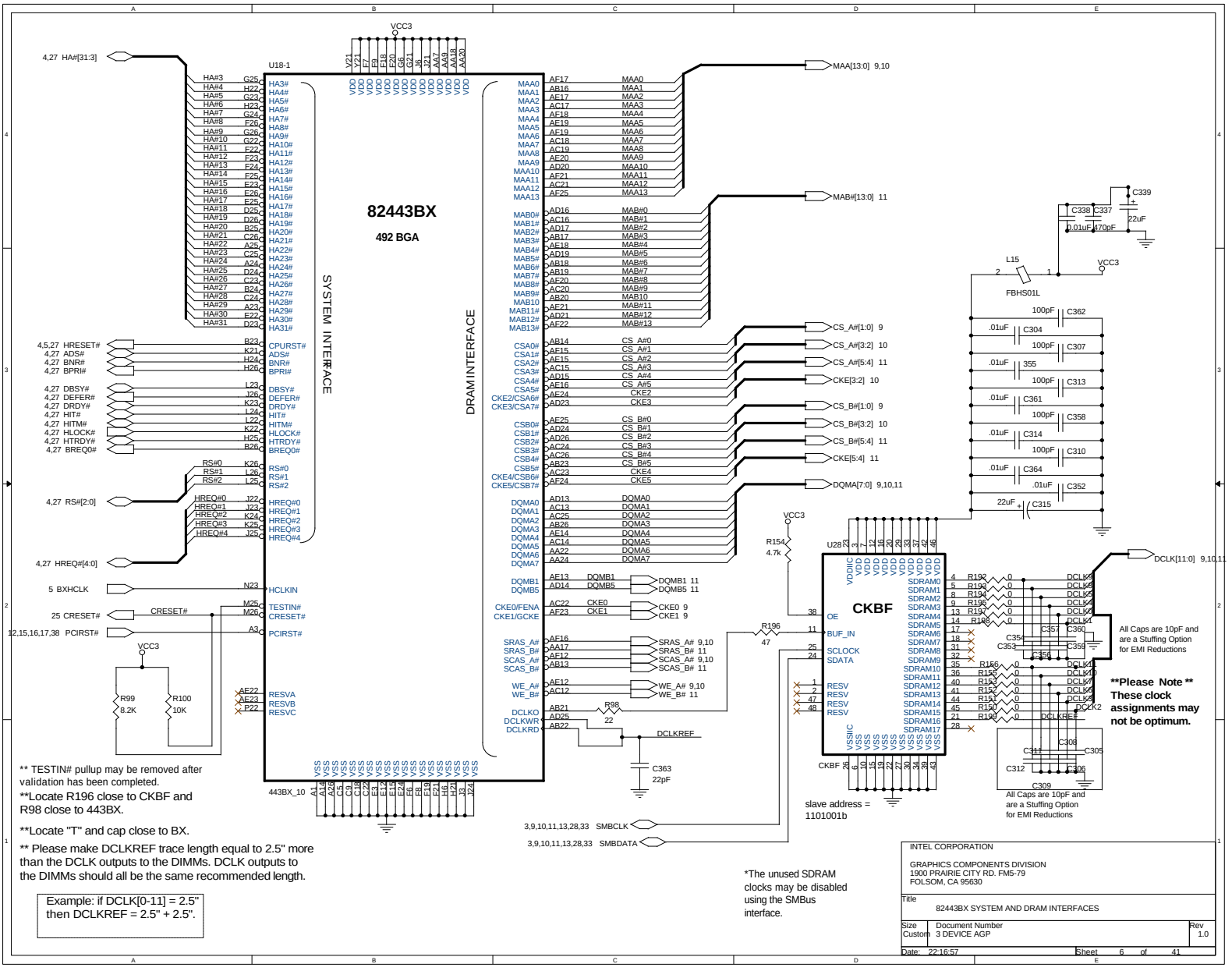
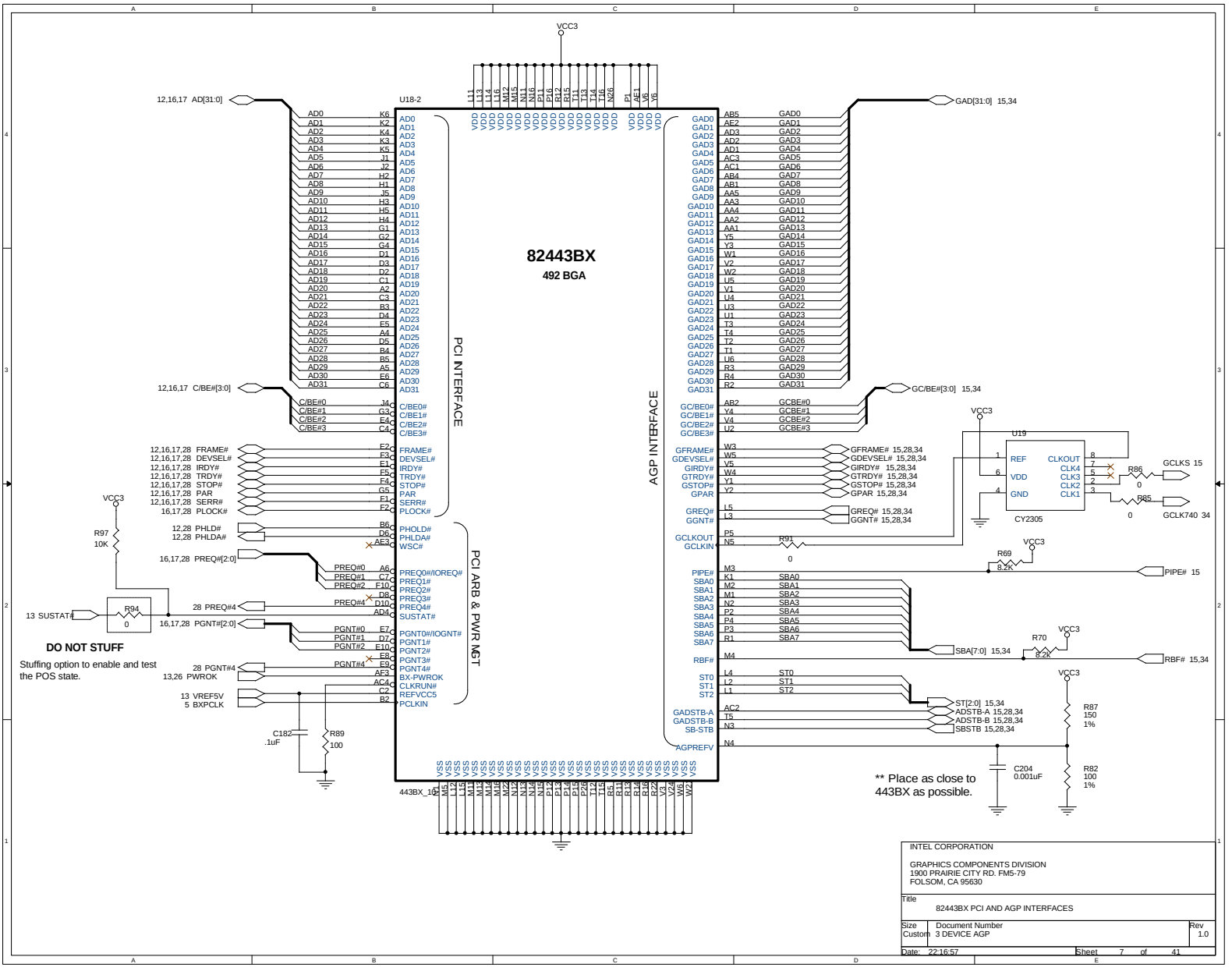
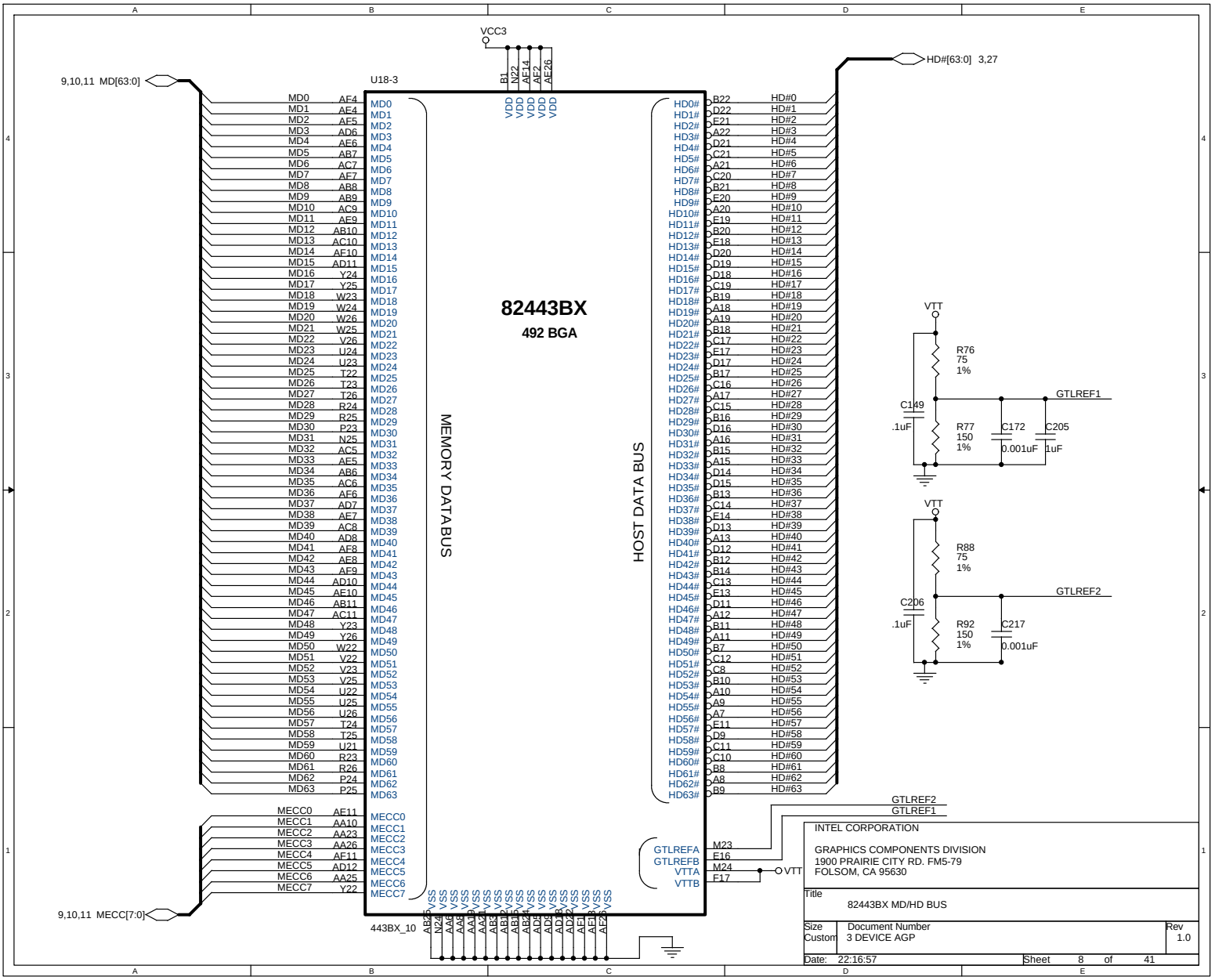

82443BX
492 BGA
U18-1
SYSTEM INTERFACE
DRAM INTERFACE
443BX_10
4,27 HA#[31:3]
MAA[13:0] 9,10
MAB#[13:0] 11
CS_A#[1:0] 9
CS_A#[3:2] 10
CS_A#[5:4] 11
CKE[3:2] 10
CS_B#[1:0] 9
CS_B#[3:2] 10
CS_B#[5:4] 11
CKE[5:4] 11
DQMA[7:0] 9,10,11
4,5,27 HRESET#
4,27 ADS#
4,27 BNR#
4,27 BPRI#
4,27 DBSY#
4,27 DEFER#
4,27 DRDY#
4,27 HIT#
4,27 HITM#
4,27 HLOCK#
4,27 HTRDY#
4,27 BREQ0#
4,27 RS#[2:0]
4,27 HREQ#[4:0]
5 BXHCLK
25 CRESET#
12,15,16,17,38 PCIRST#
VCC3
R99 8.2K
R100 10K
** TESTIN# pullup may be removed after validation has been completed.
**Locate R196 close to CKBF and R98 close to 443BX.
**Locate "T" and cap close to BX.
** Please make DCLKREF trace length equal to 2.5" more than the DCLK outputs to the DIMMs. DCLK outputs to the DIMMs should all be the same recommended length.
Example: if DCLK[0-11] = 2.5" then DCLKREF = 2.5" + 2.5".
R98 22
DCLKREF
C363 22pF
R154 4.7k
R196 47
U28
CKBF
slave address = 1101001b
3,9,10,11,13,28,33 SMBCLK
3,9,10,11,13,28,33 SMBDATA
*The unused SDRAM clocks may be disabled using the SMBus interface.
L15 FBHS01L
C339 C338 C337 22uF 0.01uF 470pF
C362 C304 C307 C313 C361 C358 C314 C310 C364 C352 C315
100pF .01uF 355 22uF
DCLK[11:0] 9,10,11
DCLKREF
All Caps are 10pF and are a Stuffing Option for EMI Reductions
**Please Note ** These clock assignments may not be optimum.
C354 C357 C360 C353 C356 C359 C355 C358 C308 C311 C305 C312 C306 C309
All Caps are 10pF and are a Stuffing Option for EMI Reductions
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
82443BX SYSTEM AND DRAM INTERFACES
Size Custom
Document Number 3 DEVICE AGP
Rev 1.0
Date: 22:16:57
Sheet 6 of 41



INTEL CORPORATION	
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title	82443BX PCI AND AGP INTERFACES
Size: Custom	Document Number: 3 DEVICE AGP
Rev: 1.0	
Date: 22:16:57	Sheet 7 of 41


VCC3
9,10,11 MD[63:0]
U18-3
HD#[63:0] 3,27
82443BX
492 BGA
MEMORY DATA BUS
HOST DATA BUS
9,10,11 MECC[7:0]
443BX_10
VTT
R76
75
1%
C149
.1uF
R77
150
1%
C172
0.001uF
C205
1uF
GTLREF1
R88
75
1%
C206
.1uF
R92
150
1%
C217
0.001uF
GTLREF2
GTLREF1
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
82443BX MD/HD BUS
Size
Custom
Document Number
3 DEVICE AGP
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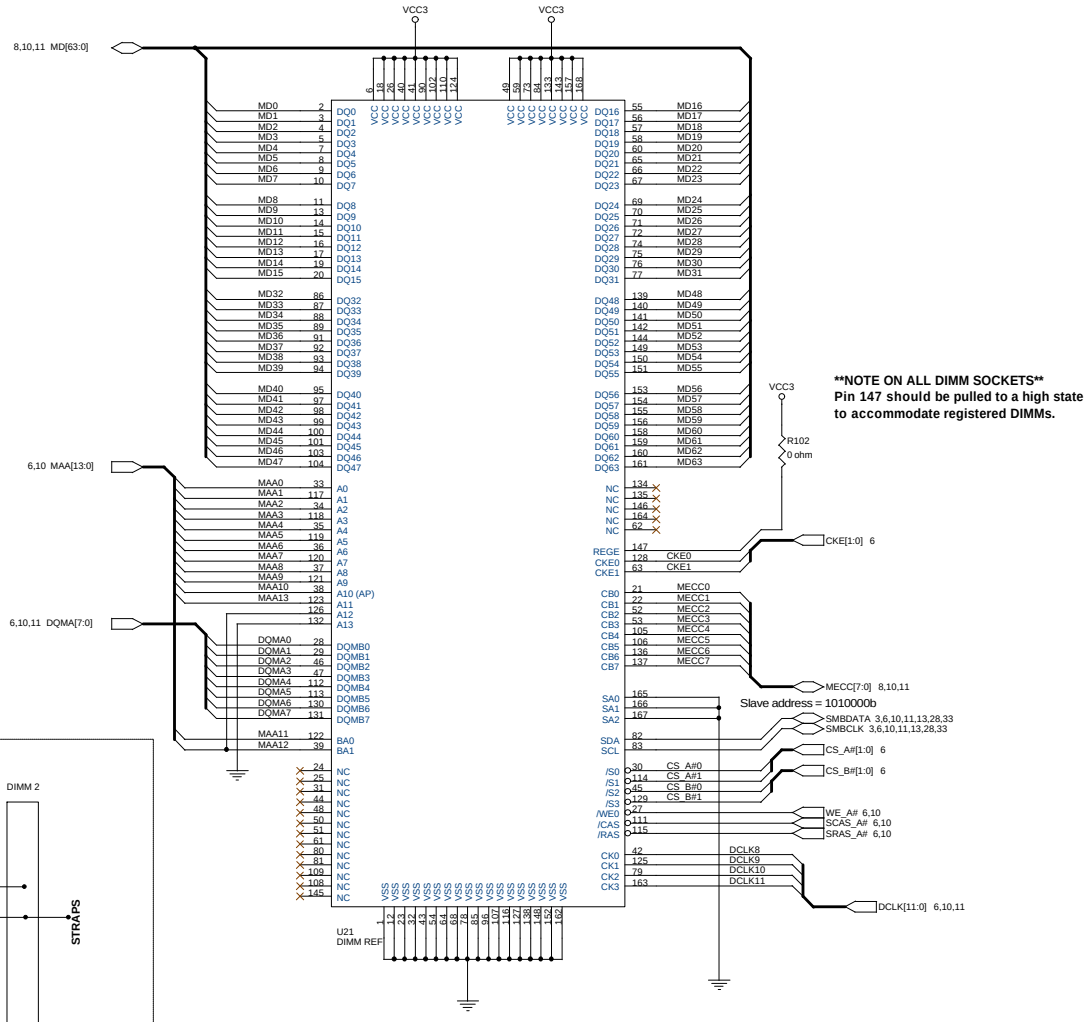
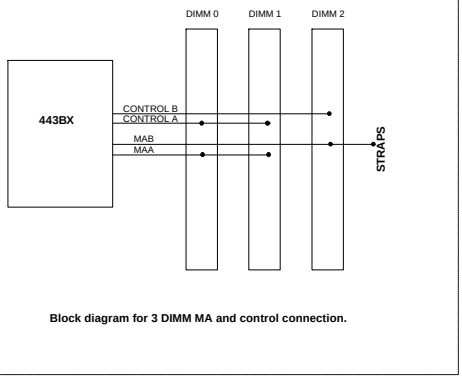
DIMM SOCKET 0



****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.



Block diagram for 3 DIMM MA and control connection.

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Title: DIMM SOCKET 0		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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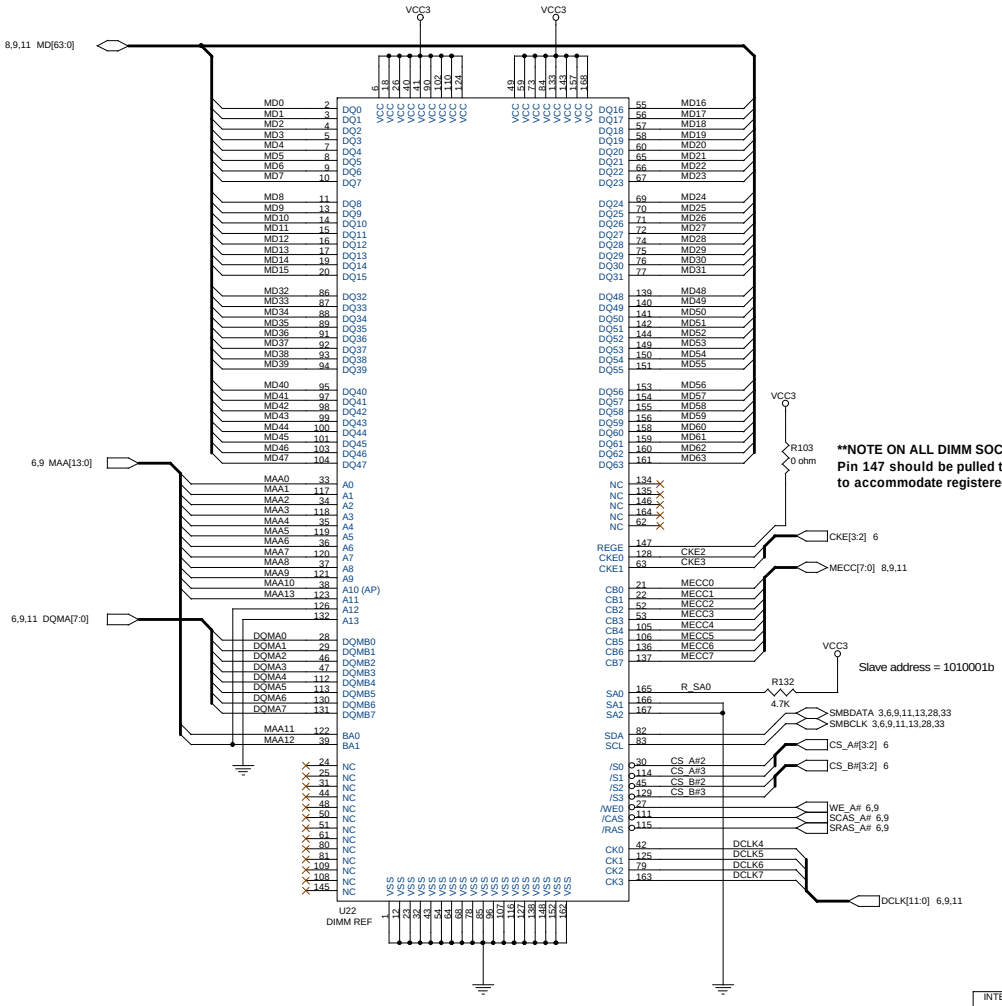
DIMM SOCKET 1



INTEL CORPORATION	
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title	DIMM SOCKET 1
Size: Custom	Document Number: 3 DEVICE AGP
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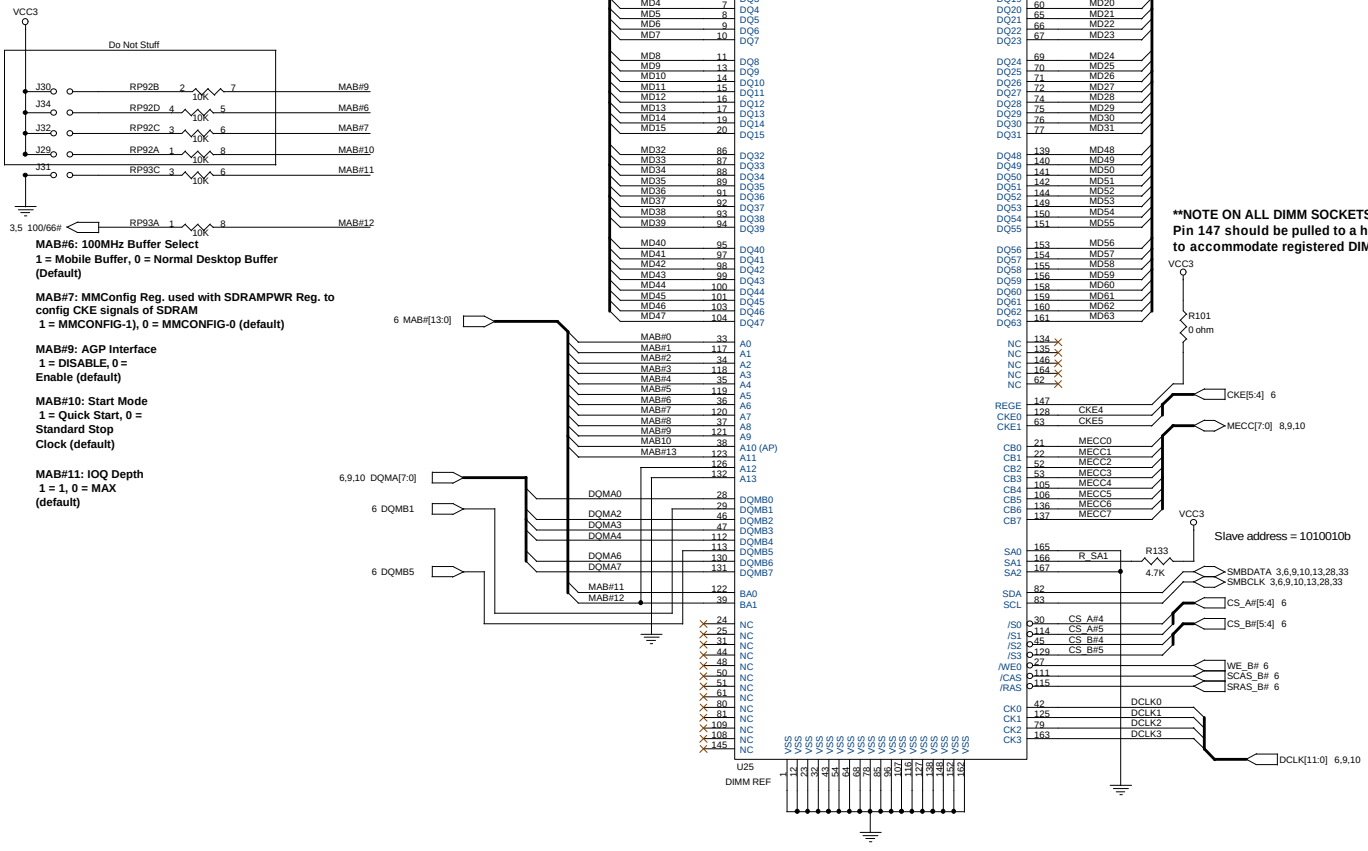
DIMM SOCKET 2



MAB#6: 100MHz Buffer Select
1 = Mobile Buffer, 0 = Normal Desktop Buffer (Default)

MAB#7: MMConfig Reg. used with SDRAMPWR Reg. to config CKE signals of SDRAM
1 = MMCONFIG-1), 0 = MMCONFIG-0 (default)

MAB#9: AGP Interface
1 = DISABLE, 0 = Enable (default)

MAB#10: Start Mode
1 = Quick Start, 0 = Standard Stop Clock (default)

MAB#11: IOQ Depth
1 = 1, 0 = MAX (default)

****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

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Title	DIMM SOCKET 2
Size: Custom	Document Number: 3 DEVICE AGP
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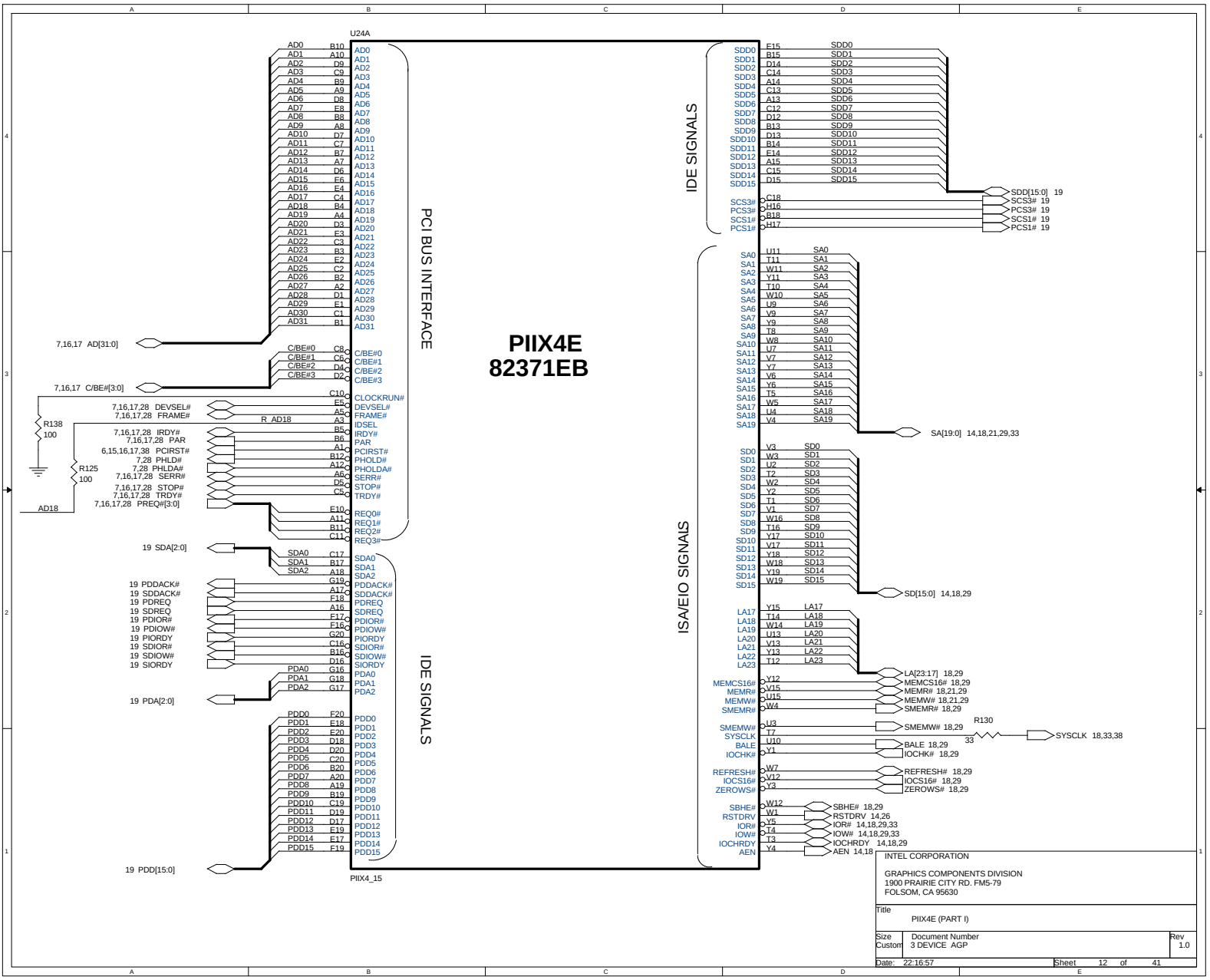
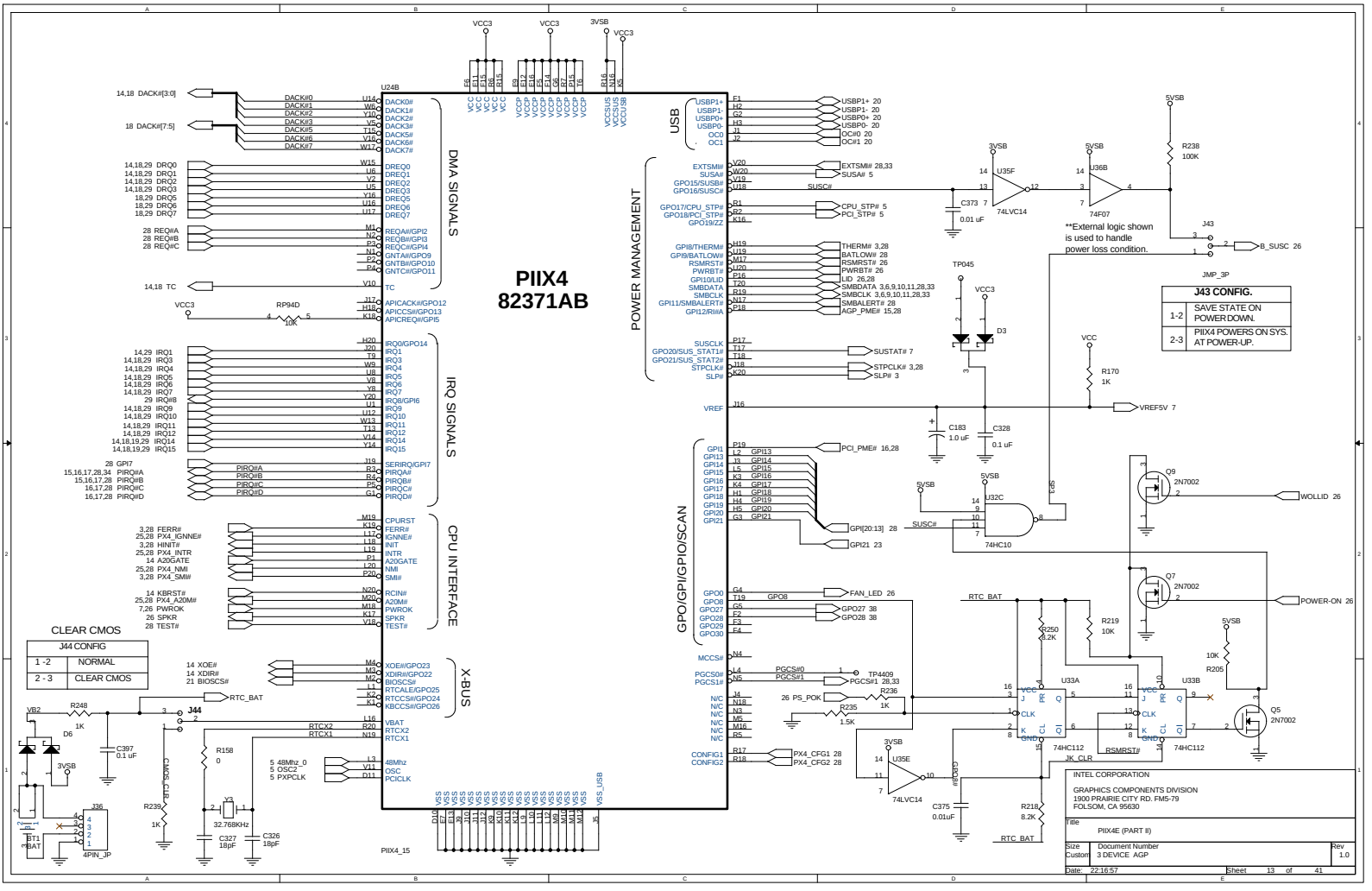
Date: 22:16:57	Sheet 11 of 41


U24A
PIIX4E
82371EB
PCI BUS INTERFACE
IDE SIGNALS
ISA/EIO SIGNALS
IDE SIGNALS
PIIX4_15
7,16,17 AD[31:0]
7,16,17 C/BE#[3:0]
7,16,17,28 DEVSEL#
7,16,17,28 FRAME#
7,16,17,28 IRDY#
7,16,17,28 PAR
6,15,16,17,38 PCIRST#
7,28 PHLD#
7,28 PHLDA#
7,16,17,28 SERR#
7,16,17,28 STOP#
7,16,17,28 TRDY#
7,16,17,28 PREQ#[3:0]
R_AD18
AD18
R138
100
R125
100
19 SDA[2:0]
19 PDDACK#
19 SDDACK#
19 PDREQ
19 SDREQ
19 PDIOR#
19 PDIOW#
19 PIORDY
19 SDIOR#
19 SDIOW#
19 SIORDY
19 PDA[2:0]
19 PDD[15:0]
SA[19:0] 14,18,21,29,33
SD[15:0] 14,18,29
LA[23:17] 18,29
MEMCS16# 18,29
MEMR# 18,21,29
MEMW# 18,21,29
SMEMR# 18,29
SMEMW# 18,29
R130
33
SYSCLK 18,33,38
BALE 18,29
IOCHK# 18,29
REFRESH# 18,29
IOCS16# 18,29
ZEROWS# 18,29
SBHE# 18,29
RSTDRV 14,26
IOR# 14,18,29,33
IOW# 14,18,29,33
IOCHRDY 14,18,29
AEN 14,18
SDD[15:0] 19
SCS3# 19
PCS3# 19
SCS1# 19
PCS1# 19
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
PIIX4E (PART I)
Size
Custom
Document Number
3 DEVICE AGP
Rev
1.0
Date: 22:16:57
Sheet 12 of 41


PIIX4
82371AB
U24B
DMA SIGNALS
IRQ SIGNALS
CPU INTERFACE
X-BUS
USB
POWER MANAGEMENT
GPO/GPI/GPIO/SCAN
DACK#0 DACK#1 DACK#2 DACK#3 DACK#5 DACK#6 DACK#7
DREQ0 DREQ1 DREQ2 DREQ3 DREQ5 DREQ6 DREQ7
REQA#/GPI2 REQB#/GPI3 REQC#/GPI4 GNTA#/GPO9 GNTB#/GPO10 GNTC#/GPO11
TC
APICACK#/GPO12 APICCS#/GPO13 APICREQ#/GPI5
IRQ0/GPO14 IRQ1 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ8/GPI6 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15
SERIRQ/GPI7 PIRQ#A PIRQ#B PIRQ#C PIRQ#D
CPURST FERR# IGNNE# INIT# INTR A20GATE NMI SMI#
RCIN# A20M# PWROK SPKR TEST#
XOE#/GPO23 XDIR#/GPO22 BIOSCS# RTCALE/GPO25 RTCCS#/GPO24 KBCCS#/GPO26
VBAT RTCX2 RTCX1
48Mhz OSC PCICLK
USBP1+ USBP1- USBP0+ USBP0- OC0 OC1
EXTSMI# SUSA# GPO15/SUSB# GPO16/SUSC#
GPO17/CPU_STP# GPO18/PCI_STP# GPO19/ZZ
GPI8/THERM# GPI9/BATLOW# RSMRST# PWRBT# GPI10/LID SMBDATA SMBCLK GPI11/SMBALERT# GPI12/RI#A
SUSCLK GPO20/SUS_STAT1# GPO21/SUS_STAT2# STPCLK# SLP#
VREF
GPI1 GPI13 GPI14 GPI15 GPI16 GPI17 GPI18 GPI19 GPI20 GPI21
GPO0 GPO6 GPO27 GPO28 GPO29 GPO30
MCCS#
PGCS0# PGCS1#
N/C
CONFIG1 CONFIG2
VCC3 3VSB 5VSB
VCCP VCCSUS VCCUSB
VSS VSS_USB
PIIX4_15
J44 CONFIG
1 -2 NORMAL
2 - 3 CLEAR CMOS
CLEAR CMOS
RTC_BAT
VB2 R248 1K D6 C397 0.1 uF
3VSB
J36 4PIN_JP
BT1 mBAT
R158 0
R239 1K
CMOS CLR
Y3 32.768KHz
C327 18pF
C326 18pF
RTCX2 RTCX1
5 48Mhz_0
5 OSCZ
5 PXPCLK
14,18 DACK#[3:0]
18 DACK#[7:5]
14,18,29 DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7
28 REQ#A 28 REQ#B 28 REQ#C
14,18 TC
RP94D 10K
14,29 IRQ1 14,18,29 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 29 IRQ#8 14,18,29 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 14,18,19,29 IRQ15
28 GPI7 15,16,17,28,34 PIRQ#A 15,16,17,28 PIRQ#B 16,17,28 PIRQ#C 16,17,28 PIRQ#D
3,28 FERR# 25,28 PX4_IGNNE# 3,28 HINIT# 25,28 PX4_INTR 14 A20GATE 25,28 PX4_NMI 3,28 PX4_SMI#
14 KBRST# 25,28 PX4_A20M# 7,28 PWROK 26 SPKR 28 TEST#
14 XOE# 14 XDIR# 21 BIOSCS#
USBP1+ 20 USBP1- 20 USBP0+ 20 USBP0- 20 OC#0 20 OC#1 20
EXTSMI# 28,33 SUSA# 5
CPU_STP# 5 PCI_STP# 5
THERM# 3,28 BATLOW# 28 RSMRST# 26 PWRBT# 26 LID 26,28 SMBDATA 3,6,9,10,11,28,33 SMBCLK 3,6,9,10,11,28,33 SMBALERT# 28 AGP_PME# 15,28
SUSTAT# 7 STPCLK# 3,28 SLP# 3
PCI_PME# 16,28
GPI[20:13] 28 GPI21 23
FAN_LED 26 GPO27 38 GPO28 38
PGCS#0 PGCS#1 TP4409
26 PS_POK R236 1K R235 1.5K
CONFIG1 PX4_CFG1 28 CONFIG2 PX4_CFG2 28
SUSC# SUSB# SUSA#
74LVC14 74HC10 74HC112
C373 0.01 uF C183 1.0 uF C328 0.1 uF C375 0.01uF
TP045 D3
R170 1K R250 8.2K R219 10K R205 10K R218 8.2K R238 100K
VREF5V 7
WOLLID 26 POWER-ON 26
Q9 Q7 Q5 2N7002
**External logic shown is used to handle power loss condition.
J43 JMP_3P B_SUSC 26
J43 CONFIG.
1-2 SAVE STATE ON POWER DOWN.
2-3 PIIX4 POWERS ON SYS. AT POWER-UP.
RSMRST# JK_CLR
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title PIIX4E (PART II)
Size Custom
Document Number 3 DEVICE AGP
Rev 1.0
Date: 22:16:57
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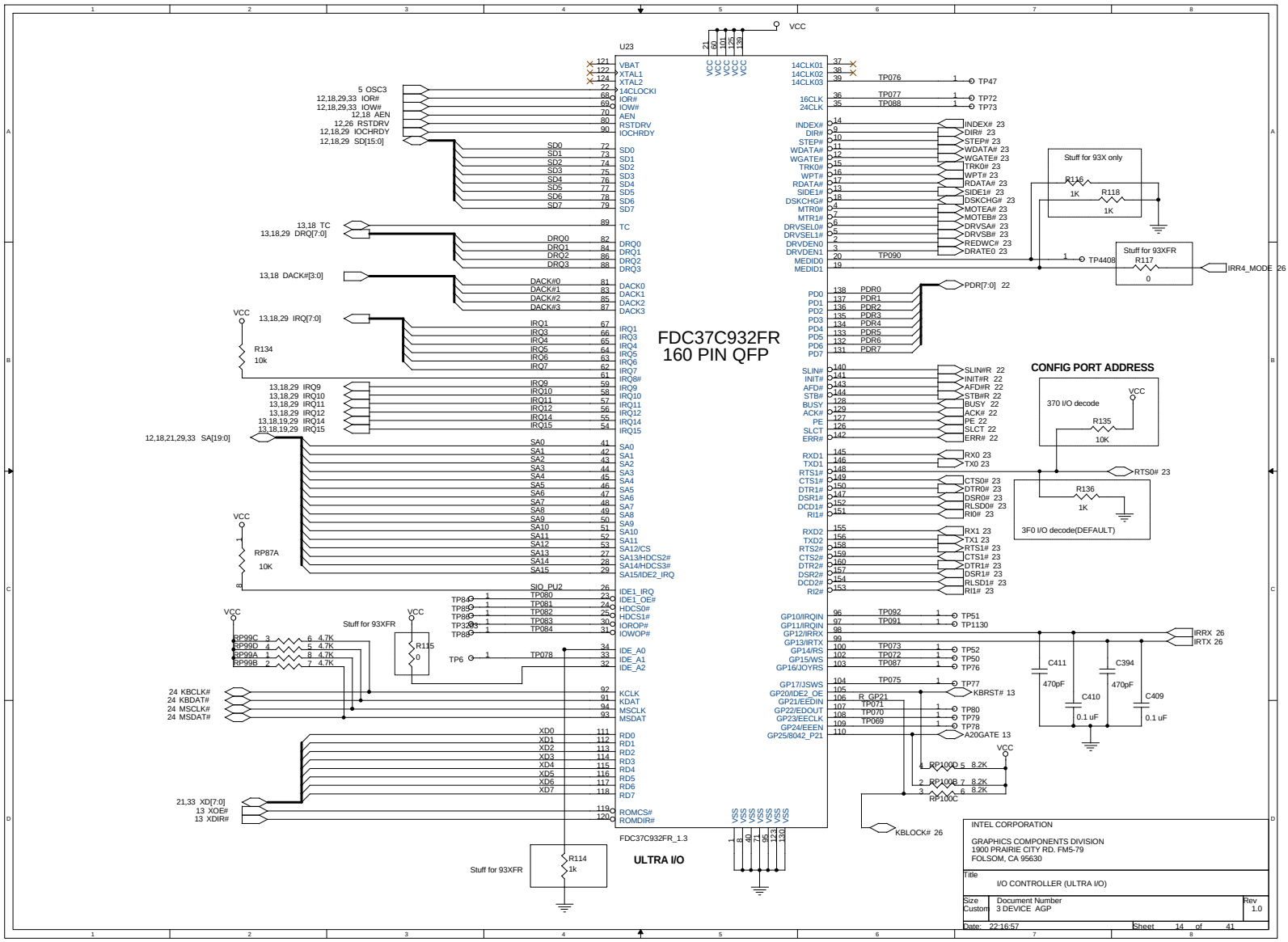
U23
FDC37C932FR
160 PIN QFP
FDC37C932FR_1.3
ULTRA I/O
VCC
VBAT
XTAL1
XTAL2
14CLOCKI
IOR#
IOW#
AEN
RSTDRV
IOCHRDY
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
TC
DRQ0
DRQ1
DRQ2
DRQ3
DACK#0
DACK#1
DACK#2
DACK#3
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8#
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12/CS
SA13/HDCS2#
SA14/HDCS3#
SA15/IDE2_IRQ
SIO_PU2
IDE1_IRQ
IDE1_OE#
HDCS0#
HDCS1#
IOROP#
IOWOP#
IDE_A0
IDE_A1
IDE_A2
KCLK
KDAT
MSCLK
MSDAT
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
ROMCS#
ROMDIR#
14CLK01
14CLK02
14CLK03
16CLK
24CLK
INDEX#
DIR#
STEP#
WDATA#
WGATE#
TRK0#
WPT#
RDATA#
SIDE1#
DSKCHG#
MTR0#
MTR1#
DRVSEL0#
DRVSEL1#
DRVDEN0
DRVDEN1
MEDID0
MEDID1
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
SLIN#
INIT#
AFD#
STB#
BUSY
ACK#
PE
SLCT
ERR#
RXD1
TXD1
RTS1#
CTS1#
DTR1#
DSR1#
DCD1#
RI1#
RXD2
TXD2
RTS2#
CTS2#
DTR2#
DSR2#
DCD2#
RI2#
GP10/IRQIN
GP11/IRQIN
GP12/IRRX
GP13/IRTX
GP14/RS
GP15/WS
GP16/JOYRS
GP17/JSWS
GP20/IDE2_OE
GP21/EEDIN
GP22/EDOUT
GP23/EECLK
GP24/EEEN
GP25/8042_P21
5 OSC3
12,18,29,33 IOR#
12,18,29,33 IOW#
12,18 AEN
12,26 RSTDRV
12,18,29 IOCHRDY
12,18,29 SD[15:0]
13,18 TC
13,18,29 DRQ[7:0]
13,18 DACK#[3:0]
13,18,29 IRQ[7:0]
13,18,29 IRQ9
13,18,29 IRQ10
13,18,29 IRQ11
13,18,29 IRQ12
13,18,19,29 IRQ14
13,18,19,29 IRQ15
12,18,21,29,33 SA[19:0]
24 KBCLK#
24 KBDAT#
24 MSCLK#
24 MSDAT#
21,33 XD[7:0]
13 XOE#
13 XDIR#
KBLOCK# 26
PDR[7:0] 22
KBRST# 13
A20GATE 13
IRR4_MODE 26
IRRX 26
IRTX 26
RTS0# 23
CONFIG PORT ADDRESS
370 I/O decode
3F0 I/O decode(DEFAULT)
Stuff for 93X only
Stuff for 93XFR
R134 10k
RP87A 10K
R115 0
R114 1k
R116 1K
R118 1K
R117 0
R135 10K
R136 1K
C411 470pF
C394 470pF
C410 0.1 uF
C409 0.1 uF
RP100D 8.2K
RP100B 8.2K
RP100C
RP99C 4.7K
RP99D 4.7K
RP99A 4.7K
RP99B 4.7K
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
I/O CONTROLLER (ULTRA I/O)
Size Custom
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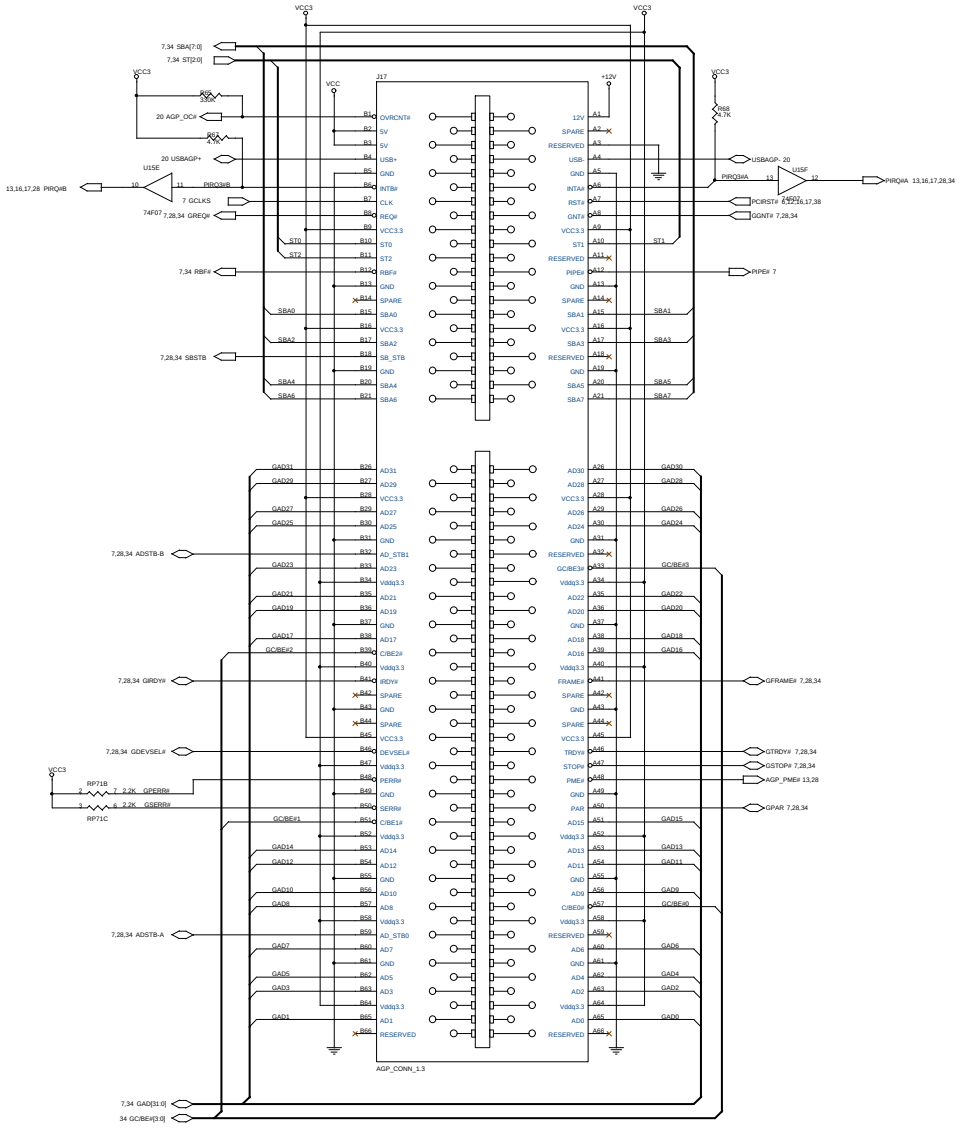
AGP CONNECTOR



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Title: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR

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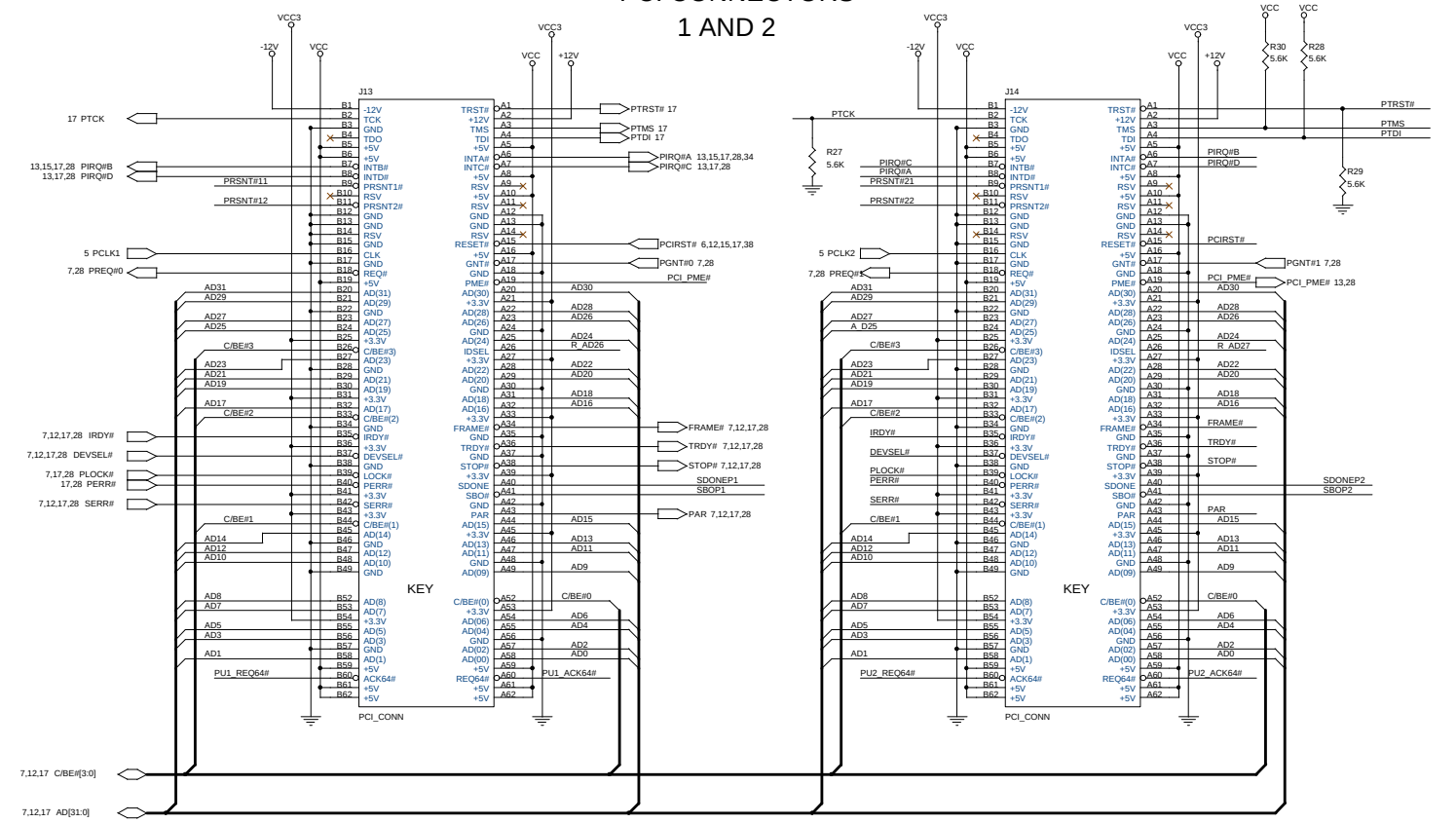
PCI CONNECTORS 1 AND 2



INTEL CORPORATION	
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title: PCI CONNECTORS 1 & 2	
Size: Custom	Document Number: 3 DEVICE AGP
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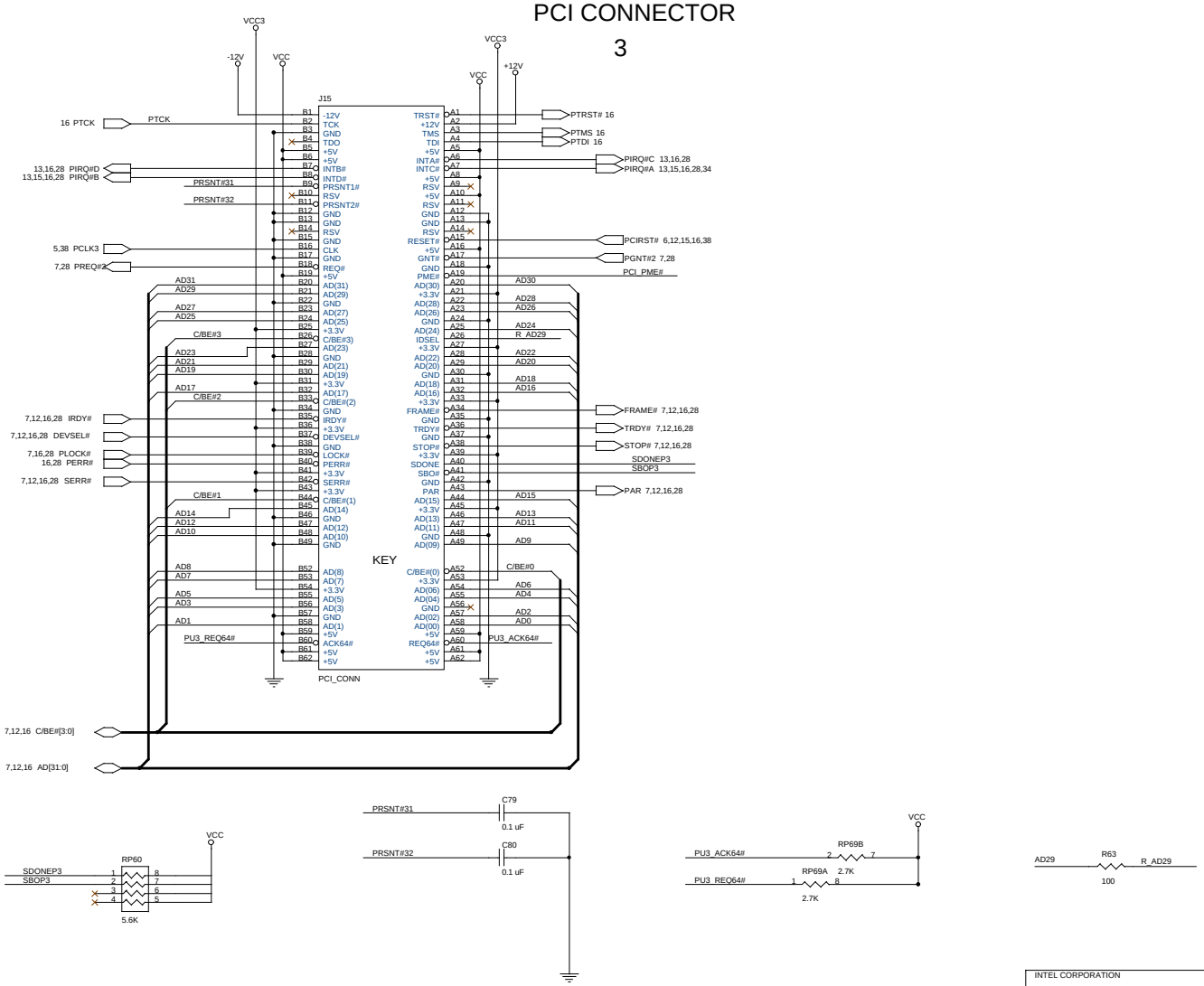
PCI CONNECTOR

3



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GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: PCI CONNECTORS 3 & 4		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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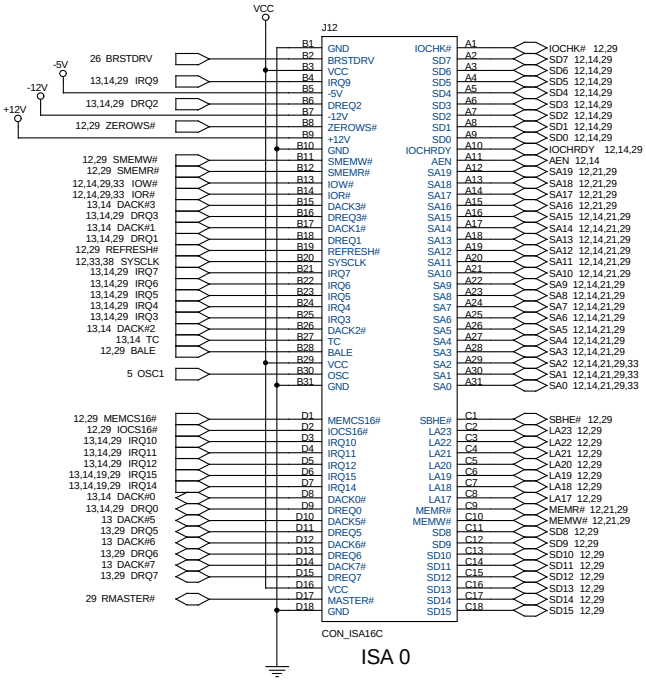
ISA SLOTS



ISA 0

INTEL CORPORATION

GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title	ISA SLOTS	
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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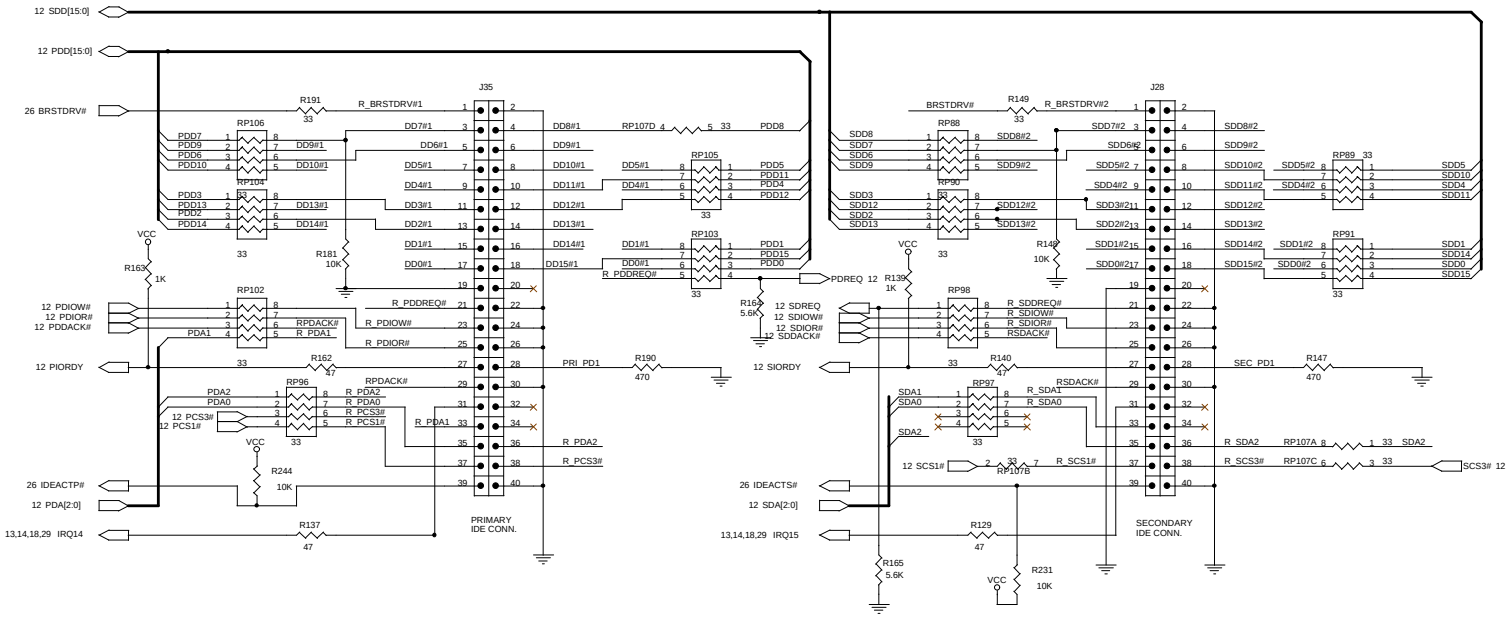
IDE CONNECTORS



INTEL CORPORATION		
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: PCI IDE CONNECTORS		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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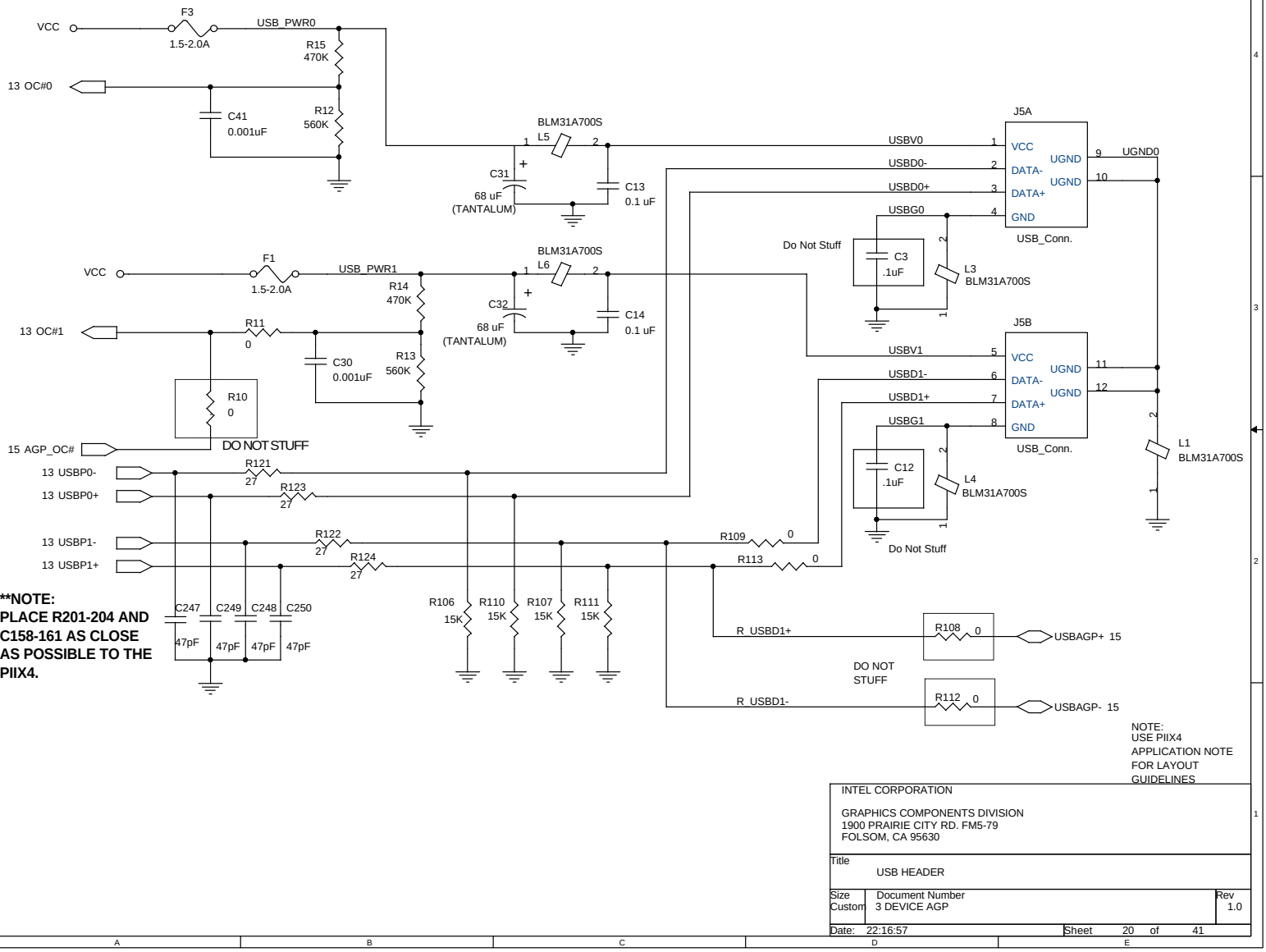
USB CONNECTORS



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1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title	USB HEADER	
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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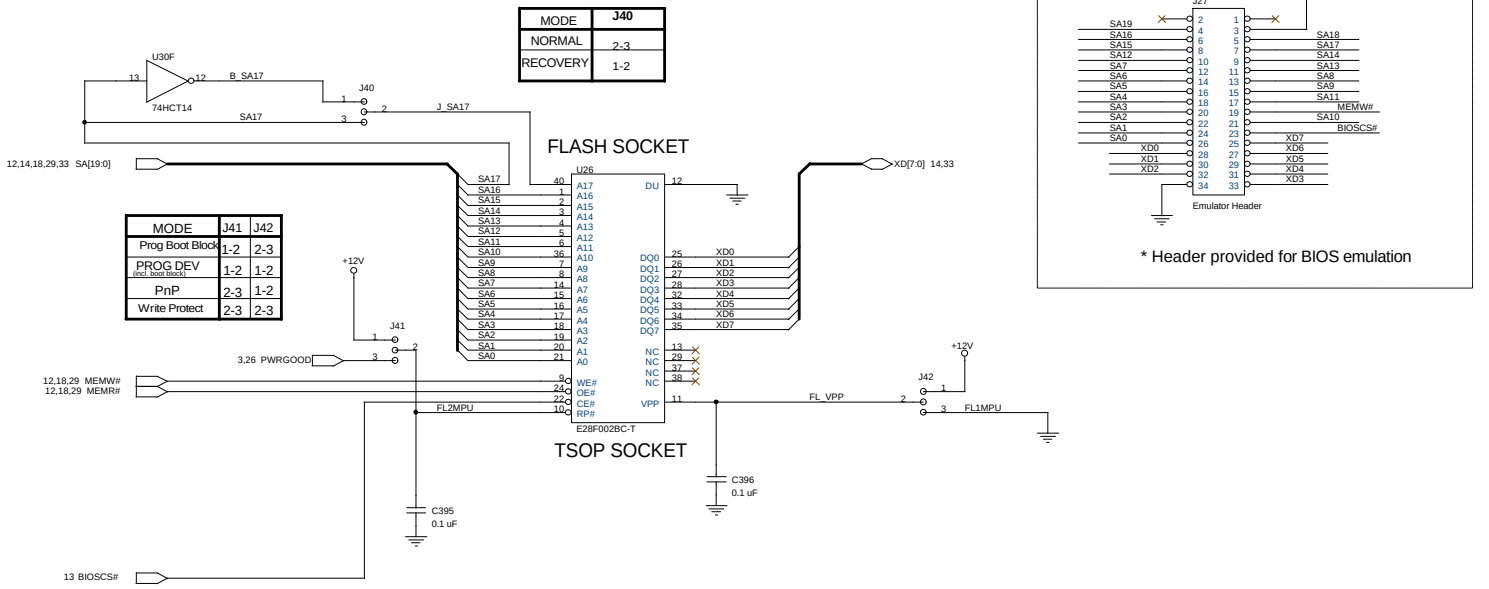
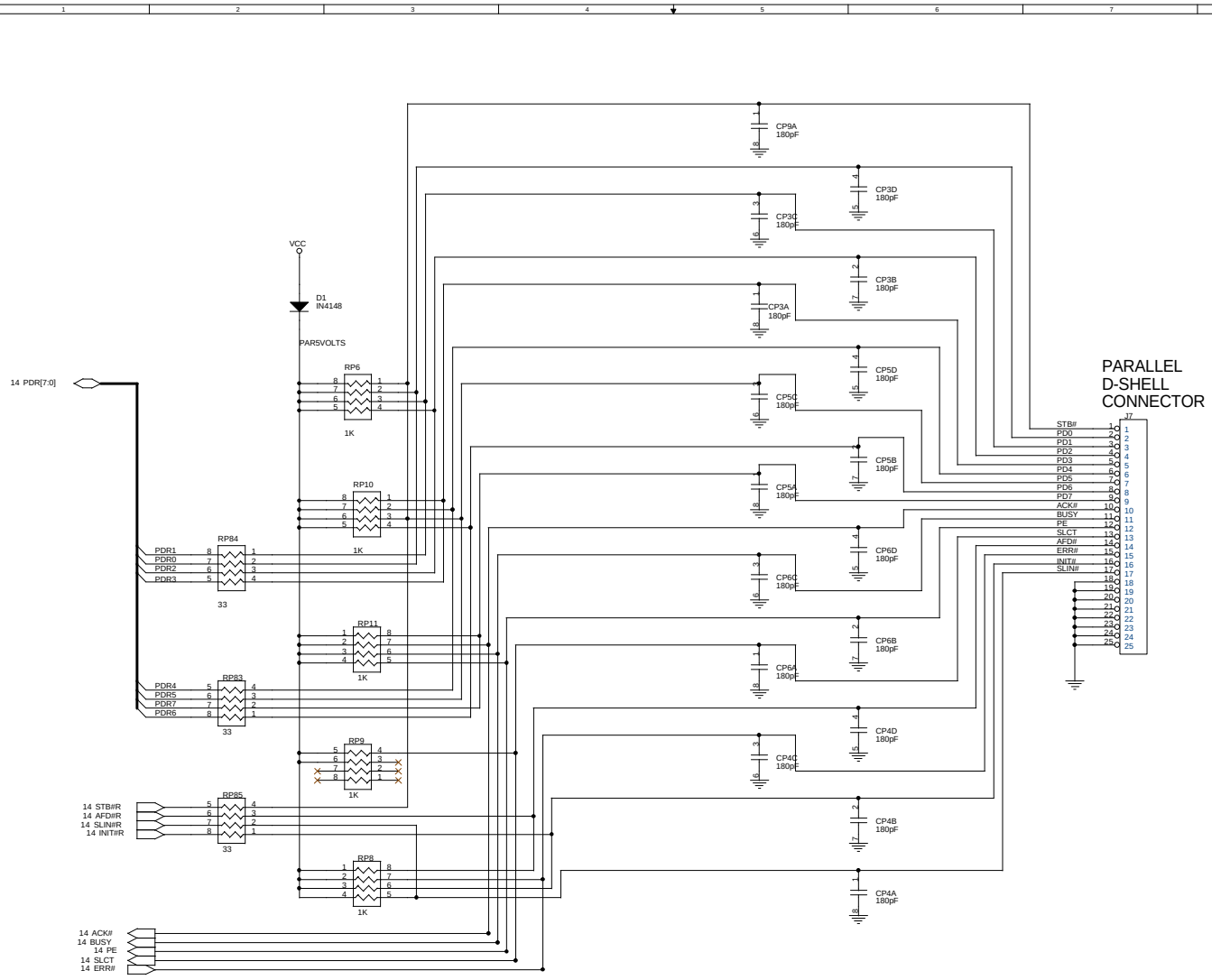
SYSTEM ROM



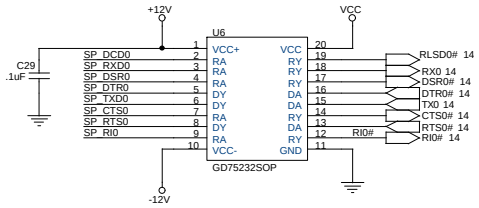
STUFFING OPTION

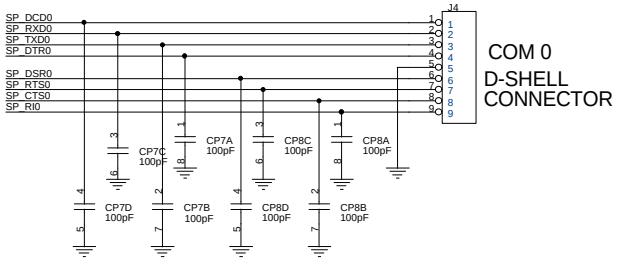
* Header provided for BIOS emulation

INTEL CORPORATION	
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title: SYSTEM ROM	
Size: Custom	Document Number: 3 DEVICE AGP
Rev: 1.0	
Date: 15:23:35	Sheet 21 of 41

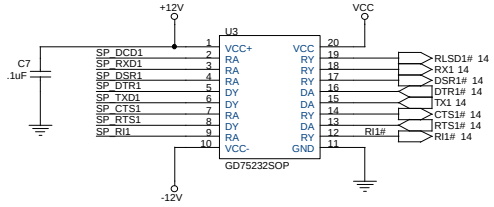


INTEL CORPORATION		
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: PARALLEL PORT		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
Date: 22:16:57	Sheet 22 of 41	

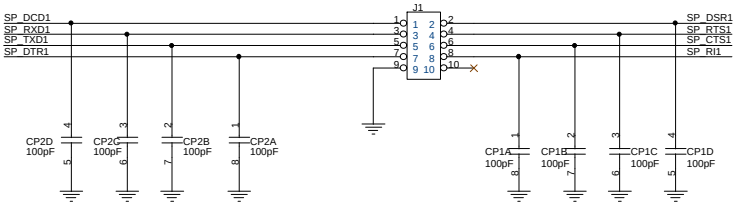


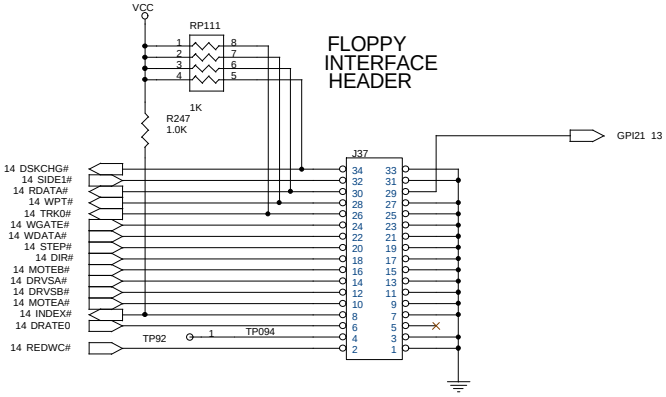


COM 0
D-SHELL
CONNECTOR



COM 1
HEADER

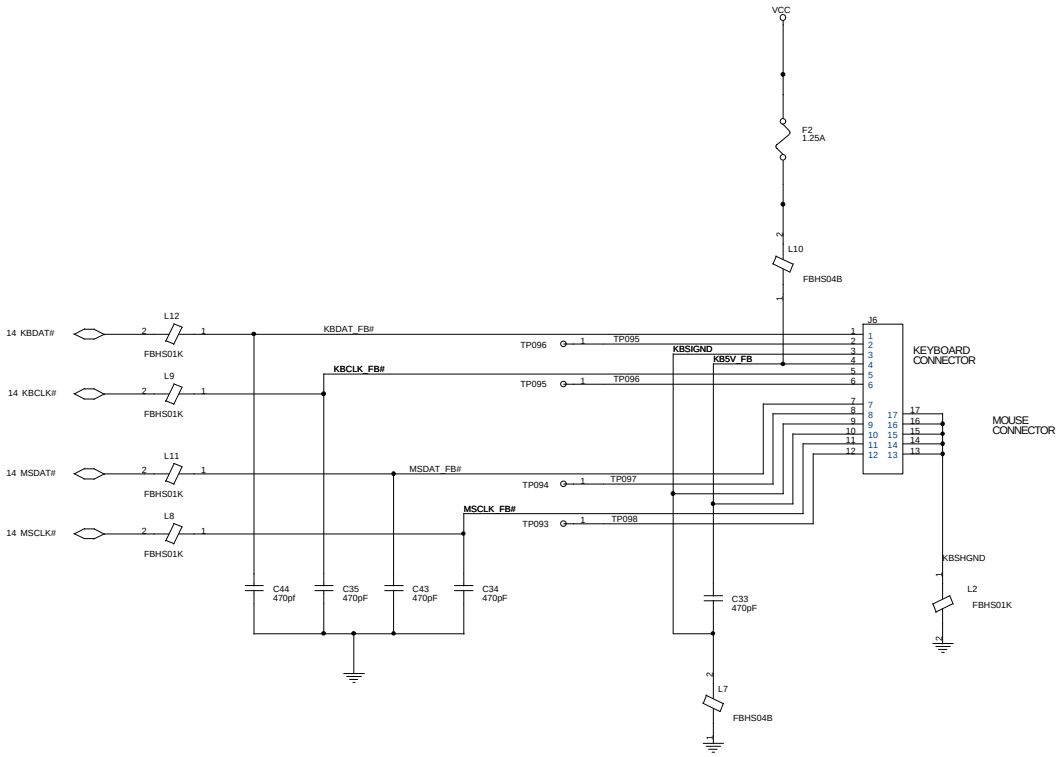




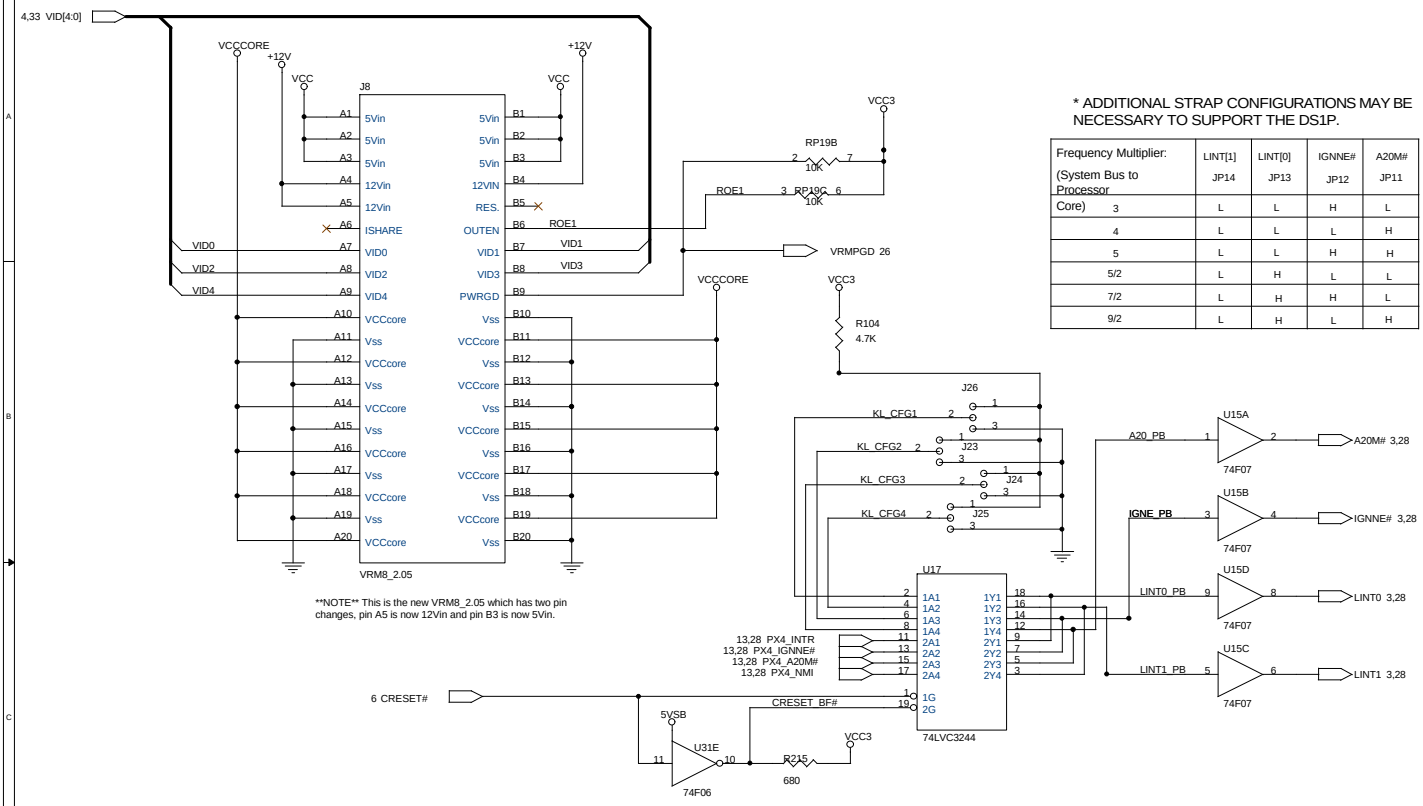
FLOPPY
INTERFACE
HEADER

**** Connected to GPI21 of the PIIX4 for BIOS detection of a floppy drive.**

INTEL CORPORATION GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title: SERIAL AND FLOPPY	
Size: Custom	Document Number: 3 Device AGP
Rev: 1.0	
Date: 15:23:35	Sheet 23 of 41



INTEL CORPORATION		
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: KEYBOARD/MOUSE INTERFACE		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
Date: 22:16:57	Sheet 24 of 41	



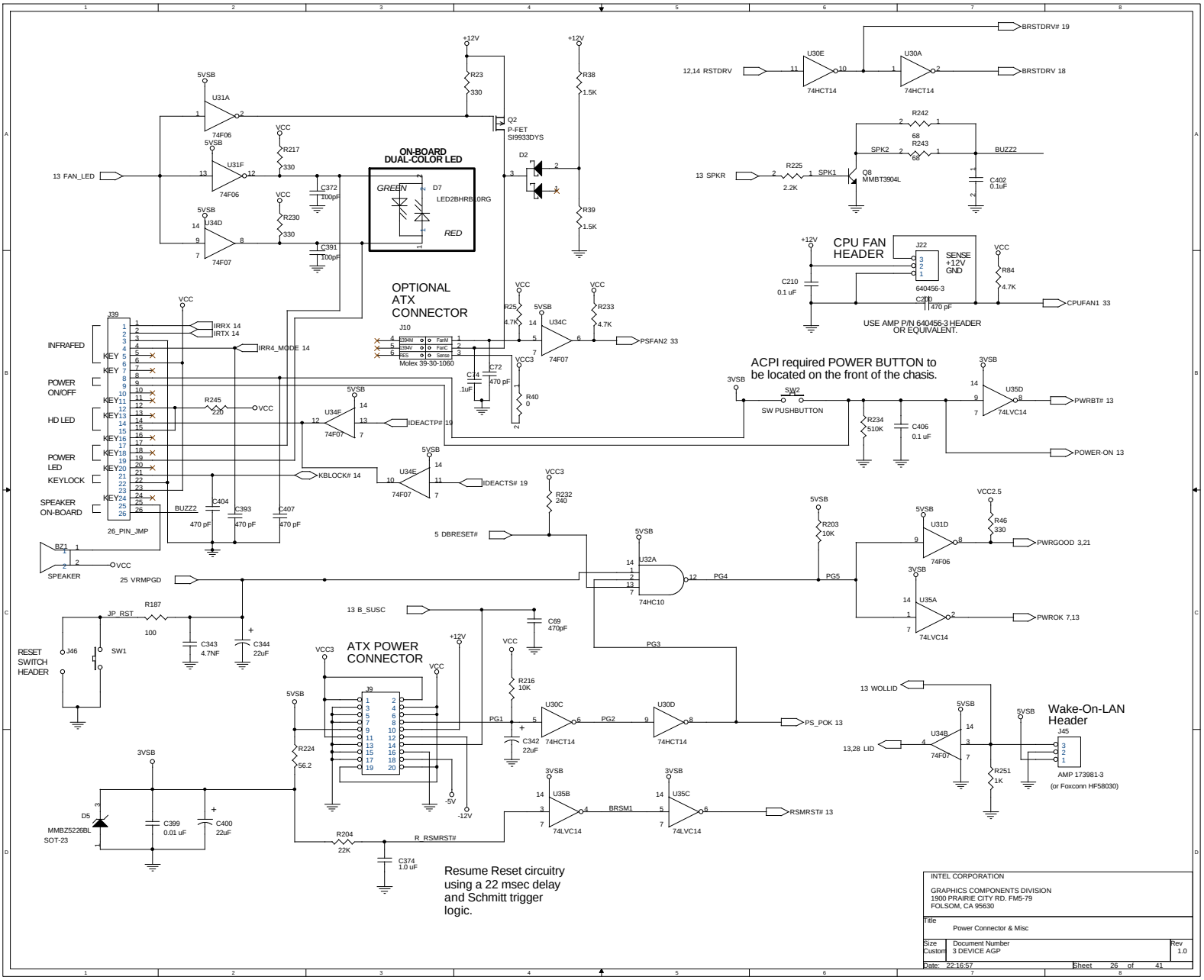
INTEL CORPORATION

GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title: DC-DC CONVERTER CONNECTORS

Size: Custom | Document Number: 3 DEVICE AGP | Rev: 1.0

Date: 22:16:57 | Sheet 25 of 41


ON-BOARD
DUAL-COLOR LED
GREEN
RED
LED2BHRB10RG
OPTIONAL
ATX
CONNECTOR
Molex 39-30-1060
CPU FAN
HEADER
SENSE
+12V
GND
640456-3
USE AMP P/N 640456-3 HEADER
OR EQUIVALENT.
ACPI required POWER BUTTON to
be located on the front of the chasis.
SW PUSHBUTTON
ATX POWER
CONNECTOR
Wake-On-LAN
Header
AMP 173981-3
(or Foxconn HF58030)
RESET
SWITCH
HEADER
SPEAKER
ON-BOARD
INFRAFED
POWER
ON/OFF
HD LED
POWER
LED
KEYLOCK
26_PIN_JMP
MMBZ5226BL
SOT-23
Resume Reset circuitry
using a 22 msec delay
and Schmitt trigger
logic.
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Power Connector & Misc
Custom
3 DEVICE AGP
1.0
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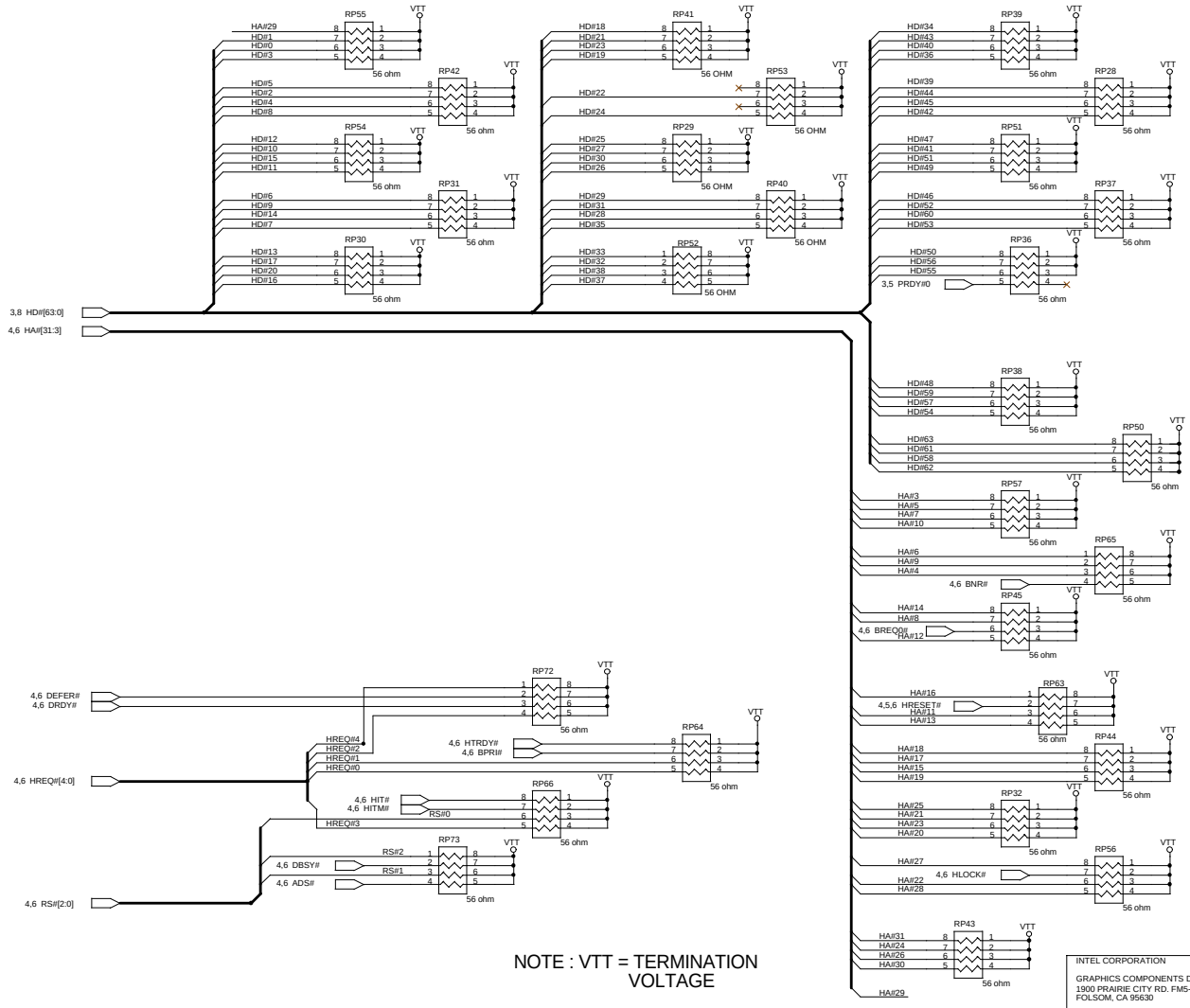
Sheet 26 of 41

GTL+ TERMINATION RESISTORS

*NOTE: May be removed if route lengths can be restricted to 1.5" MIN to 4.0" MAX.



NOTE : VTT = TERMINATION VOLTAGE

INTEL CORPORATION

GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title: GTL TERMINATION

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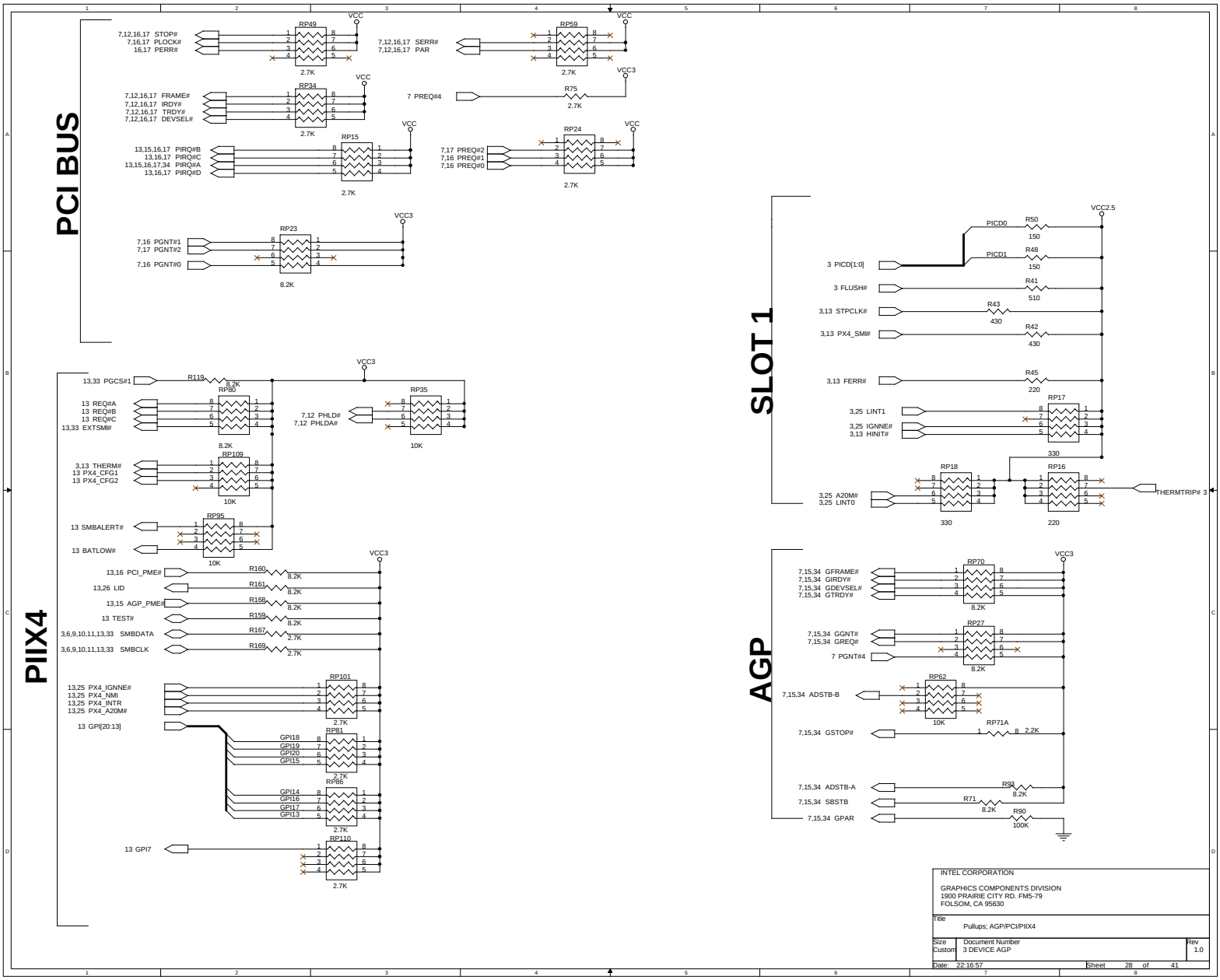
Date: 22:16:57 Sheet 27 of 41


PCI BUS
SLOT 1
PIIX4
AGP
7,12,16,17 STOP#
7,16,17 PLOCK#
16,17 PERR#
RP49
2.7K
7,12,16,17 SERR#
7,12,16,17 PAR
RP59
2.7K
7,12,16,17 FRAME#
7,12,16,17 IRDY#
7,12,16,17 TRDY#
7,12,16,17 DEVSEL#
RP34
2.7K
7 PREQ#4
R75
2.7K
13,15,16,17 PIRQ#B
13,16,17 PIRQ#C
13,15,16,17,34 PIRQ#A
13,16,17 PIRQ#D
RP15
2.7K
7,17 PREQ#2
7,16 PREQ#1
7,16 PREQ#0
RP24
2.7K
7,16 PGNT#1
7,17 PGNT#2
7,16 PGNT#0
RP23
8.2K
13,33 PGCS#1
R119
8.2K
13 REQ#A
13 REQ#B
13 REQ#C
13,33 EXTSMI#
RP80
8.2K
7,12 PHLD#
7,12 PHLDA#
RP35
10K
3,13 THERM#
13 PX4_CFG1
13 PX4_CFG2
RP109
10K
13 SMBALERT#
13 BATLOW#
RP95
10K
13,16 PCI_PME#
13,26 LID
13,15 AGP_PME#
13 TEST#
3,6,9,10,11,13,33 SMBDATA
3,6,9,10,11,13,33 SMBCLK
R160
R161
R168
R159
R167
R169
8.2K
2.7K
13,25 PX4_IGNNE#
13,25 PX4_NMI
13,25 PX4_INTR
13,25 PX4_A20M#
RP101
2.7K
13 GPI[20:13]
GPI18
GPI19
GPI20
GPI15
RP81
2.7K
GPI14
GPI16
GPI17
GPI13
RP86
2.7K
13 GPI7
RP110
2.7K
PICD0
PICD1
R50
R48
150
3 PICD[1:0]
3 FLUSH#
3,13 STPCLK#
3,13 PX4_SM#
R41
R43
R42
510
430
430
3,13 FERR#
R45
220
3,25 LINT1
3,25 IGNNE#
3,13 HINIT#
RP17
330
3,25 A20M#
3,25 LINT0
RP18
330
RP16
220
THERMTRIP# 3
7,15,34 GFRAME#
7,15,34 GIRDY#
7,15,34 GDEVSEL#
7,15,34 GTRDY#
RP70
8.2K
7,15,34 GGNT#
7,15,34 GREQ#
7 PGNT#4
RP27
8.2K
7,15,34 ADSTB-B
RP62
10K
7,15,34 GSTOP#
RP71A
2.2K
7,15,34 ADSTB-A
7,15,34 SBSTB
7,15,34 GPAR
R92
R71
R90
8.2K
8.2K
100K
VCC
VCC3
VCC2.5
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
Pullups; AGP/PCI/PIIX4
Size
Custom
Document Number
3 DEVICE AGP
Rev
1.0
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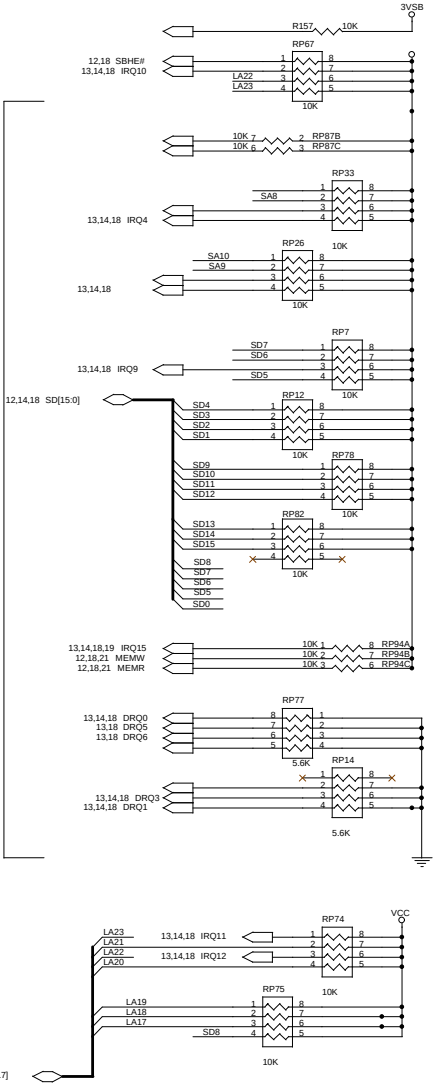
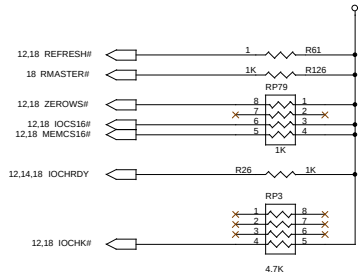
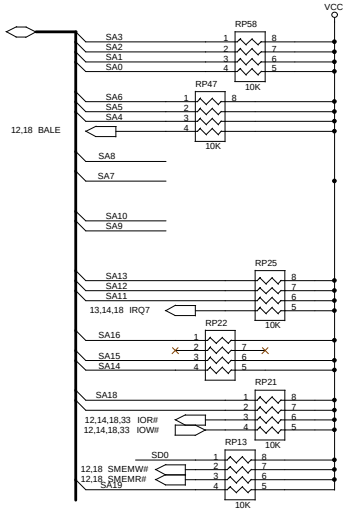
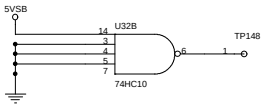
ISA BUS

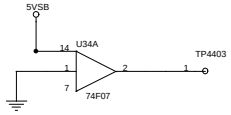


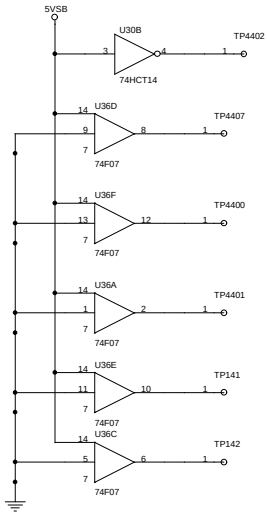


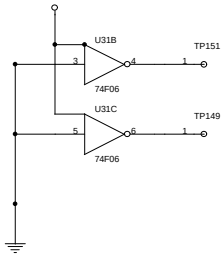


UNUSED GATES

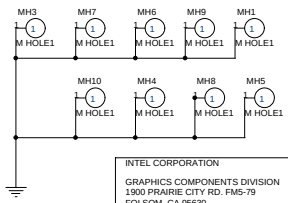




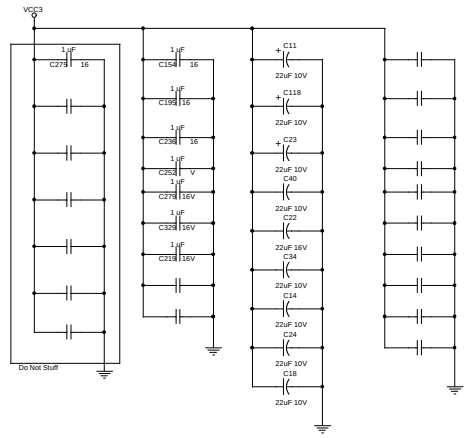


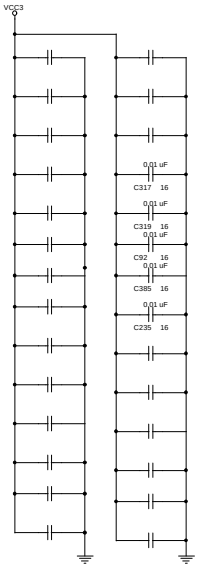


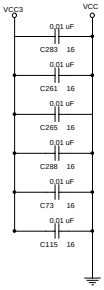
Mounting Holes

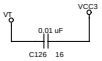


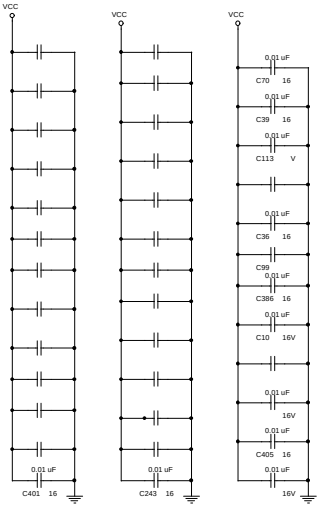
INTEL CORPORATION	
GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630	
Title	ISA BUS PULLUPS
Size: Custom	Document Number: 3 DEVICE AGP
Rev	1.0
Date:	Sheet 29 of 41











INTEL CORPORATION

GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title

DRAM, CLOCK AND 440BX DECOUPLING CAPACITORS

Size C | Document Number 3 DEVICE AGP | 1.0

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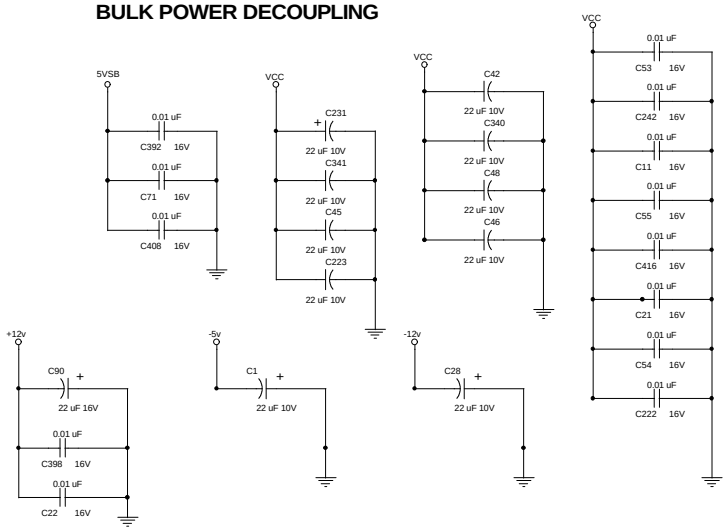
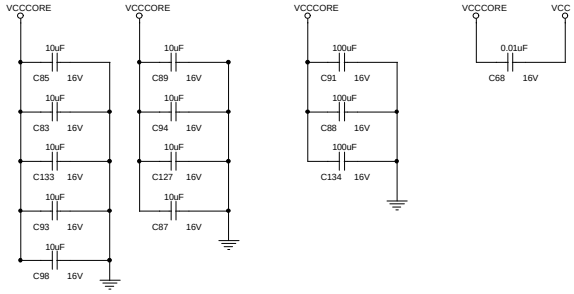
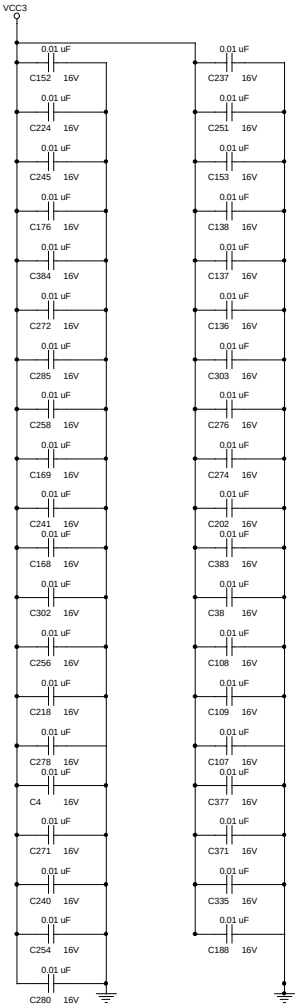
BULK POWER DECOUPLING



CORE VOLTAGE DECOUPLING





INTEL CORPORATION

GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title: 3.3 VOLT AND BULK POWER DECOUPLING

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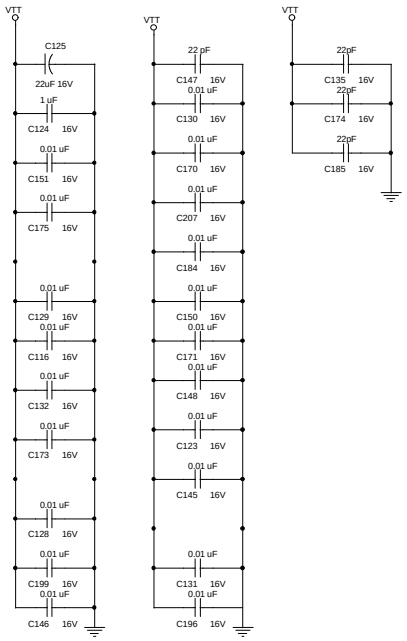
TERMINATION VOLTAGE DECOUPLING



INTEL CORPORATION GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: TERMINATION DECOUPLING		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
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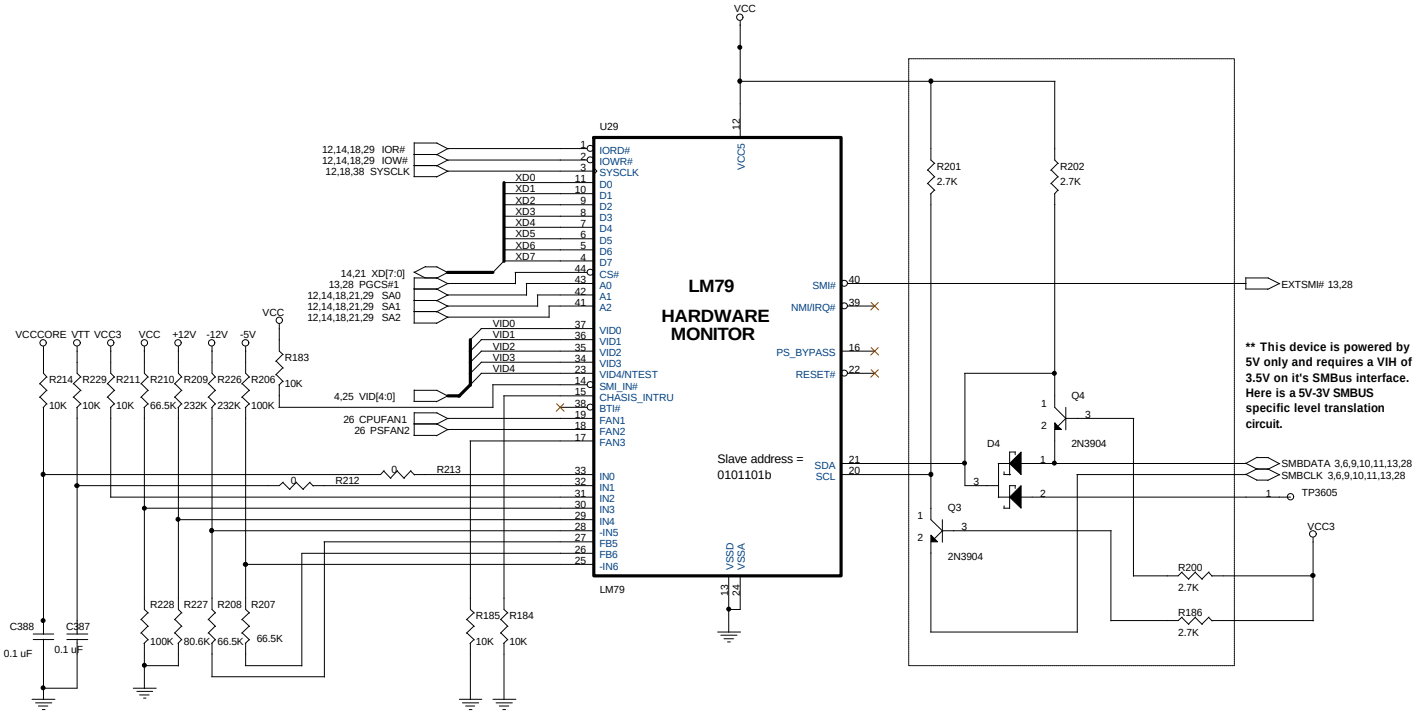
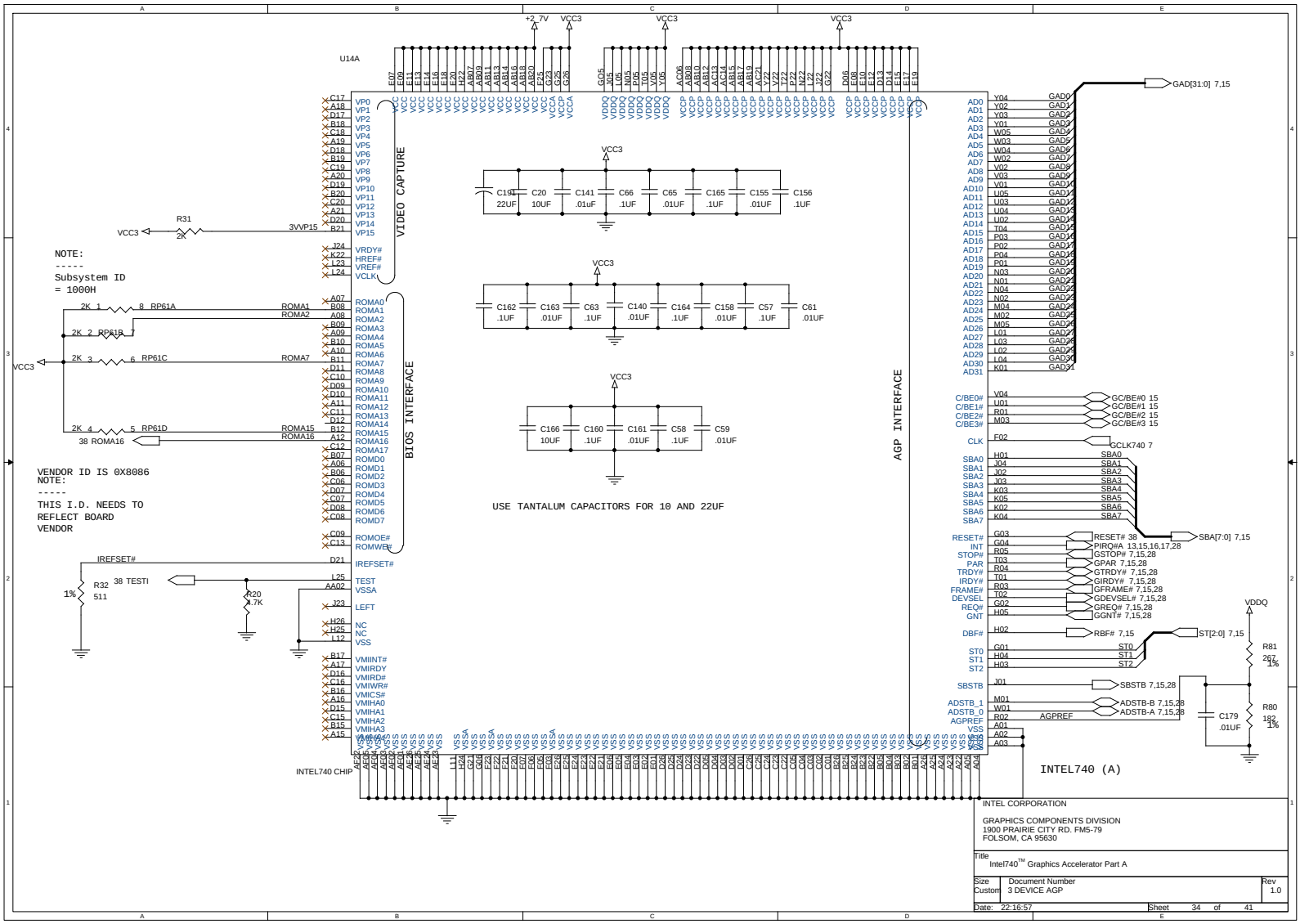
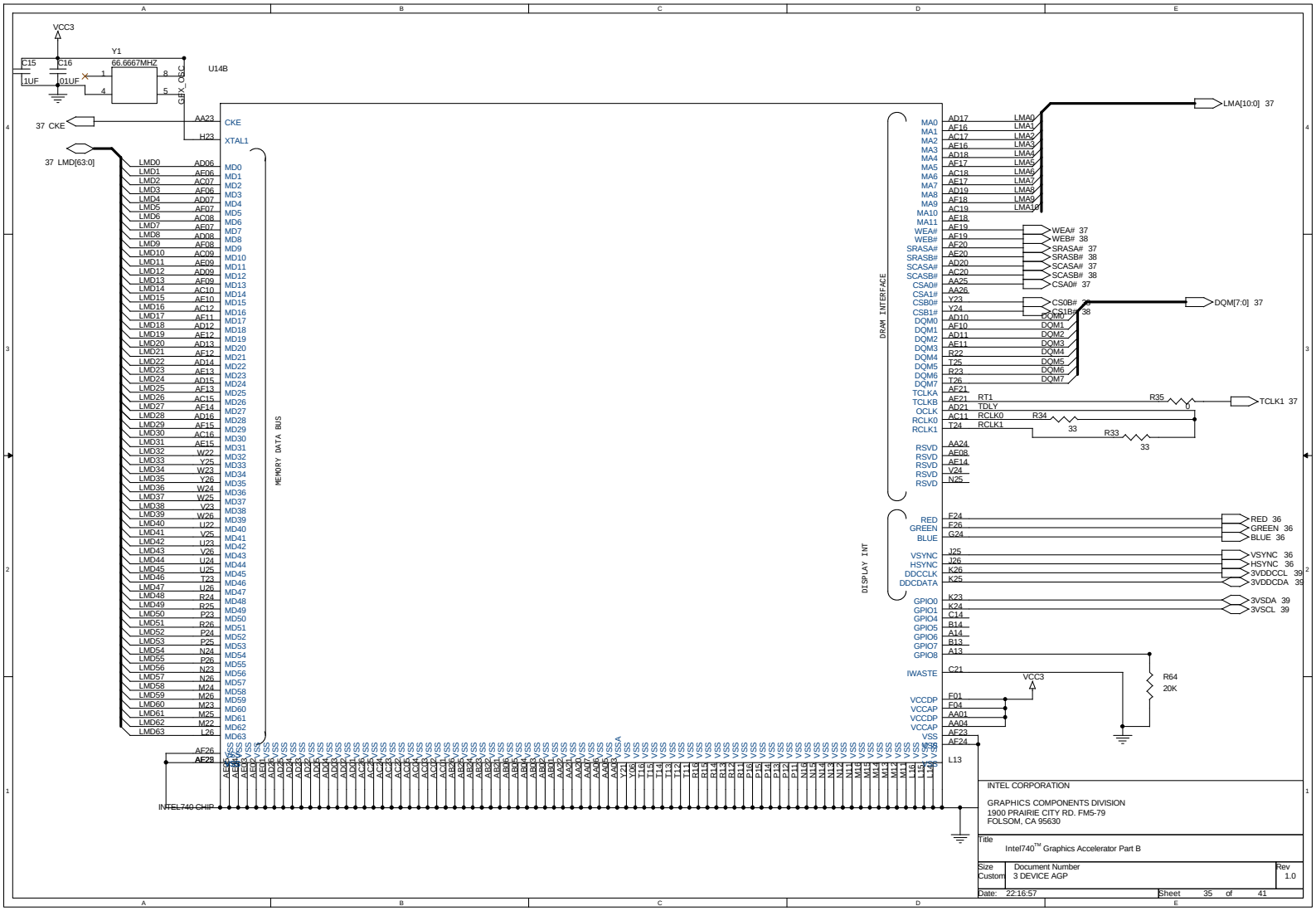


**** This device is powered by 5V only and requires a VIH of 3.5V on it's SMBus interface. Here is a 5V-3V SMBUS specific level translation circuit.**

INTEL CORPORATION GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA. 95630		
Title: LM79 MONITOR		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
Date: Thursday, July 02, 1998	Sheet 33 of 41	


U14A
VIDEO CAPTURE
BIOS INTERFACE
AGP INTERFACE
INTEL740 CHIP
INTEL740 (A)
+2_7V
VCC3
VDDQ
GAD[31:0] 7,15
NOTE:
Subsystem ID
= 1000H
VENDOR ID IS 0X8086
NOTE:
THIS I.D. NEEDS TO
REFLECT BOARD
VENDOR
USE TANTALUM CAPACITORS FOR 10 AND 22UF
R31
2K
3VVP15
RP61A
RP61B
RP61C
RP61D
ROMA1
ROMA2
ROMA7
ROMA15
ROMA16
38 ROMA16
IREFSET#
R32
511
1%
38 TESTI
R20
4.7K
C191
22UF
C20
10UF
C141
.01uF
C66
.1UF
C65
.01UF
C165
.1UF
C155
.01UF
C156
.1UF
C162
.1UF
C163
.01UF
C63
.1UF
C140
.01UF
C164
.1UF
C158
.01UF
C57
.1UF
C61
.01UF
C166
10UF
C160
.1UF
C161
.01UF
C58
.1UF
C59
.01UF
GC/BE#0 15
GC/BE#1 15
GC/BE#2 15
GC/BE#3 15
GCLK740 7
SBA[7:0] 7,15
RESET# 38
PIRQ#A 13,15,16,17,28
GSTOP# 7,15,28
GPAR 7,15,28
GTRDY# 7,15,28
GIRDY# 7,15,28
GFRAME# 7,15,28
GDEVSEL# 7,15,28
GREQ# 7,15,28
GGNT# 7,15,28
RBF# 7,15
ST[2:0] 7,15
R81
267
1%
R80
182
1%
C179
.01UF
SBSTB 7,15,28
ADSTB-B 7,15,28
ADSTB-A 7,15,28
AGPREF
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
Intel740™ Graphics Accelerator Part A
Size
Custom
Document Number
3 DEVICE AGP
Rev
1.0
Date: 22:16:57
Sheet 34 of 41


VCC3
Y1
C15
C16
66.6667MHZ
1UF
01UF
U14B
CKE
XTAL1
MEMORY DATA BUS
DRAM INTERFACE
DISPLAY INT
INTEL740 CHIP
LMA[10:0] 37
DQM[7:0] 37
TCLK1 37
R35
R34
R33
33
R64
20K
RED 36
GREEN 36
BLUE 36
VSYNC 36
HSYNC 36
3VDDCCL 39
3VDDCDA 39
3VSDA 39
3VSCL 39
WEA# 37
WEB# 38
SRASA# 37
SRASB# 38
SCASA# 37
SCASB# 38
CSA0# 37
CS0B# 38
CS1B# 38
INTEL CORPORATION
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630
Title
Intel740™ Graphics Accelerator Part B
Size
Custom
Document Number
3 DEVICE AGP
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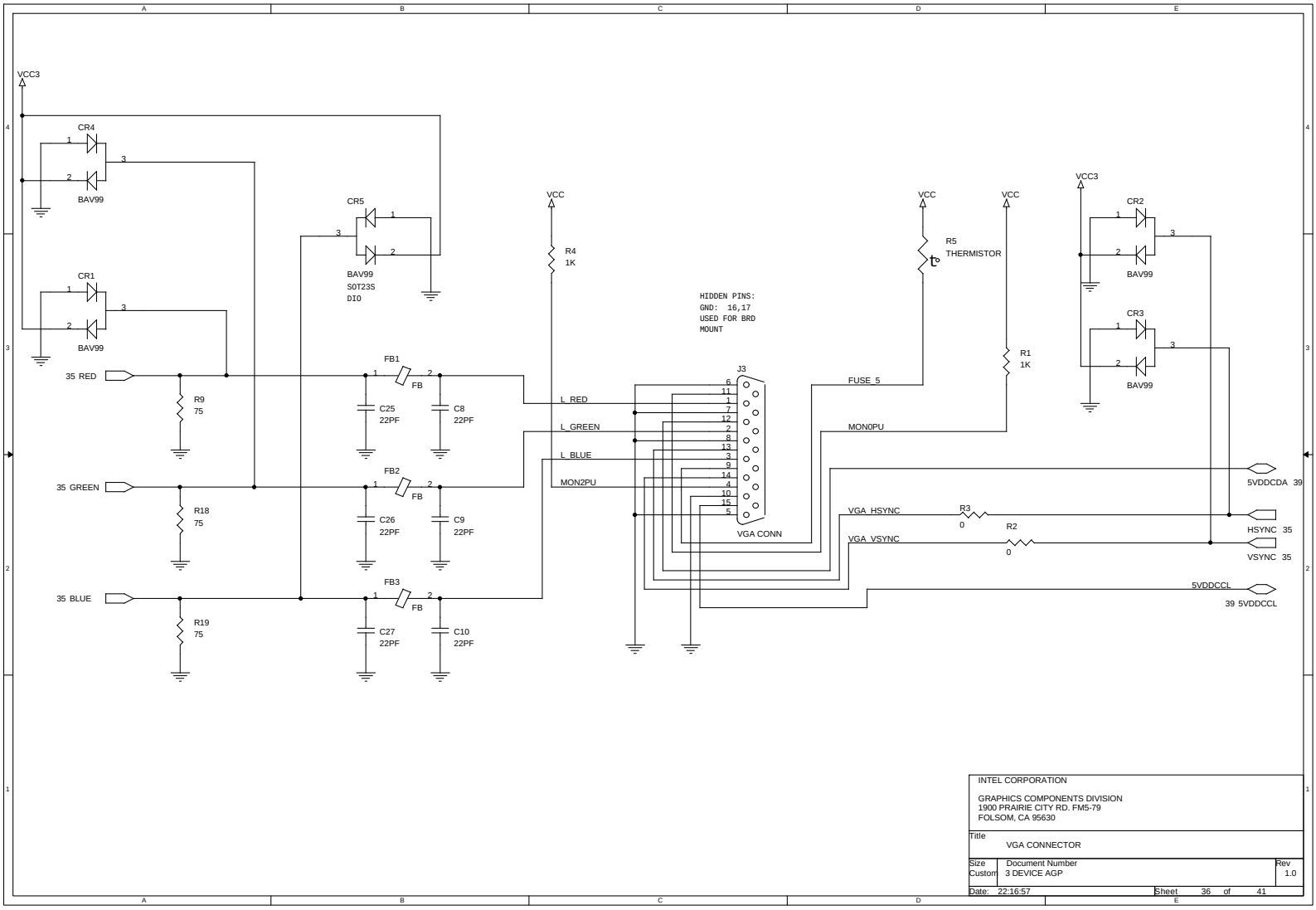
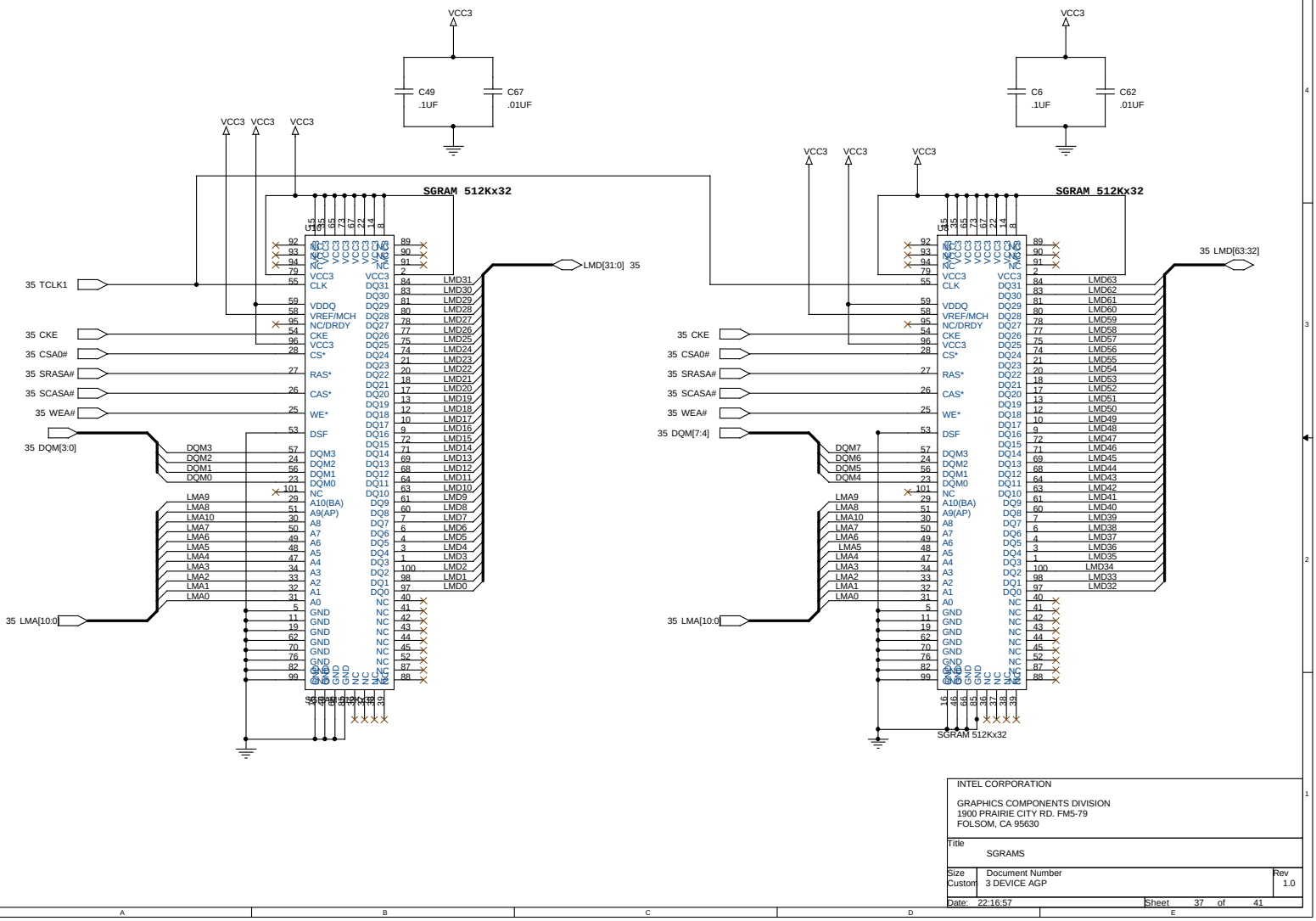


INTEL CORPORATION GRAPHICS COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-79 FOLSOM, CA 95630		
Title: VGA CONNECTOR		
Size: Custom	Document Number: 3 DEVICE AGP	Rev: 1.0
Date: 22:16:57	Sheet 36 of 41	



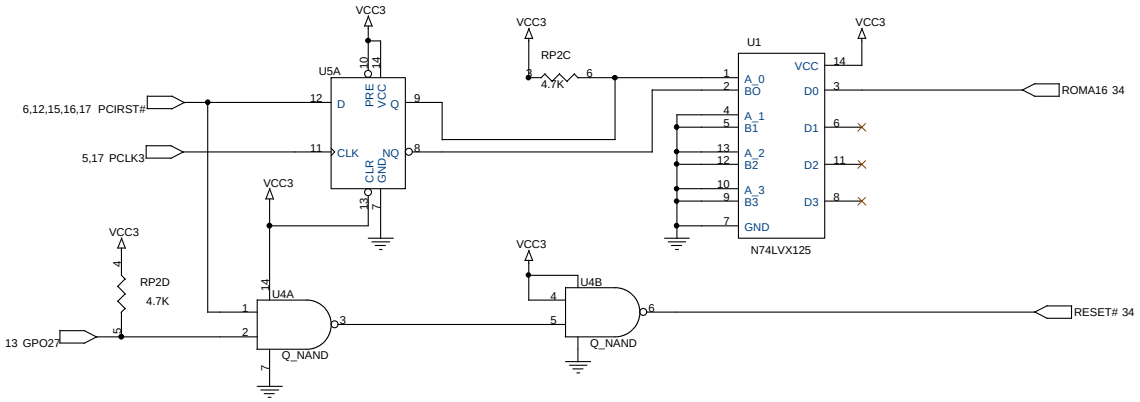
INTEL CORPORATION

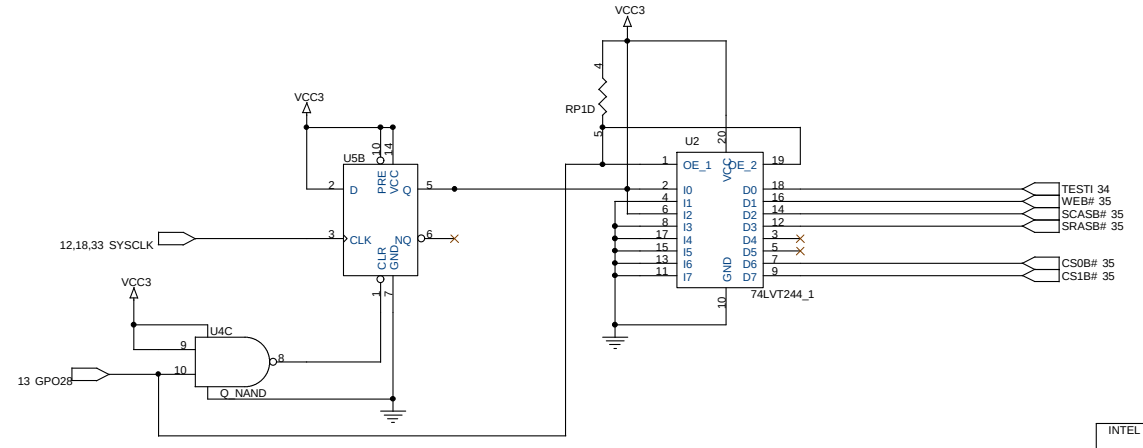
GRAPHICS COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-79
FOLSOM, CA 95630

Title: SGRAMS

Size	Document Number	Rev
Custom	3 DEVICE AGP	1.0

Date: 22:16:57 Sheet 37 of 41





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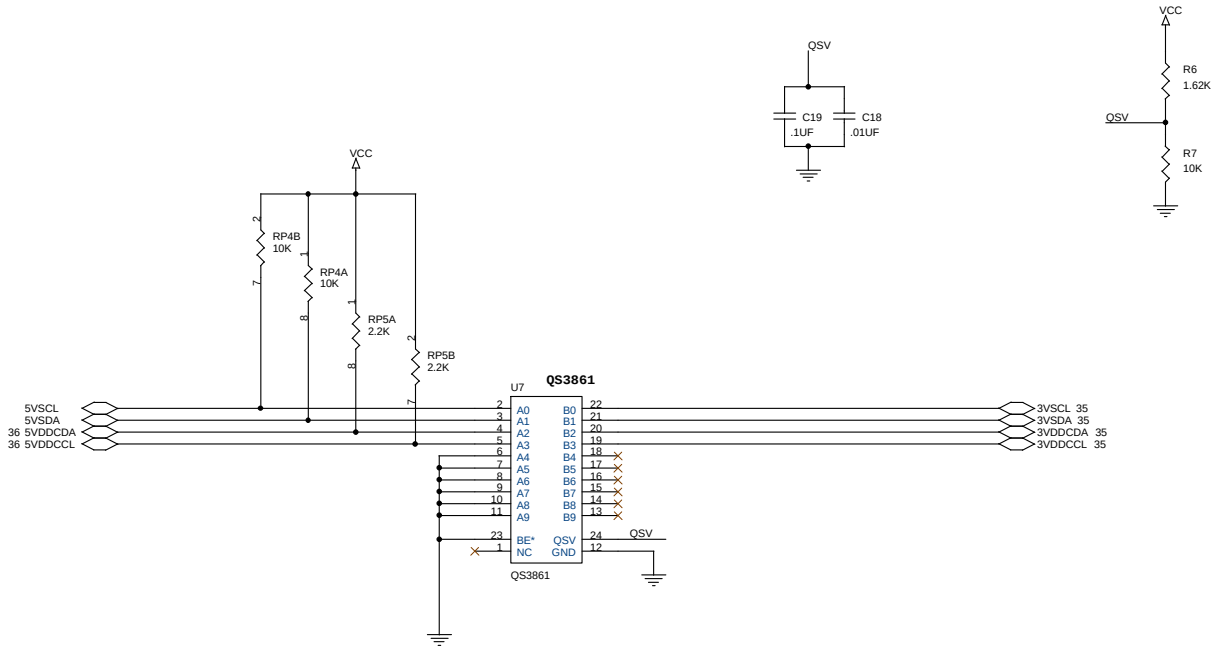

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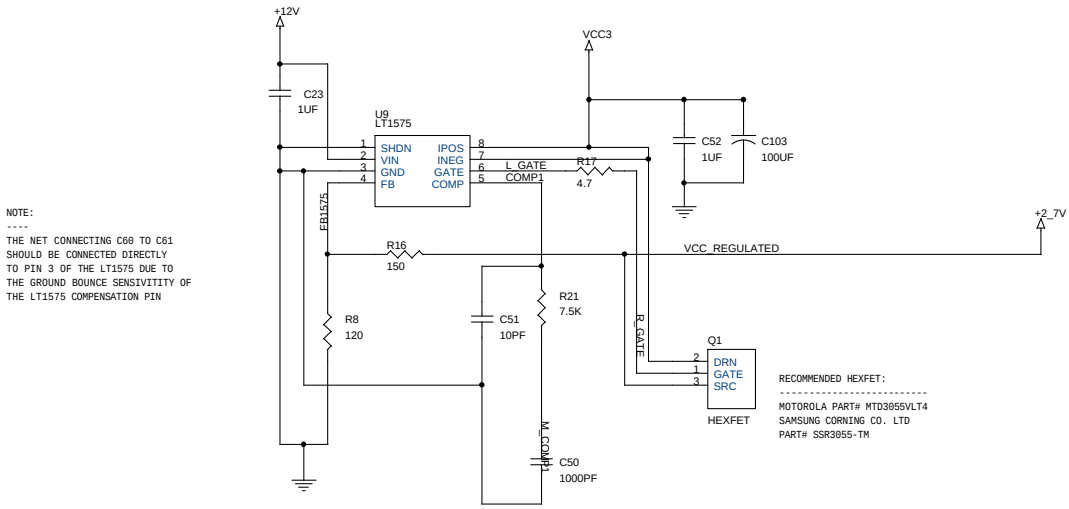
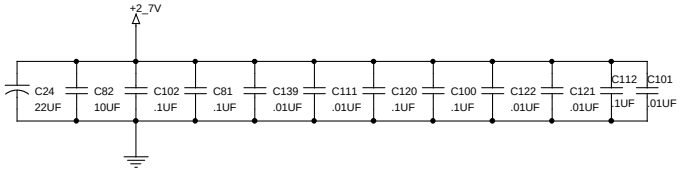


NOTE:

THE NET CONNECTING C60 TO C61
SHOULD BE CONNECTED DIRECTLY
TO PIN 3 OF THE LT1575 DUE TO
THE GROUND BOUNCE SENSIVITITY OF
THE LT1575 COMPENSATION PIN

RECOMMENDED HEXFET:

MOTOROLA PART# MTD3055VLT4
SAMSUNG CORNING CO. LTD
PART# SSR3055-TM



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REVISION1.0 8/98 -First release of 3 Device AGP schematics.

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4

Thermal Considerations

Thermal Considerations 4

Thermal design is an important step in the total design process which must not be overlooked. ***Systems or cards designed without considering the thermal environment may experience failures.*** Depending on the usage of the Intel740™ graphics accelerator, the thermal solution may change. The following table lists the design considerations which must be made.

Table 4-1. Thermal Design Considerations Chart

Intel740 Graphics Accelerator Usage	Design Considerations
Designing for Retail Add-In Card	Must design for worst case (no Airflow, 55^{o} C)
Designing for Use With OEM System	Work with the OEM, determining Chassis & Airflow

For a comprehensive guide to thermal design, please refer to *Application Note 653, Thermal Design Considerations.*This application note is provided in *Appendix B* of this document.

5

Mechanical Information

Mechanical Information 5

5.1 Board Dimensions

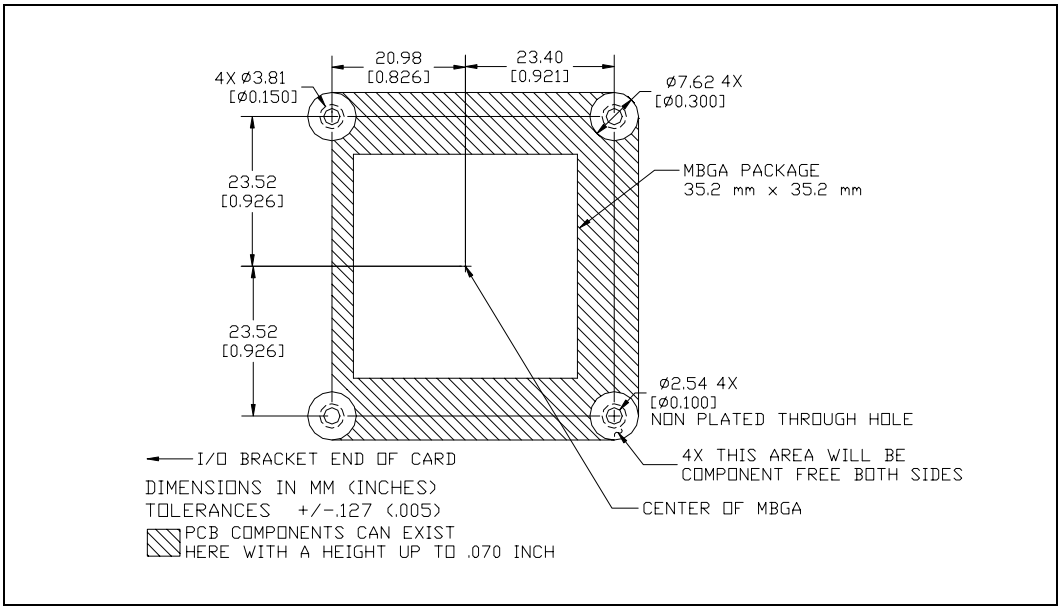
Board Dimensions should be obtained from the AGP 1.0 Specifications and the associated Engineering Change Requests (ECRs).

5.2 Fan/Heatsink Hole Pattern

Note: This solution is only need for those designs in which it has been determined there is a need for additional thermal cooling through the use of a fansink.

The Intel740™ graphics accelerator reference board has the capability of attaching a fansink. If a design requires a fansink, the following design issues must be observed to be compatible with the fan attach mechanism Intel has enabled. The mounting holes must be nonplated but each must have a grounded annular ring on the solder side of the board surrounding the hole. This annular ring should have an inner diameter of 150 mils and an outer diameter of 300 mils. This ring should contain at least eight ground connections. The solder mask opening for these holes should have a radius of 300 mils. The position of these mounting holes in relation to the MBGA is shown in Figure 5-1.

Figure 5-1. Mounting Hole Locations (Fan/Heatsink Assembly)



5.3 VMI Header Placement

The VMI header allows the connection of a DVD daughter Card. The reference card places the header at the bottom of the card. For other designs, these headers may be placed at the top of the board. The latter is recommended for an NLX card.

Figure 5-2. VMI Header Placement

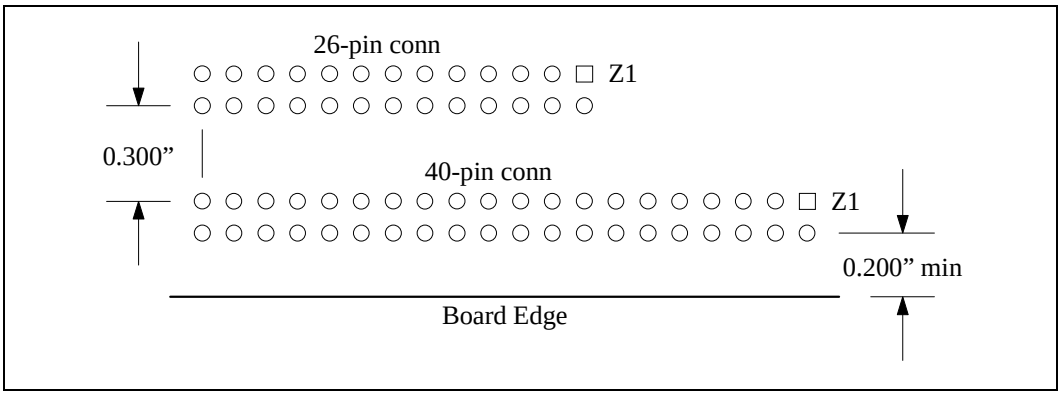
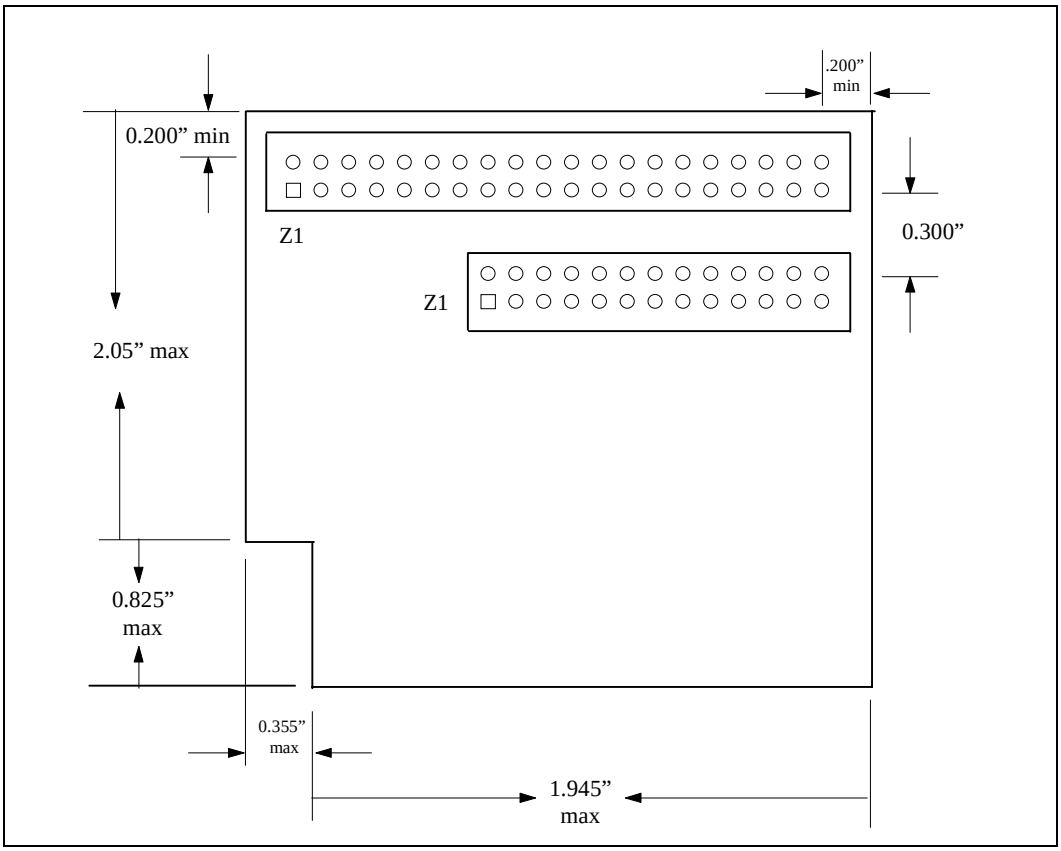


Figure 5-3. DVD Daughter Card Dimensions (ATX and NLX)—Top Side



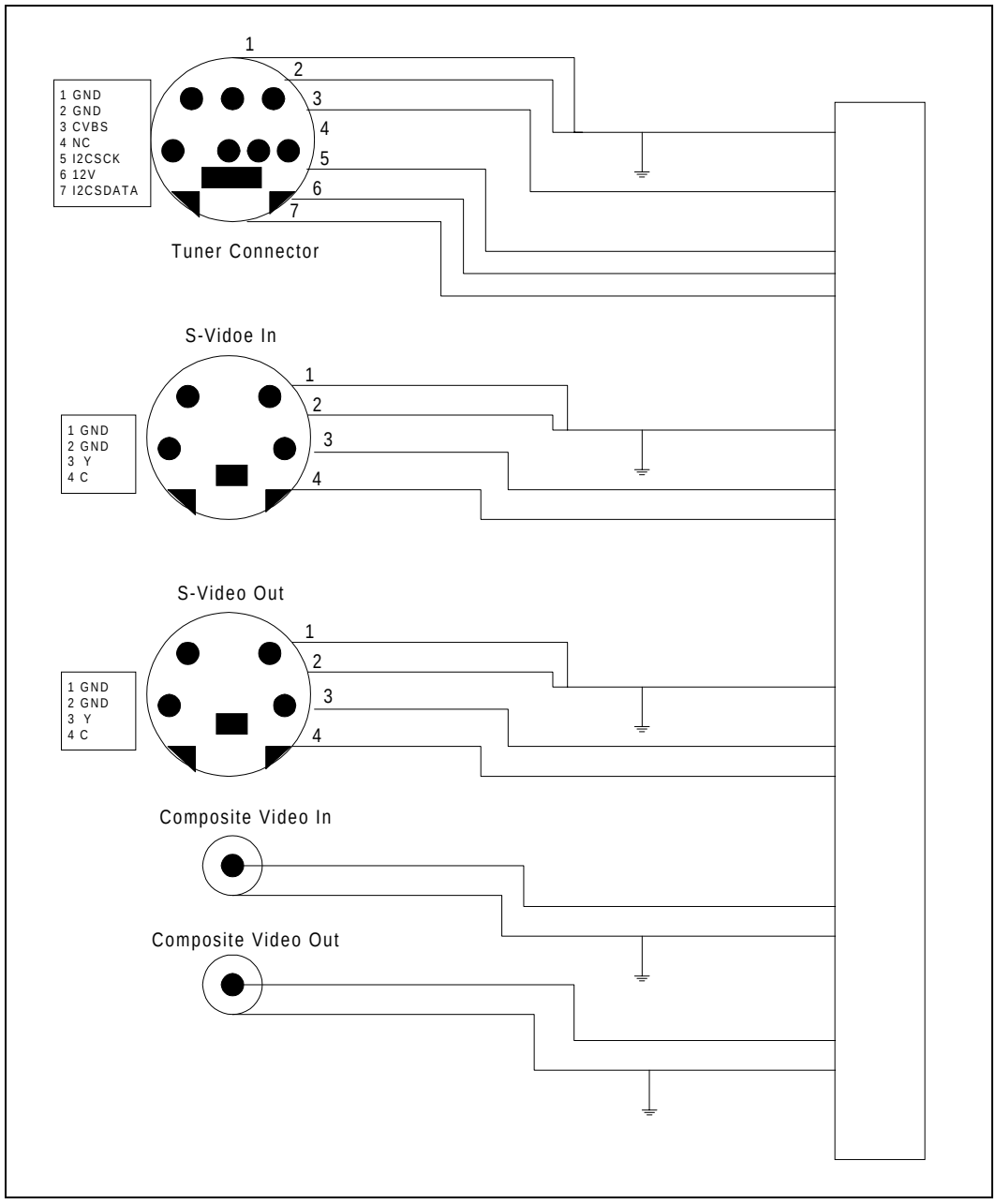
Note: Z1 Connectors in Figure 5-3 are on the backside of the card.

The dimensions shown in Figure 5-3 should be kept in mind when placing the VMI Headers. The reference DVD daughter cards will be designed for a maximum graphics board component height of 0.2”. If the component height exceeds these dimensions underneath the daughter card, the daughter card may not fit.

5.4 50 Pin Video Connector

The following diagram is a pinout view of the 50 pin video connector illustrating the different video connections which can exist.

Figure 5-4. 50 Pin Video Connector Schematic



5.5 Bracket

Figure 5-5. Recommended Bracket Placement

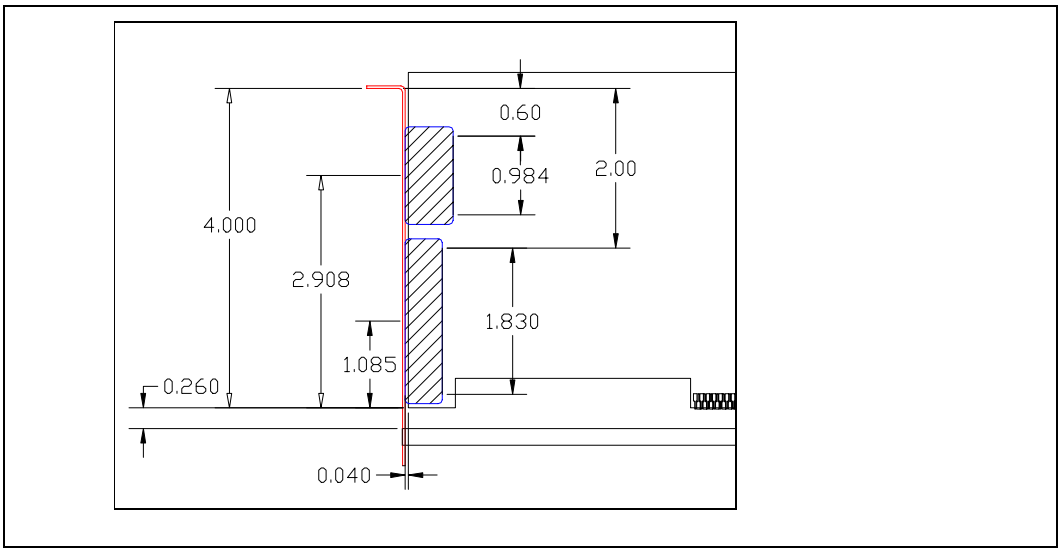
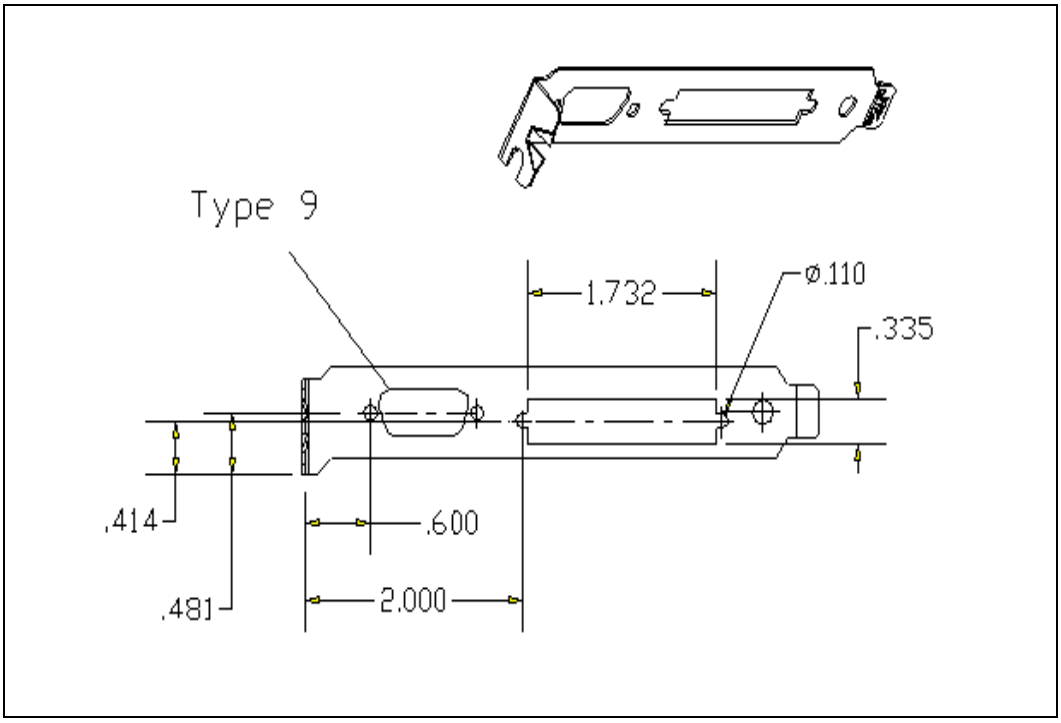


Figure 5-6. Recommended Bracket Cutout



5.6 NLX Considerations

The NLX card has a special bracket design and card cutout to accommodate the NLX chassis. The NLX card can be used in an ATX chassis, but needs to use an ATX bracket. Unless a dual sided board is used, the full featured reference design will not be feasible on the NLX add-in card. This is due to the decreased physical size of the NLX add-in card. The 50 pin video connector will not fit in the NLX chassis. Each board designer must determine the placement of their desired features on the NLX card.

6

Third Party Vendors

Third Party Vendors 6

This chapter provides a useful list of contacts for a design using the Intel740™ graphics accelerator.

6.1 Voltage Regulator

- Linear Technology*
  - Todd Jackson (408) 428-2061

6.2 50 Pin Connector

- Foxconn*
  - P/N QA11253-58

6.3 Fan/Heatsink

- Sanyo Denki*
  - James Sia (310) 212-7724
  - Fan/Heatsink P/N 109P4405H9026
  - Clip, prototype XF-8300
  - Clip, production 109-688

6.4 Flash Components

- Intel
  - 28F010
  - 28F001

6.5 Video Encoders/Decoders

- Rockwell* Semiconductor
  - Tim Yates (619) 535-3522
  - Video Encoder (Bt868/869)
  - Video Decoder (Bt829a)

6.6 DVD Daughter Cards

Intel has worked to enable a variety of hardware DVD solutions. Each of the vendors below will have a functional reference daughter card compatible with the Intel740™ graphics accelerator reference design. These designs can be modified so that the DVD component is down on the card or left as is so that multiple DVD solutions can be implemented.

Depending on the implementation of audio chosen three options exist. One option is to have a software audio solution. This decreases the overall board cost and makes the physical requirements of audio hook-up relatively straight forward. The second option is to have hardware audio and cable this over to the system's sound solution (sound card or motherboard audio). The third option is to use an SPDIF connector to connect to an external SPDIF decoder outside of the chassis.

- C-Cube* Microsystems
  - — Clint Chao (408) 490-8112
- Sigma* Designs
  - — Ron Berti (510) 770-2691
- Toshiba*
  - — Elie Semaan (408) 965-4266
- Zoran*

  Jack Koplik (408) 919-4237

6.7 TV Tuner

- Hauppauge Computer Works, Inc., 91 Cabot Court, Hauppauge, NY 11788
  Phone: (516) 434-1600 Fax: 516-434-3198 Web Site: www.hauppauge.com
  Contact name: Bob Rosoff (brosoff@hauppauge.com)
  - — Model 5901
    4.1x4.2" ISA form-factor NTSC (systems M/N) tuner card. The only contacts on the ISA bus are for power supply. Software includes support for Windows* 95 and Windows* NT.
  - — Model 5904
    4.1x4.2" ISA form-factor PAL (systems B/G) tuner card. The only contacts on the ISA bus are for power supply. Software includes support for Windows95 and Windlassing.
  - — Model 5905
    4.1x4.2" ISA form-factor PAL (system I) tuner card. The only contacts on the ISA bus are for power supply. Software includes support for Windows95 and WindowsNT.
  - — Model 5906
    4.1x4.2" ISA form-factor PAL/SECAM (systems B/G and L) tuner card. The only contacts on the ISA bus are for power supply. Software includes support for Windows95 and WindowsNT.
  - — Model 5907
    4.1x4.2" ISA form-factor PAL/SECAM (systems D/K) tuner card. The only contacts on the ISA bus are for power supply. Software includes support for Windows95 and WindowsNT.

A

Application Notes

Intel740™ Graphics Accelerator

Application Note 653: Thermal Design Considerations

April 1998

Order Number: 292211-002

Contents

Figures

Tables

1.0 Introduction

In a system environment, the chipset temperature is a function of both the system and component thermal characteristics. The system level thermal constraints consist of the local ambient temperature at the component, the airflow over the component and surrounding board as well as the physical constraints at, above, and surrounding the component. The component's case temperature depends on the component power dissipation, size, packaging materials (effective thermal conductivity), the type of interconnection to the substrate and motherboard, the presence of a thermal cooling solution, the thermal conductivity and the power density of the substrate, nearby components, and motherboard.

All of these parameters are pushed by the continued trend of technology to increase performance levels (higher operating speeds, MHz) and packaging density (more transistors). As operating frequencies increase and packaging size decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased emphasis on system design to ensure that thermal design requirements are met for each component in the system.

1.1 Document Goals

The Intel740™ graphics accelerator is the newest addition to the growing market of fast, 3D graphics accelerators. Previous generations of graphics accelerators generated insufficient heat to require an enhanced cooling solution in order to meet the case temperature specifications in system designs. As the market transition to higher-speeds with enhanced features, the heat generated by these advanced graphics accelerators will introduce new thermal challenges for system designers. Depending on the type of system and the chassis characteristics, new designs may be required to provide better cooling solutions for these graphics accelerators. The goal of this document is to provide an understanding of the thermal characteristics of the Intel740 graphics accelerator and discuss guidelines for meeting the thermal requirements imposed on systems.

1.2 Importance of Thermal Management

The objective of thermal management is to ensure that the temperature of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

1.3 Intel740™ Graphics Accelerator Packaging Terminology

BGA	Ball Grid Array. A package type defined by a resin-fiber substrate on which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
Lands	Pads on the PCB where BGA Balls are soldered.
Mold-Cap	The black encapsulating molding compound. The top of this is where maximum case temperatures are taken and where heat sinks are attached.
PCB	Printed Circuit Board.
STBGA	Super Thermal BGA. A Ball Grid Array Package enhanced to improve its thermal characteristics. The Intel740 graphics accelerator uses this type of BGA packaging.
Thermal Balls	Typically, this refers to an array of balls in the center of the larger array of balls which serve to channel heat into the PCB as well as ground connections.

2.0 Thermal Specifications

The Intel740™ graphics accelerator power dissipation can be found in the Intel740™ Graphics Accelerator Datasheet and Intel740™ Graphics Accelerator Specification Updates. Please refer to these documents to verify the actual thermal specifications for the Intel740 graphics accelerator. In general, systems should be designed to dissipate the highest possible thermal power.

To ensure proper operation and reliability of the Intel740 graphics accelerator, the thermal solution must maintain the case temperature at or below its specified value (Table 1). Considering the power dissipation levels and typical system ambient environments of 45°C to 55°C, if the Intel740 graphics accelerator case temperature exceeds the maximum case temperature listed in Table 1, system or component level thermal enhancements will be required to dissipate the heat generated.

The thermal characterization data described in later sections illustrates that good system airflow is critical. In typical systems the thermal solution is limited by board layout, spacing and component placement. Airflow is determined by the size and number of fans and vents along with their placement in relation to the components and the airflow channels within the system. In addition, acoustic noise constraints may limit the size and/or types of fans and vents that can be used in a particular design.

To develop a reliable, cost-effective thermal solution, all of the above variables must be considered. Thermal characterization and simulation should be carried out at the entire system level accounting for the thermal requirements of each component.

Table 1. Intel740 Graphics Accelerator Preliminary Thermal Absolute Maximum Rating

Parameter	Maximum
$T_{case\text{-}nhs}$1	109°C
$T_{case\text{-}hs}$2	96°C

NOTES:
1. $T_{case\text{-}nhs}$ is defined as the maximum case temperature without a Heat Sink attached.
2. $T_{case\text{-}hs}$ is defined as the maximum case temperature with a Heat Sink attached (see Section 4.2, “Thermal Enhancements” on page 10).

2.1 Case Temperature

The case temperature is a function of the local ambient temperature and the internal temperature of the Intel740graphics accelerator. As a local ambient temperature is not specified for the Intel740, the only restriction is that the maximum case temperature (T_{case}) is not exceeded. Section 5.1, “Case Temperature Measurements” on page 19 discusses proper guidelines for measuring the case temperature.

Note: Increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature.

2.2 Power

In previous generations of graphics accelerators where Quad Flat Pack (QFP) packages have been the primary package type, the majority of power dissipation has been through the plastic case of the package into the surrounding air. With the advent of Ball Grid Array (BGA) packaging for graphics accelerators, the majority of the thermal power dissipated by the chipset typically flows into the motherboard where it is mounted. The remaining thermal power is dissipated by the package itself. The STBGA used for the Intel740 graphics accelerator continues this trend by further enhancing the package's ability to channel heat into the motherboard.

The amount of thermal power dissipated, either into the board or by the package, varies depending on how well the motherboard conducts heat away from the package and whether the package uses thermal enhancements. While package thermal enhancements typically serve to improve heat flow through the case via a heat sink, how well the motherboard conducts heat away from the package is strictly a function of motherboard design. The following should be taken into account by system designers when developing new systems:

- How well the thermal balls are connected to the inner planes of the motherboard. It is recommended that:
  - — One via per ground ball be used.
  - — Minimum width of the trace connecting the motherboard ground pad to the via be 10 mil.
  - — Plated Via Size for ground balls be 14 to 16 mil in diameter on a 24 to 27 mil pad. A larger via is more efficient in channeling heat.
  - — Do not use Thermal Relief Patterns on the inner plane connections of the thermal balls.
- How well the inner planes conduct heat away from the package. Good ground paths to other areas of the board will distribute heat more efficiently.
- The size of the motherboard, number of copper layers and the thickness of those layers.

3.0 Designing for Thermal Performance

In designing for thermal performance, the goal is to keep the component within the operational thermal specifications. The heat generated by the components within the chassis must be removed to provide an adequate operating environment for all of the system components. To do so requires moving air through the chassis to transport the heat generated out of the chassis.

3.1 Airflow Management

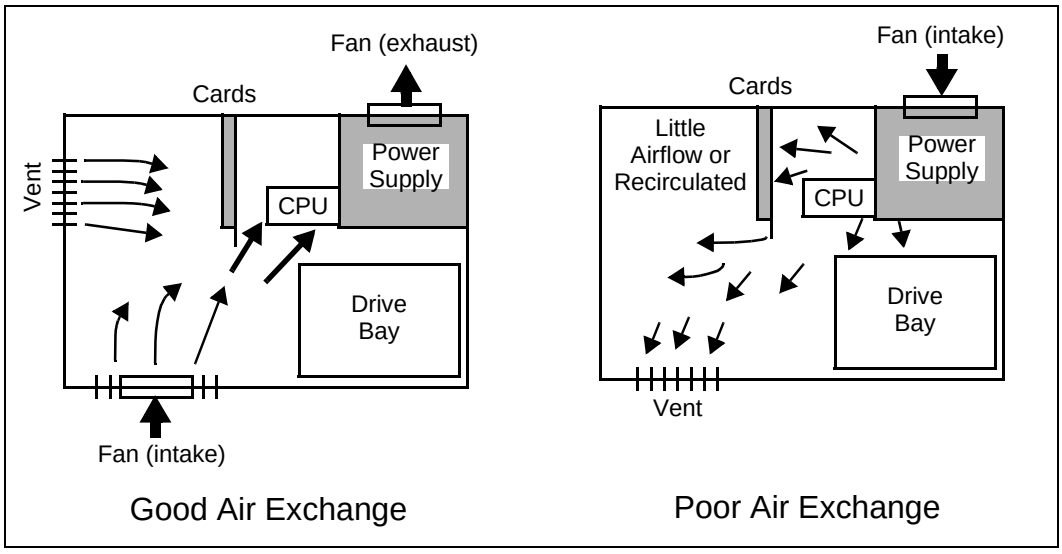
It is important to manage the air flow path and amount of air that flows through the system to maximize the amount of air that will flow over the Intel740 graphics accelerator and AGP Card. System air flow can be increased by adding one or more fans to the system, by vents and fans in combination, by increasing the output (faster speed) or size of an existing system's fan(s). Local air flow can also be increased by managing the local flow direction using baffles or ducts. An important consideration in airflow management is the temperature of the air flowing over the graphics processor. Heating effects from add-in boards, memory, other accelerators and disk drives greatly reduce the cooling efficiency of this air, as does re-circulation of warm interior air. Care must be taken to minimize the heating effects of other system components and to eliminate excessive warm air re-circulation.

For example, a clear air path from the external system vents to the system fan(s) will enable the warm air from the Intel740 graphics accelerator and AGP Card to be efficiently removed from the system. If no air path exists across the them, the warm air ambient to the Intel740 graphics accelerator and AGP Card will not be removed from the system, resulting in localized heating ("hot spots") at and around the graphics processor requiring the addition of a thermal cooling device. Figure 1 shows two examples of air exchange through a PC-ATX style chassis. The system on the left is an example of good air exchange incorporating both the power supply fan, an additional system fan and good venting. The system on the right shows a system with only a power supply fan (blowing into the box) and minimal venting resulting in poor air flow past the AGP card.

Re-circulation of internal warm air is most common between the system fan and chassis, between the system fan intake and the drive bays behind the front bezel and in the card area. These paths may be eliminated by mounting the fan flush to the chassis, thereby obstructing the flow between the drive bays and fan inlet, and by providing generous intake vents in both the chassis and the front bezel.

Note: Note that these are recommendations. With careful engineering, modeling and testing, other solutions may work equally well in cooling the system.

Figure 1. Example of air exchange through a PC chassis



4.0 Cooling Solutions

Numerous alternatives for cooling solutions exist for the Intel740 graphics accelerator. This section will explore system cooling solutions as well as package heat-sinks. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.

4.1 System Fans

Fans are needed to move the air through the chassis. The airflow rate of a fan is a function of the system's impedance to airflow and the capability of the fan itself. Maximum acceptable noise levels may limit the fan output or the number of fans selected for a system. It is appropriate at this time to reiterate Section 2.2, "Power" on page 4. The majority of the thermal power dissipated by the Intel740 graphics accelerator typically flows into the motherboard to which it is mounted. Cooling the motherboard will cool the component by increasing the efficiency of heat transfer from the device to the motherboard.

4.1.1 Fan Placement

Proper placement of the fans can ensure that the Intel740 graphics accelerator is properly cooled. Because of the difficulty in building, measuring and modifying a mechanical assembly, models are typically developed and used to simulate a proposed prototype for thermal effectiveness to determine the optimum location for fans and vents within a chassis. Prototype assemblies can also be built and tested to verify if thermal specifications for the system components are met.

An air fan is typically in the power supply exhausting air through the power supply vents. A second system fan is added to improve airflow to the chipset and other system components. The second fan can improve component cooling up to 15% depending on airflow management within the system, obstructions and thermal enhancements. Figure 2 and Figure 3 show recommended fan placements for an ATX form factor layout and a NLX form factor, respectively. Again, note that these are recommendations, with careful engineering, modeling and testing, other solutions may work equally well in cooling the graphics processor.

Figure 2. Fan Placement and Layout of an ATX Form Factor Chassis - Top View

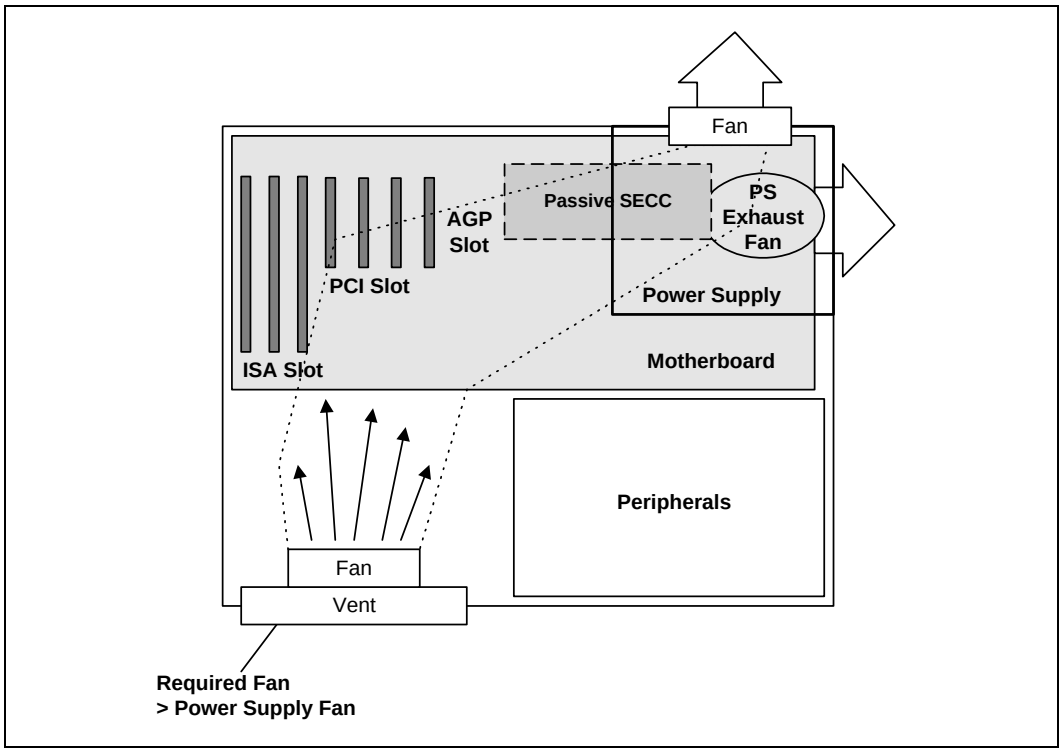
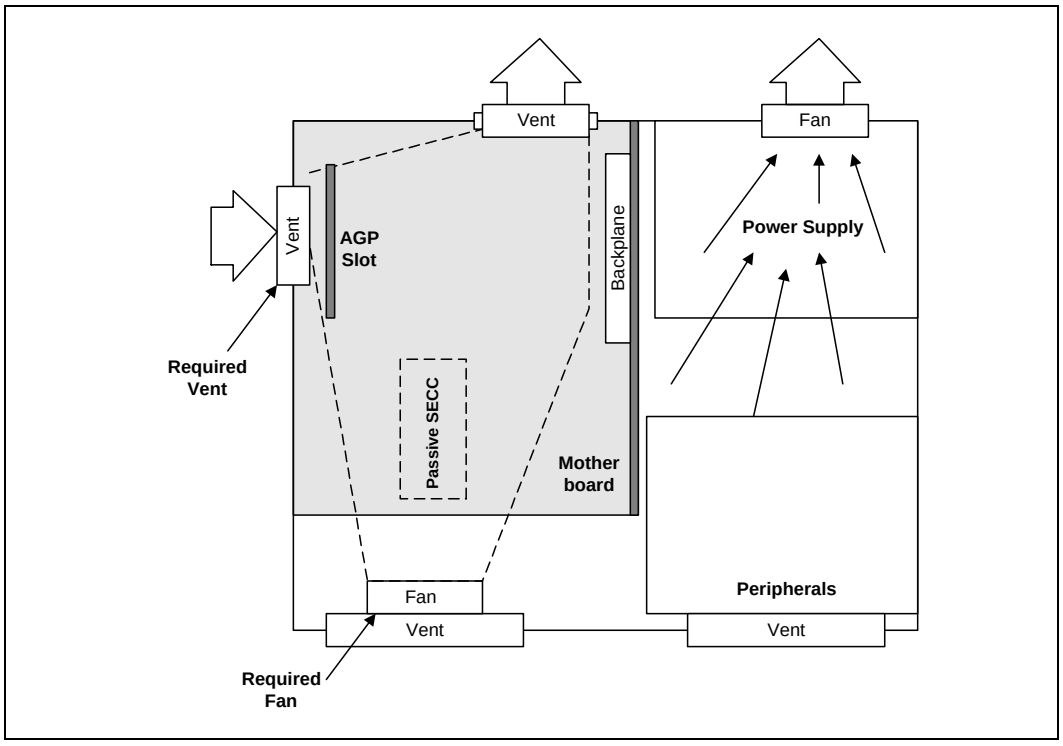


Figure 3. Fan Placement and Layout of an NLX Form Factor Chassis - Top View



4.1.2 Fan Direction

If the fan(s) are not moving air across the graphics processor and the card then little cooling can occur. Hence, the Intel740 graphics accelerator may exceed it's absolute maximum thermal ratings. Note the recommended fan airflow directions in Figure 2 and Figure 3.

The direction of the air flow can also be modified with baffles or ducts to direct the air flow over the graphics processor. This will increase the local flow over the device and card and may eliminate the need for a larger or higher speed fan.

4.1.3 Size and Quantity

A larger fan does not always increase cooling efficiency. A small blower using ducting might direct more air over the graphics card than a larger fan blowing non-directed air. The following provides some recommendations for the size and quantity of the fans in AGP systems.

- The fan should be a minimum of 80 mm (3.150") square, with a minimum airflow of approximately 40 CFM (cubic feet per minute), or approximately 400 LFM (linear feet per minute). As shown in Figure 2 and Figure 3, two fans are used. The intake air fan blows cooler external air into the chassis, while the second fan (most likely in the power supply) exhausts the air out of the system.
- As an example, in a lab test system, graphics card ambient temperatures were reduced by an average of roughly 10% in an ATX design and 15% in an NLX design by simply adding a front system fan. In general, the use of two fans benefits the entire system by reducing internal ambient temperatures. However, as system configurations vary, testing the target configuration to verify the benefit is recommended.

4.1.4 Fan Venting

As shown in Figure 2 and Figure 3, intake venting should be placed at the front (user side) of the system. Location should take into consideration cooling of the microprocessor and peripherals as well as the Intel740 graphics accelerator. A good starting point would be the lower 50% of the Front Panel (Bezel). Intake venting directly in front of the intake fan is the most optimal location.

4.1.5 Vent Placement

In most cases, exhaust venting in conjunction with an exhaust fan in the power supply is sufficient. However, depending on the number, location and types of add-in cards, intake or exhaust venting may be necessary near the cards as well. This is particularly important for the graphics card in NLX designs as it aids in eliminating dead air space near the AGP Slot (see Figure 3).

Vent placements should be modeled or prototyped for the optimum thermal potential. Hence, a system should be modeled for the worst case (i.e., all expansion slots should be occupied with typical add-in options).

4.1.5.1 Vent Area/Size

The area and/or size of the intake vents should consider the size and shape of the fan(s). Adequate air volume must be obtained and this will require appropriately sized vents. Intake vents should be located in front of the intake fan(s) and adjacent to the drive bays. Venting should be approximately 50% to 60% open in the EMI containment area due to EMI constraints. Outside the EMI containment area, the open percentage can be greater if needed for aesthetic appeal (i.e., bezel/cosmetics). For more information concerning EMI constraints and Pentium II processor based system design, see the *Pentium II Processor EMI Design Guidelines* Application Note.

4.1.5.2 Vent Shape

Round, staggered pattern openings are best for EMI containment, acoustics and airflow balance. For material related to EMI considerations please see the *Pentium II Processor EMI Design Guidelines* Application Note.

4.1.6 Ducting

Ducts can be designed to isolate components from the effects of system heating and to maximize the thermal budget. Air provided by a fan or blower could be channeled directly over the Intel740 graphics accelerator and card or split into multiple paths to cool multiple components.

4.1.6.1 Ducting Placement

When ducting is to be used, it should direct the airflow evenly from the fan across the entire component and surrounding motherboard. The ducting should be accomplished, if possible, with smooth, gradual turns as this will enhance the airflow characteristics. Sharp turns in ducting should be avoided. Sharp turns increase friction and drag and will greatly reduce the volume of air reaching the Intel740 graphics accelerator and card.

4.2 Thermal Enhancements

One method used to improve thermal performance is to increase the surface area of the device by attaching a metallic heat sink to the mold cap. To maximize the heat transfer, the thermal resistance from the heat sink to the air can be reduced by maximizing the surface area of the heat sink itself.

For users whose ambient environments exceed 55°C, a Fan Heat Sink is strongly recommended to effectively cool the Intel740 graphics accelerator (discussed in Section 4.2.2, “Low Profile Fan Heat Sink” on page 11).

Note: Increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature.

4.2.1 Clearance

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the constraints typically placed on the Intel740 graphics accelerator by an adjacent PCI Card is 0.450” clearance between the Intel740 graphics accelerator mold cap and the back of the adjacent PCI Card.

Note: If the heat sink selected is larger than 35 mm x 35 mm, the maximum component height under the portion of the heat sink overhaning the board is 0.09 inches.

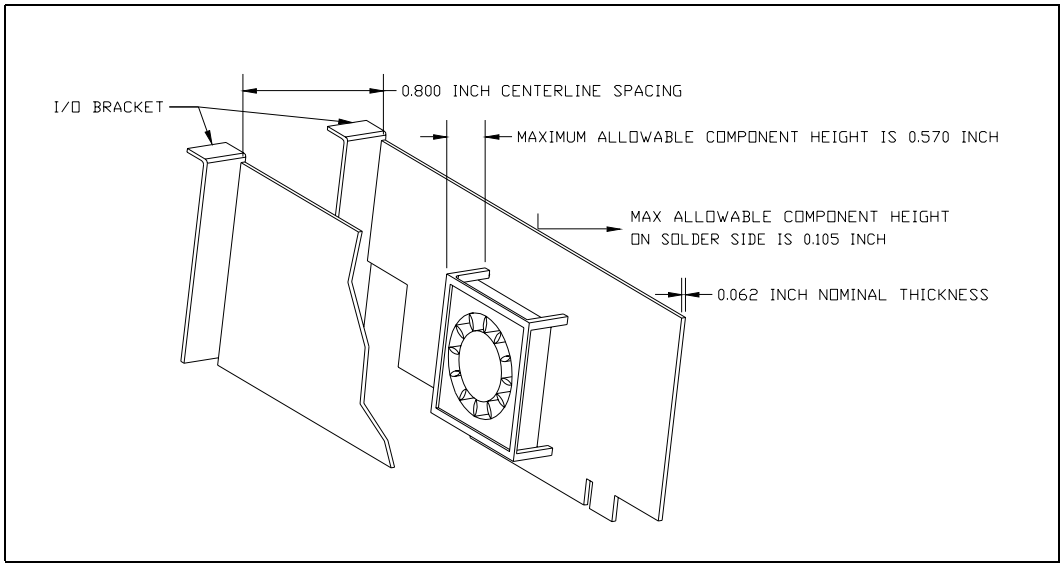
4.2.2 Low Profile Fan Heat Sink

A generic drawing for this Fan Heat Sink is shown in Figure 4. Recommended sources for the Low Profile Fan Heat Sink are discussed in Appendix A, “Sources”.

The thermal performance of the Fan Heat Sink and Thermal Interface Material (combined) must be sufficient to maintain a case temperature at or below $T_{case\text{-}hs}$ (See Table 1) in a worst case system environment (defined as: zero airflow, 55°C ambient temperature).

Note: The weight of the Fan Heat Sink must not exceed 55 gm.

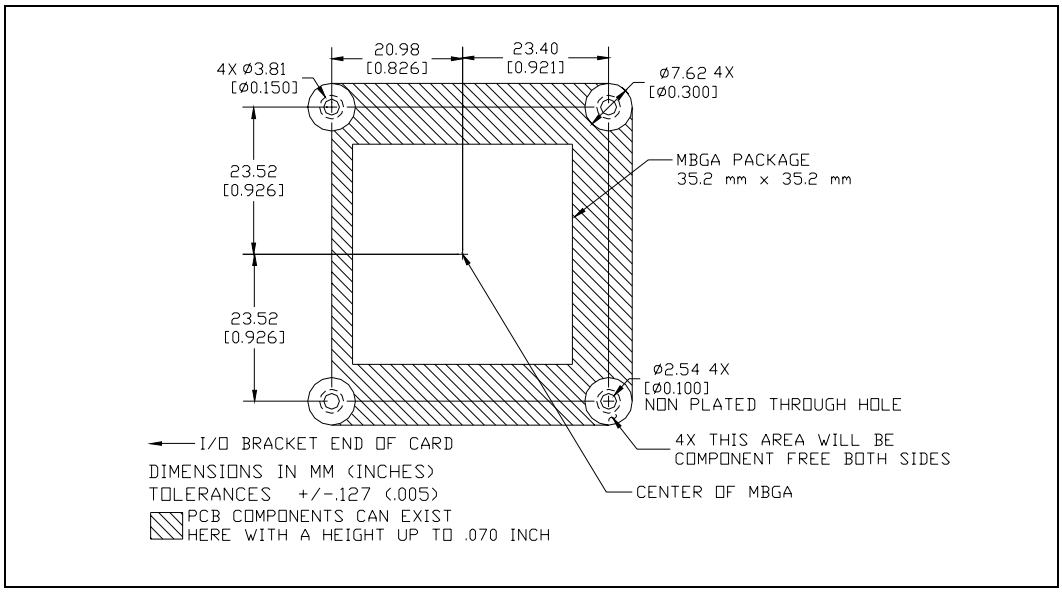
Figure 4. Low Profile Fan Heat Sink Drawing



4.2.2.1 Low Profile Fan Heat Sink PCB Layout Guidelines

As the Low Profile Fan Heat Sink uses a mechanical attach, mounting holes must be provided in the PCB to accommodate the clips necessary in attaching the Fan Heat Sink. PCB Guidelines for the Fan Heat Sink mounting hole layout are provided in Figure 5. The mounting holes must be non-plated, but each must have a grounding pad on the solder side of the board surrounding the hole. It must be designed in such a way to ensure that the mechanical attachment clip is in solid contact with this pad. The mechanical assembly should only contact the PCB within the four 0.300 inch diameter component keep-out zones as shown in Figure 5. The outline of the Fan Heat Sink should be silk-screened onto the PCB to facilitate placement of the Fan Heat Sink on to the package.

Figure 5. PCB Layout Guidelines for Mounting Holes



4.2.2.2 Low Profile Fan Heat Sink Electrical Requirements

The Fan Heat Sink's total maximum power usage should not exceed 1 Watt and should start and operate within ±10% of rated voltage.

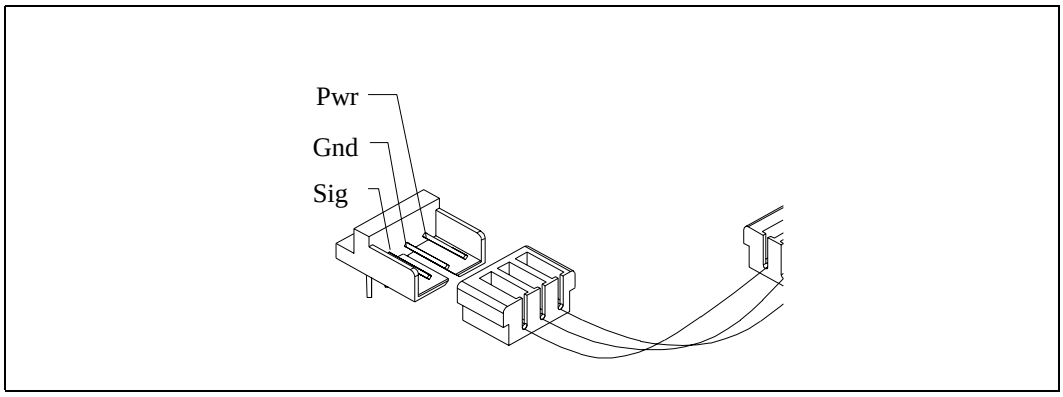
The Fan Heat Sink may use a connector which incorporates 2 separate connections: 12 Volt power, ground and signal (tachometer function). The fan connector may mate with a receptacle attached to a power cable that will be installed by the graphics card manufacturer. See Figure 5.

The Fan Heat Sink assembly, when installed in at least one typical host application, should not cause an increase in emissions above that measured from the host application before the assembly was installed.

The signal pin on fan header may supply an open collector rotor lock output signal:

- Operating: Output is asserted by pulling the output low
- Locked Rotor: Output is de-asserted, allowing output to float high using a pull up resistor on the graphics card.

Figure 6. Fan Heat Sink Connector Design



4.2.2.3 Low Profile Fan Heat Sink Attach

The Low Profile Fan Heat Sink uses a mechanical attach to the card in conjunction with a thermal interface material. The recommended process flow for attaching the Low Profile Fan Heat Sink is shown as follows:

1. Ensure that the surface of the component and heat sink are free from contamination. Use a clean, lint-free wipe, proper safety precautions and Isopropyl Alcohol to ensure cleanliness.
2. Apply the Thermal Interface Material to the moldcap.
3. Place the Fan Heat Sink onto the moldcap within the confines of the silkscreened markings on the board.
4. Apply the mechanical attachment clip.

To repeat, the Thermal Performance of the Fan Heat Sink and Attach (combined) must be a maximum of 4.0°C per Watt at 80% of nominal fan RPM in a worst case system environment (defined as: zero airflow, 55°C internal ambient temperature).

4.2.2.4 Low Profile Fan Heat Sink Reliability

As every motherboard, system, heat sink and attach-process combination may introduce variance in attach strength and the use of a fan heat sink adds the need for fan-lifetime evaluation, it is generally recommended that the user carefully evaluate the reliability of the completed assembly prior to use in high volume. Some Test recommendations can be seen in Table 2.

Table 2. Default Thermal Solution Reliability Validation

Test[1]	Requirement	Pass/Fail Criteria
Mechanical Shock	50G 11 msec, 3 shocks/direction	Visual Check [3] RPM Check [4]
Random Vibration	7.3 G 45 minutes/axis, 50 to 2000 Hz	Visual Check RPM Check
Temperature Life	85 °C, 2000 hours total, checkpoints occur at 168, 500, 1000 and 2000 hours	Visual Check RPM Check
Thermal Cycling	-5 °C to +70 °C 500 Cycles	Visual Check RPM Check

Table 2. Default Thermal Solution Reliability Validation

Humidity	85% relative humidity 55 °C, 1000 hours	Visual Check RPM Check
Power Cycling	7,500 on/off cycles with each cycle specified as 3 minutes on, 2 minutes off 70 °C	Visual Check RPM Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 Fan Heat Sink units from 3 assembly lots.
2. Visual Check: Labels, housing and connections all intact.
3. RPM Check: No fan RPM changes before and after test of greater than 20%.
4. The Fan Heat Sink's thermal performance should meet the minimum specified requirements at an altitude of 1 to 10,000 feet.
5. Additional Pass/Fail Criteria may be added at the discretion of the user.

4.2.3 Low Profile Passive Heat Sink

A Passive, Extruded Heat Sink may be attached using Clips and Thermal Interface (tape, grease, etc.), Epoxy or Tape Adhesives. Suggested suppliers and part numbers for a passive heat sink are listed in Section A, "Sources" on page 23.

4.2.3.1 Clip Attach

A well designed clip in conjunction with a thermal interface material (tape, grease, etc.) solution may offer the best combination of mechanical stability and reworkability. Use of a clip requires significant advance planning as mounting holes are required in the PCB. The mounting holes should be non-plated, but each must have a grounded annular ring on the solder side of the board surrounding the hole. For a typical low-cost clip, this annular ring should have an inner diameter of 150 mils and an outer diameter of 300 mils. This ring should contain at least 8 ground connections. The solder mask opening for these holes should have a radius of 300 mils.

As clip designs are generally unique to a specific system and board layout, no procedural comments are provided.

4.2.3.2 Epoxy

Some users may prefer to implement Epoxy attaches for their thermal solution. For these users, products known to be compatible with the mold cap material are listed in Appendix A. Epoxy users should plan their process carefully as once attached, the heat sink may be difficult or impossible to remove without damaging the component.

For the Epoxies described in Section A, "Sources" on page 23, the manufacturer's recommended attach procedure is as follows:

1. Ensure that the surface of the component and heat sink are free from contamination. Use a clean, lint-free wipe, proper safety precautions and Isopropyl Alcohol to ensure cleanliness.
2. Use the applicator provided by the epoxy manufacturer to apply the epoxy-activator to the mold-cap.
3. After the activator-solvent evaporates, the active ingredients will appear "wet" and will remain active for a maximum of two hours after application**. Contamination of the surface during this time prior to bonding must be avoided.**
4. Apply the adhesive to the heat sink. The amount of adhesive applied to the heat sink should be limited to the amount necessary to fill the bond and provide a small fillet (see Section 4.3.1, "Bond Line Management" on page 18).

5. Join and secure the assembly centering the heat sink on the component. Wait for the adhesive to fixture (approximately 5 minutes) before any further handling. Full cure occurs in 4-24 hours.

Note: The successful application of this product depends on accurate dispensing on to the parts being bonded. The manufacturer (Section A, "Sources" on page 23) offers equipment engineers to assist customers in selecting and implementing the appropriate dispensing equipment for various applications.

To remove the heat sink after the epoxy has set, the manufacturer recommends applying heat (70°C - 93°C) to the assembly. When in this temperature range the heat sink can safely be removed from the component without damaging it.

4.2.3.3 Tape Attach

For users who prefer to attach via Tape, please refer to Section A, "Sources" on page 23 for the suggested manufacturer and part number. To maximize the bond line contact area and improve adhesion we recommend using two pieces of tape, one attached to the heat sink and one attached to the moldcap as shown in Figure 7, Figure 8, and Figure 9. The recommended attach procedure is at the end of this section.

Figure 7. Tape Layers

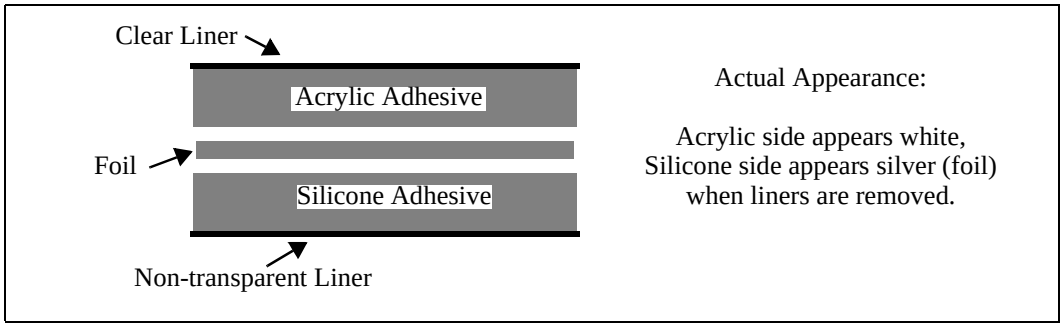


Figure 8. Attaching the Tape to the Package and Heat Sink

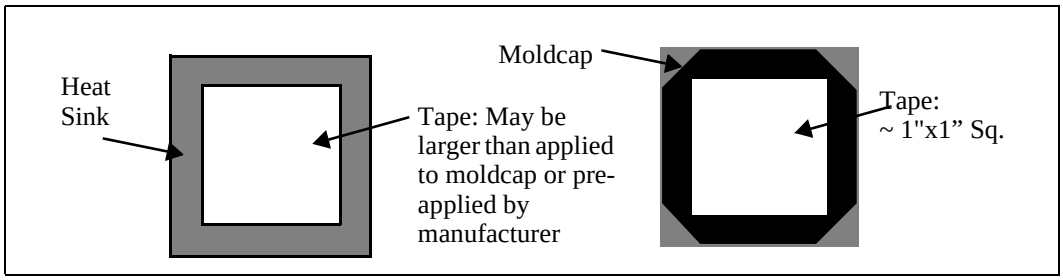
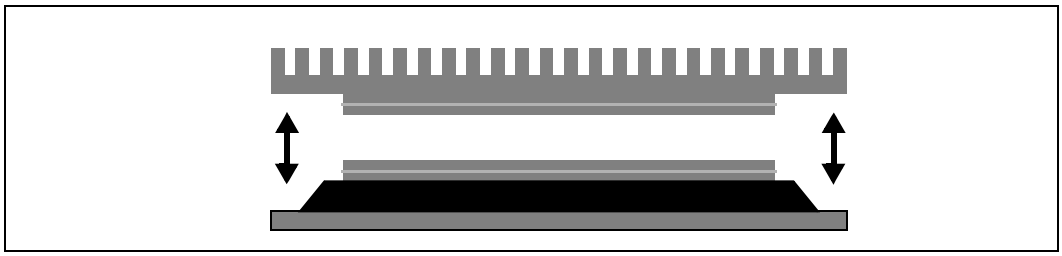


Figure 9. Completing the Attach Process



Note: Silicone Adhesive always joins to either the heat sink or the moldcap, the Acrylic Adhesive sides must join to each other (Figure 9).

Note: As every motherboard, system and heat sink combination may introduce variance in attach strength, it is generally recommended that the user carefully evaluate the reliability of tape attaches prior to using in high volume.

For the Tape described in Appendix A, "Sources," the recommended two-piece attach procedure is as follows:

1. Ensure that the surface of the component and heat sink are free from contamination. Use a clean, lint-free wipe, proper safety precautions and Isopropyl Alcohol to ensure cleanliness.
2. Cut tape to size. Suggestions for the appropriate size can be seen in Figure 8.
3. Heat Sink Side: Remove the non-transparent liner. You will see foil underneath (Figure 7). Apply the tape to the center of the heat sink and smooth over the entire surface using moderate pressure. **There should be no air bubbles under the tape.**
4. Component Side: Remove the non-transparent liner. You will see foil underneath (Figure 7). Apply the tape to the center of the mold cap and smooth over the entire surface using moderate pressure. **There should be no air bubbles under the tape.**
5. Both Sides: Remove the clear liners from each side, center the heat sink over the component and apply using any one of the manufacturer's recommended temperature/pressure options shown in Table 3.

Table 3. Tape Attach Application Temperature/Pressure Option

Pressure	Temperature	Time
10 psi (0.069 mPa)	22°C	15 seconds
30 psi (0.207 mPa)	22°C	5 seconds
10 psi (0.069 mPa)	50-65°C	5 seconds
30 psi (0.207 mPa)	50-65°C	3 seconds

NOTE: Approximately 70% of the ultimate adhesion bond strength is achieved with initial application, 80-90% of the ultimate adhesion bond is achieved within 15 minutes and ultimate adhesion strength is achieved within 36 hours.

4.2.3.4 Reliability

As every motherboard, system, heat sink and attach-process combination may introduce variance in attach strength, it is generally recommended that the user carefully evaluate the reliability of the completed assembly prior to use in high volume. Some Test recommendations can be shown in Table 4.

Table 4. Reliability Validation

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	50G, board level 11 msec, 3 shocks/direction	Visual Check
Random Vibration	7.3 G, board level 45 minutes/axis, 50 to 2000 Hz	Visual Check
Temperature Life	85°C, 2000 hours total, checkpoints occur at 168, 500, 1000 and 2000 hours	Visual Check
Thermal Cycling	-5°C to +70°C 500 Cycles	Visual Check
Humidity	85% relative humidity 55°C, 1000 hours	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

4.3 Thermal Interface Management for Heat Sink Solutions

For solutions where a heat sink is preferred, to optimize the heat sink design for Intel740 graphics accelerator, it is important to understand the impact of factors related to the interface between the mold-cap and the heat sink base. Specifically, the bond line thickness, interface material area and interface material thermal conductivity should be managed to realize the most effective heat-sink solution.

4.3.1 Bond Line Management

The gap between the mold-cap and the heat sink base will impact heat-sink solution performance. The larger the gap between the two surfaces, the greater the thermal resistance. The thickness of the gap is determined by the flatness of both the heat sink base and the mold-cap, plus the thickness of the thermal interface material (e.g., PSA, thermal grease, epoxy) used between these two surfaces.

The Intel740 graphics accelerator mold cap planarity is specified as 0.006 inches maximum (see the Intel740™ Graphics Accelerator Datasheet, order number 290618, for package drawing).

4.3.2 Interface Material Performance

Two factors impact the performance of the interface material between the thermal plate and the heat sink base:

- Thermal resistance of the material
- Wetting/filling characteristics of the material

Thermal resistance is a description of the ability of the thermal interface material to transfer heat from one surface to another. The higher the thermal resistance, the less efficient an interface is at transferring heat. The thermal resistance of the interface material has a significant impact on the thermal performance of the overall thermal solution. The higher the thermal resistance, the higher the temperature drop across the interface and the more efficient the thermal solution must be.

The wetting/filling of the thermal interface material is its ability to fill the gap between the case and the heat-sink. Since air is an extremely poor thermal conductor, the more completely the interface material fills the gaps, the lower the temperature drop across the interface.

5.0 Measurements for Thermal Specifications

To appropriately determine the thermal properties of the system, measurements must be made. Guidelines have been established for the proper techniques to be used when measuring the Intel740 graphics accelerator case temperatures. Section 5.1, "Case Temperature Measurements" on page 19 provides guidelines on how to accurately measure the case temperature of the Intel740 graphics accelerator. Section 5.2, "Power Simulation Software" on page 20 contains information on running an application program which will emulate anticipated thermal design power. The flowchart in Figure 12 as well as Section 4.2, "Thermal Enhancements" on page 10 offer useful guidelines for performance and evaluation.

5.1 Case Temperature Measurements

To ensure functionality and reliability, the Intel740 graphics accelerator is specified for proper operation when T_{case} (case temperature) is maintained at or below the maximum case temperatures listed in Table 1. The surface temperature of the case in the geometric center of the mold cap is measured. Special care is required when measuring the T_{case} temperature to ensure an accurate temperature measurement.

Thermocouples are often used to measure T_{case}. Before any temperature measurements are made, the thermocouples must be calibrated.

When measuring the temperature of a surface which is at a different temperature from the surrounding local ambient air, errors could be introduced in the measurements. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation, convection, by conduction through thermocouple leads, or by contact between the thermocouple cement and the heat-sink base for those solutions which implement a heat-sink. To minimize these measurement errors, the following approach is recommended:

Attaching the Thermocouple

- Use 36 gauge or smaller diameter K type thermocouples.
- Ensure that the thermocouple has been properly calibrated.
- Attach the thermocouple bead or junction to the top surface of the package (case) in the center of the mold-cap using high thermal conductivity cements. An alternative for tape attach users is to use the tape itself to mount the thermocouple. **It is Critical that the thermocouple be intimately attached across the entire moldcap.**
- The thermocouple should be attached at a 0° angle if there is no interference with the thermocouple attach location or leads (refer to Figure 10). This is the preferred method and is recommended for use with both unenhanced packages as well as packages employing Thermal Enhancements.
- For solutions where a heat-sink is preferred, the thermocouple should be attached at a 90° angle if a heat sink is attached to the case and the heat sink covers the location specified for T_{case} measurement (refer to Figure 11).
- The hole size through the heat sink base to route the thermocouple wires out should be smaller than 0.150" in diameter.
- Make sure there is no contact between the thermocouple cement and heat sink base. This contact will affect the thermocouple reading.

Figure 10. Technique for Measuring T_{case} with 0° Angle Attachment

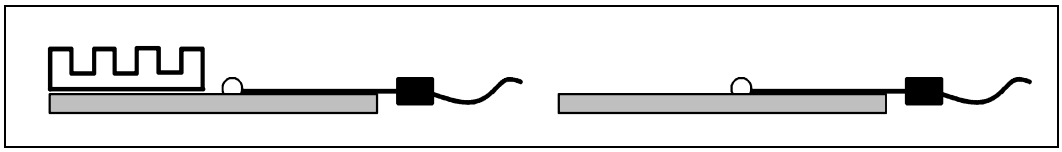
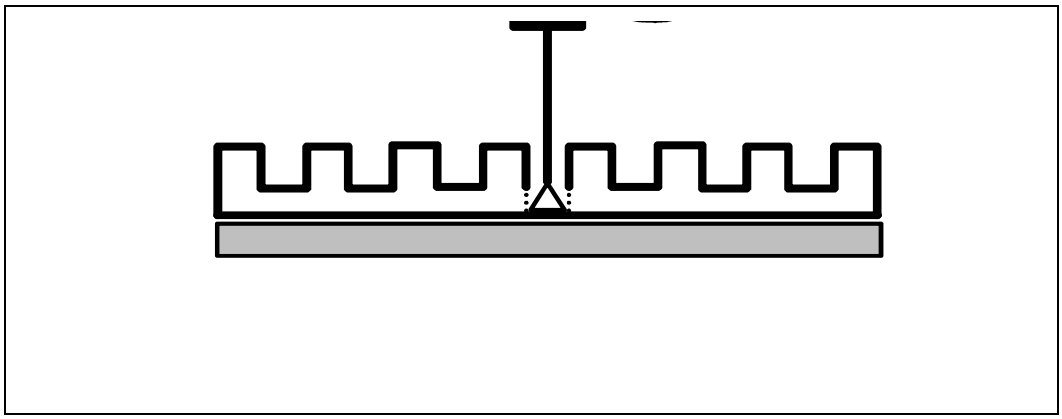


Figure 11. Technique for Measuring T_{case} with 90° Angle Attachment



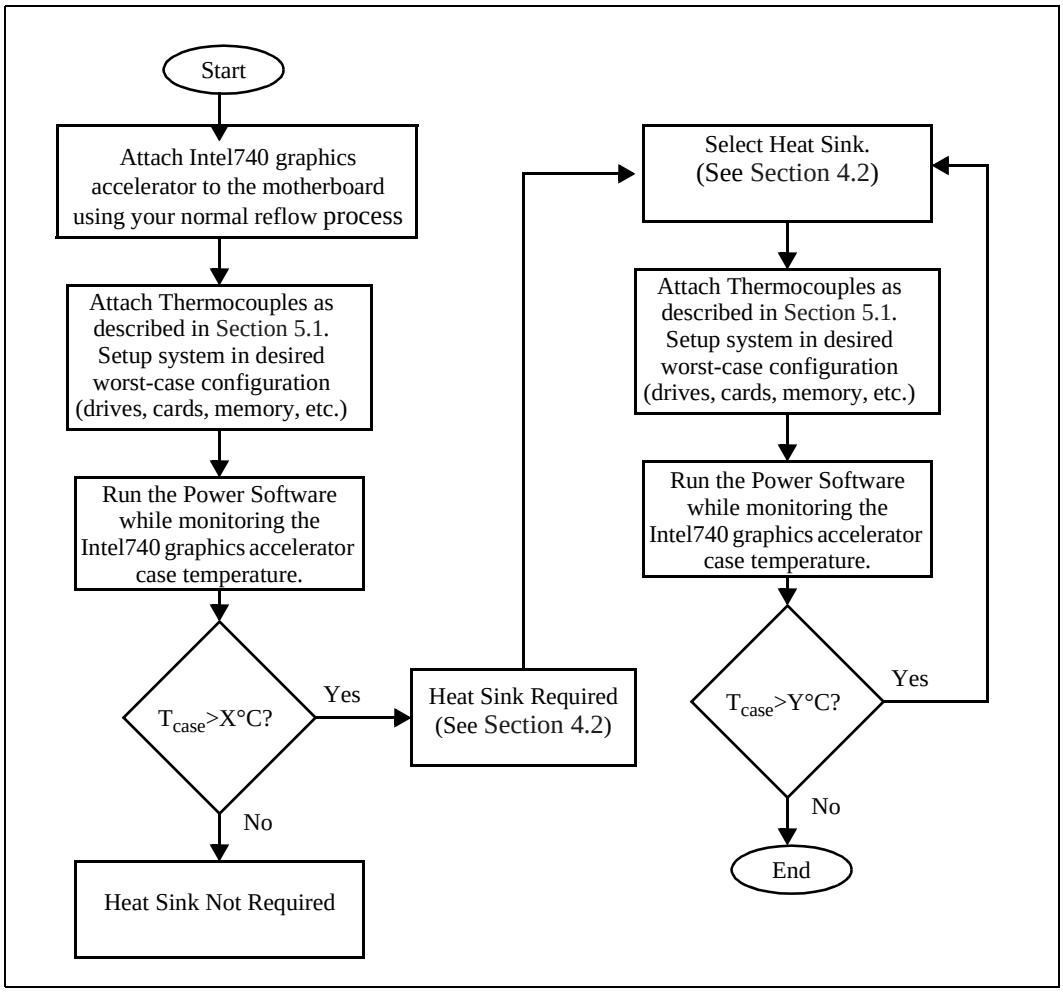
5.2 Power Simulation Software

The power simulation software for the Intel740 graphics accelerator is a utility designed to stress the thermal design power for an Intel740 graphics accelerator when used in conjunction with a Pentium II processor. The combination of the Pentium II processor along with the high bandwidth capability of the new enables new levels of graphics performance which are not utilized in most current software applications. However, it is conceivable that new applications and drivers will be written which take advantage of this increased bandwidth. To ensure the thermal performance of the Intel740 graphics accelerator while running future applications, Intel has developed a software utility which emulates this anticipated power dissipation.

The power simulation software has been developed only for testing Thermal Design Power. Real future applications may exceed the Thermal Design Power limit for transient time periods. For power supply current requirements under these transient conditions, please refer to the *Intel740 Graphics Accelerator Datasheet* for $I_{CC-740,}$ the Power Supply Current (Max) specification.

Note: Please contact your local Intel representative for more information about the Intel740™ Graphics Accelerator Power Simulation Software.

Figure 12.Thermal Enhancement Decision Flowchart



Note: For the latest values of "X°C" and "Y°C", refer to the Power Simulation Software User Guide.

6.0 Conclusion

As the complexity of today's graphics accelerators continues to increase, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting and/or passive heat sinks.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans and ducts. When additional cooling is required, thermal enhancements in conjunction with enhanced system cooling. The size of the fan or heat sink can be varied to balance size and space constraints with acoustic noise. This document has presented the conditions and requirements for properly designing a cooling solution a system implementing the Intel740 graphics accelerator. Properly designed solutions provide adequate cooling to maintain the Intel740 graphics accelerator case temperature at or below those listed in Table 1. This is accomplished by providing a low local ambient temperature and creating a minimal thermal resistance to that local ambient temperature. By maintaining the Intel740 graphics accelerator case temperature at or below those recommended in this document, a system will function properly and reliably.

Appendix A Sources

A.1 Low Profile Fan Heat Sink Sales Locations

Sanyo Denki	Please visit WEB at http://www.sanyodenki.co.jp/profile_e17.html
Future Second Source	Panasonic
Part Numbers	
Sanyo Denki	109P4405H9026

A.2 Low Profile Passive Heat Sink Sales Locations

Thermalloy	please visit WEB at: http://www.thermalloy.com
JME	please visit WEB at: http://www.jme.com
Part Numbers	
Thermalloy	2522B
JME:	HAA740BBXXB-001 (with 1-layer Chomerics T410)
	HAA740BBXXX-001 (without attach)

A.3 Attach Sales Locations

For Epoxy	please visit WEB: http://www.loctite.com Select the country of your choice and Select Products for the Electronics Industry.
For Tape	please visit WEB: http://www.chomerics.com/locate
Part Numbers	
Loctite Epoxy	Part Numbers 383 or 384
Chomerics Tape	T-410

UNITED STATES AND CANADA
Intel Corporation
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Intel740™ Graphics Accelerator

Application Note: 3 Device AGP System BIOS Design Guidelines

August 1998

Order Number: 290628-001

Contents

Figures

Tables

1.0 Introduction

For the 3 Device AGP down motherboard design discussed in the Intel740™ Graphics Accelerator Design Guide, Rev 3 (order number 290619), both the video BIOS and support for the 3 Device AGP low power logic must be integrated into the system BIOS. This document details the needed changes to system BIOS to implement the low power logic. Details to incorporate the video BIOS in the system BIOS is beyond the scope of this document.

The on-board AGP device and the AGP add-in card will not be active simultaneously. If an add-in card is present in the AGP slot, the on-board AGP graphics device remains disabled. The system BIOS will provide support for single monitor or multimonitor configurations with or without an AGP graphic device active. The latter is achieved through a CMOS option that will allow the end user, system integrator, or OEM to manually disable the on board Intel740 chip and bypass any enabling events.

2.0 Low Power Mode Overview

Two signals, GPO27# and GPO28#, from the PIIX4E are used in this design. These GPOx signals must be asserted by the system BIOS.

GPO28# is needed to put the Intel740 chip in low power mode. This signal must be asserted sometime after the trailing edge of system RESET (See Figure 2).

GPO27# serves as the hardware reset for the Intel740 chip. A hardware reset to the Intel740 chip takes the device out of the low power state. Since the PCIRST# signal is used to disable the device, it can not be used for this purpose. At the trailing edge of GPO27# the Intel740 chip will be functional (See Figure 1).

The duration of GPO28# and GPO27# are listed in Table 1.

Table 1. Signal Duration of the GPO Signals from PIIX4

Signal	Active	Minimum Duration	Actual Duration*
GP027# from PIIX4	Low (0)	1ms	1ms
GP028# from PIIX4	Low (0)	=SUM	1ms

NOTE:
1. 1 ms is the smallest system BIOS increment of time
2. SUM = The sum of the propagation delaly for the logic depicted in Figure 2.

Figure 1. Schematic Diagram for GPO27#

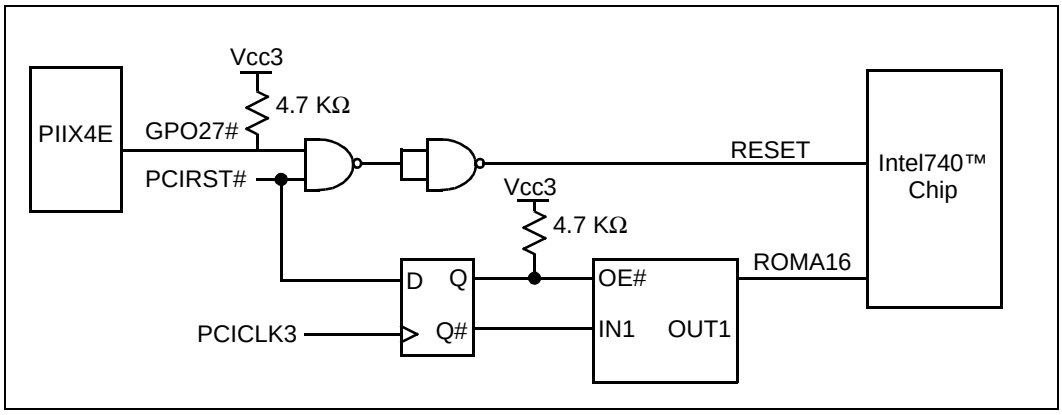
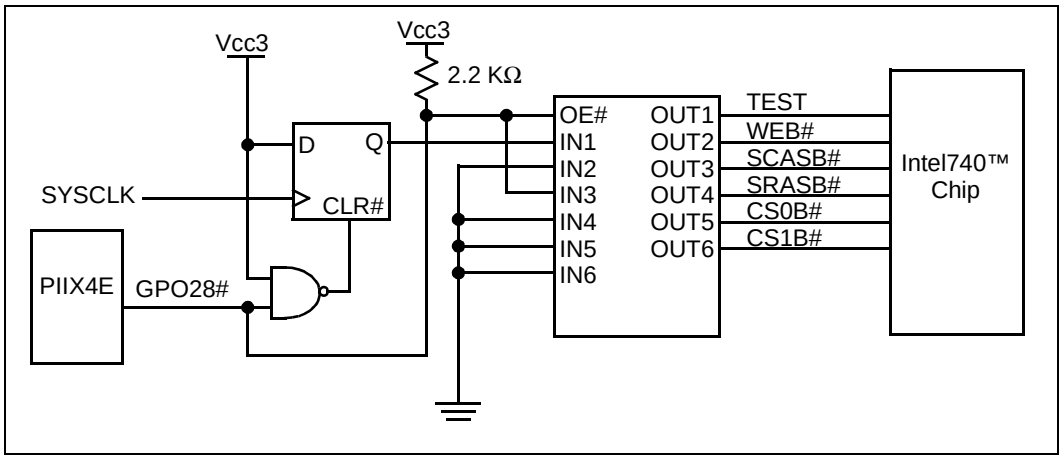


Figure 2. Schematic Diagram for GPO28#



2.1 State Diagrams

At system RESET, the Intel740™ graphics controller on the motherboard is always put into the low power state. The following are examples in which the on-board device shall remain in low power state:

1. AGP add-in card is present
2. PCI or ISA graphics device is the primary and only graphics device desired
3. Multimonitor configurations not utilizing the on-board graphics device

For example 2 and 3 above, an option should be provided in system BIOS or CMOS setup to keep the Intel740™ chip in low power mode.

Note: When not in use, both GPO27# and GPO28# should be driven high (1).

Figure 3. Intel740™ Graphics Controller (On-board Device) Remains in Low Power Mode

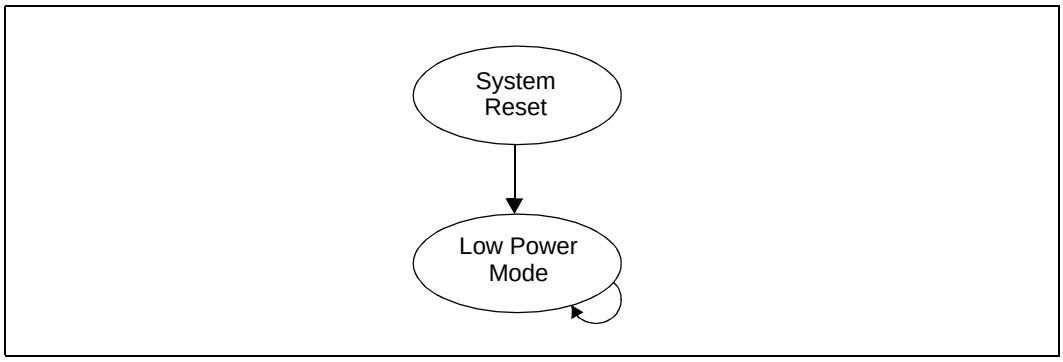
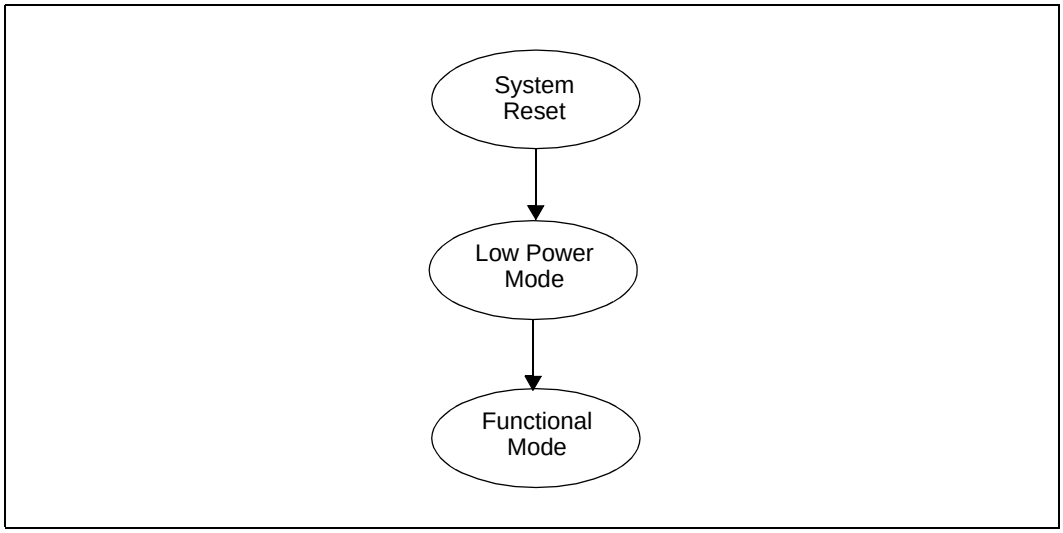


Figure 4. Intel740™ Graphics Controller (On-board Device) State Diagram



The Intel740 graphics controller down on the motherboard enters the low power mode at system reset. If an enabling event occurs, the device enters the functional mode from the low power mode (see Figure 4).

The following are examples in which functional mode would be invoked:

1. Intel740™ graphics accelerator as the primary and only graphics device
2. Multimonitor configurations utilizing the Intel740™ graphics controller

2.2 Supported Single Monitor and Mulitmonitor Configurations

Table 2. Monitor and Mulitmonitor Configurations

Configuration	Single Monitor			Multimonitor		
Primary Graphics Device	On-Board Intel740™ Device	AGP Add-in Card	Non AGP (PCI or ISA)	Non AGP (PCI or ISA)	Non AGP (PCI or ISA)	Non AGP (PCI or ISA)
Secondary Graphics Device	None	None	None	On-Board Intel740	AGP Add-in Card	Non AGP (PCI or ISA)
Flow						
System RESET (GP028# Asserted to Enter Low Power Mode)	Yes	Yes	Yes	Yes	Yes	Yes
Primary Video Initialization	GP027# Asserted to enable the Intel740 Chip	AGP Add-in initialized	PCI or ISA card initialized	PCI or ISA card initialized	PCI or ISA card initialized	PCI or ISA card initialized
Secondary Video Initialization	Does not Apply	Does Not Apply	Does Not Apply	GP027# asserted to enable the Intel740 Chip	AGP Add-in initialized	PCI or ISA card(s) initialized

2.3 Software Sequence

The system BIOS has to follow sequence below for enabling the Intel740™ graphics controller (on-board device). The instructions below should be executed early in POST so that the Intel740™ graphics controller (on-board device) is placed in a low power state.

1. Assert GPO28# low for a minimum of 149 ns.
2. Assert GPO28# high. The Intel740™ graphics controller (on-board device) is placed in a low power state after executing this instruction.
3. Enable the 82443BX Device #1 (AGP Bridge) to access the devices behind the bridge.
4. Check whether any devices are present behind the 82443BX Device #1 (AGP Bridge). The check can be performed by checking the Vendor ID and Device ID register for a non 0FFFFh value.
5. If there are any devices present behind the 82443BX Device #1 (AGP Bridge), go to step #8.
6. Assert GP028# low for at least 1us.
7. Assert GP028# high, the Intel740™ Graphics Controller (on-board device) is in a normal operating state after executing this instruction.
8. Re-program the 82443BX Device #1 (AGP Bridge) to disable the access to devices behind the bridge.
9. Continue with rest of POST in BIOS.

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B

Reference Information

PC SGRAM Specification

Revision 0.9

February 1998

Order Number: Not Applicable

Revision 0.9

Contents

Figures

Tables

1.0 Introduction

1.1 Objective

The objective of this document is to define a SGRAM specification (“PC SGRAM”). It should be easy to design and manufacture and highly cost optimized for the main stream volume desktop Graphics architecture PCs.

1.2 Scope of This Document

The scope of this document is limited to identify and define all the essential functionality that is needed to be implemented for “PC SGRAM”. Implementation details are left to the designers of the device.

1.3 Convention Used

- # sign after signals are used after the signal names for active low signals (e.g., CS#, RAS#, etc.)

2.0 Pinout

The pinout for 8Mb and 16Mb SGRAM configurations are shown below.

Figure 1. 256kx32 SGRAM Pinout

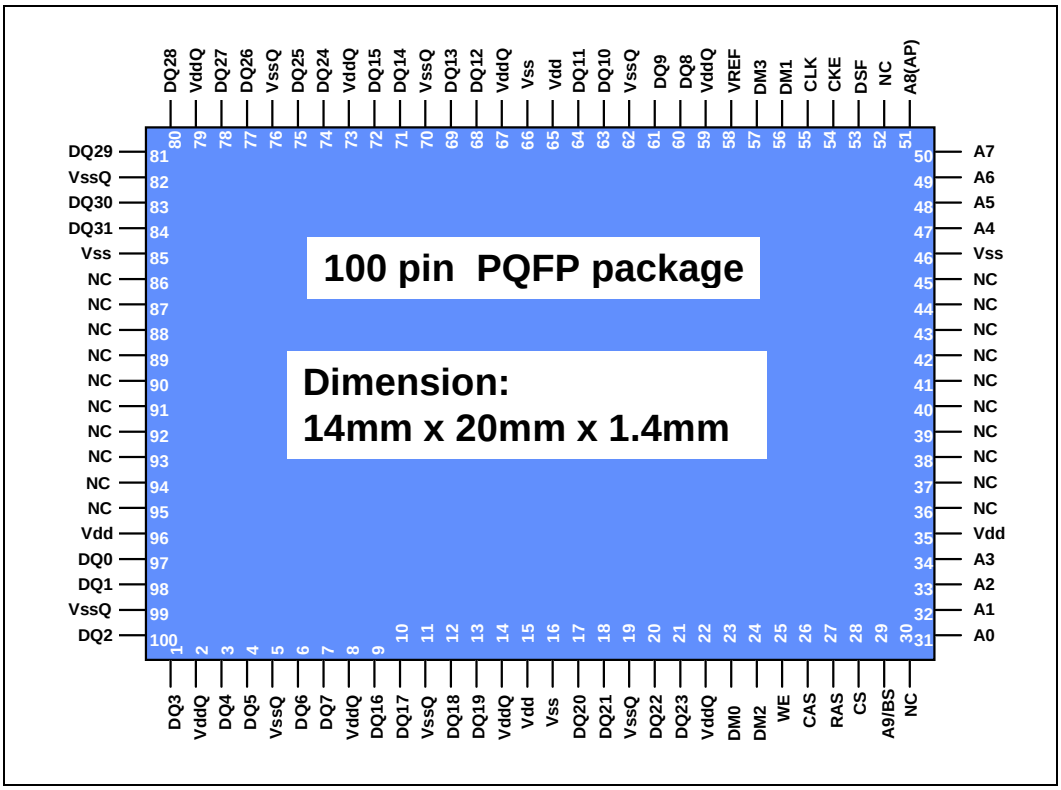
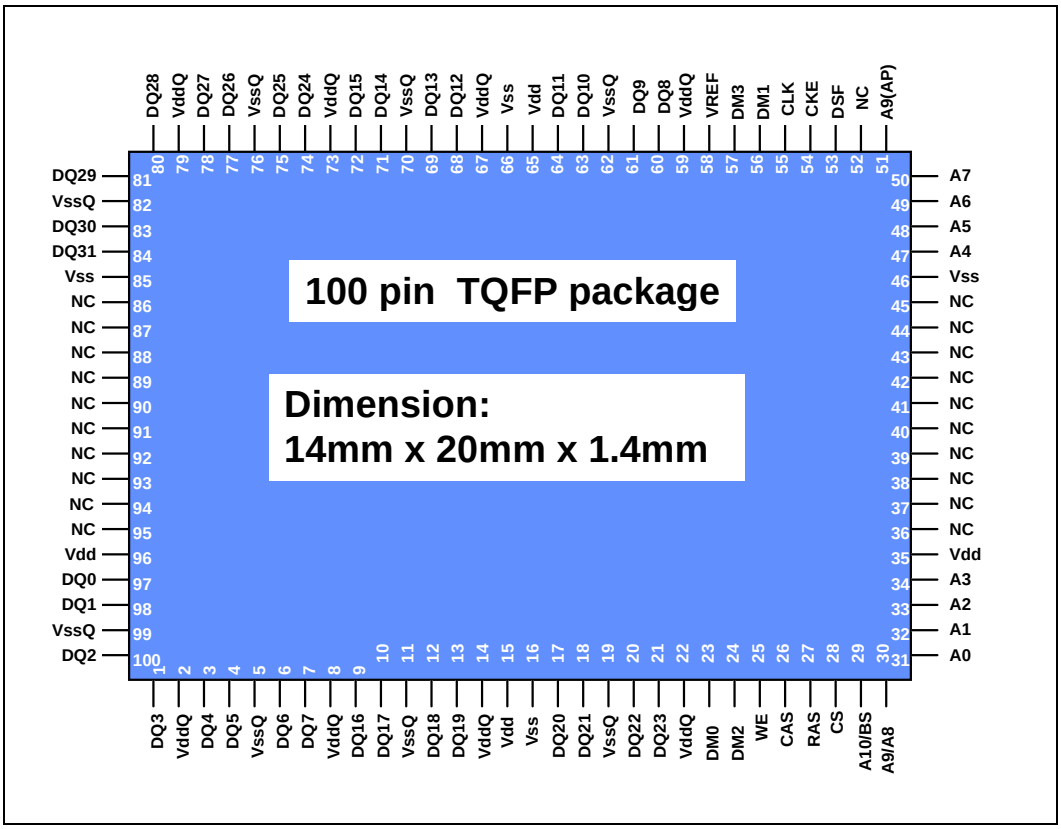


Figure 2. 512kx32 SGRAM Pinout



2.1 Pin Functional Descriptions (Simplified)

Table 1. Pin Functional Description

Symbol	Type	Description[a]
A[9:0]	Input - Synchronous	Address. Multiplexed Row and Column Address.
BA	Input - Synchronous	Bank Address. BA0 and BA1 specify the selected Bank during
AP	Input - Synchronous	Auto Precharge (Multiplexed with Row Address).
CLK	Input - Clock	Clock Input
CKE	Input - Clock Enable	Activates the CLK signal when high and deactivates when low. By deactivating the clock, CLKE low initiates the Power Down mode.
CS#	Input - Synchronous	Chip Select. Disables or enables the device operation by masking or enabling all inputs except CLK, CLK#, CKE, DQS, DQ and DM.
RAS#	Input - Synchronous	Row address strobe.
CAS#	Input - Synchronous	Column address strobe.
WE#	Input - Synchronous	Write Enable.
DQM[3:0]	Input	DQ Mask. Write data byte mask, Read output byte enables Active high. Read latency is two cycle from DQM and zero cycle for write. In write mode it masks the data from being written to the memory array. DM masking occurs in the same cycle during write operation. Write data byte mask, Read output byte enables. DQM is synchronous to the clock; thus, the masking occurs for the whole clock.
DQ[31:0]	Input/Output	Data IO pins.
DSF	Input - Synchronus	DFS: Enables the write per bit and Block write function. This pin has an internal pull-down resistor.
Vcc, Vss	Power pins	Supply Pins for the core
VccQ, VssQ	Power pins	Supply Pins for the output buffers

a. See the Truth Table and functional description for detailed information about the functionality

3.0 Control Registers

3.1 Mode Register and Modes Required to be Supported

PC SGRAM's mode register is accessed through the Mode Register Write command. The Mode Register is used to load the value of CAS Latency, Burst Type, & Burst Length

Table 2. Mode Register Description

Bit	Attribute	Description
BA	Reserved	Reserved: For normal operation, BA[1:0] should be "0"
A[9:7]	Reserved	Reserved: For normal operation, A[9:7] should be "000"
A[6:4]	WO	**CAS Latency:** 000 Reserved 001 Reserved 010 2 011 3 100 Reserved 101 Reserved 110 Reserved 111 Reserved
A[3:0]	WO	**Burst Type:** 0 = Sequential 1 = Interleave
A[2:0}	WO	**Burst Length:** **BT=0** **BT=1** 000 1 1 001 2 2 010 4 4 011 8 8 100 Reserved Reserved 101 Reserved Reserved 110 Reserved Reserved 111 Full Page Reserved

3.2 Special Mode Register

SGRAM's Special Mode Register is accessed through the Mode Register Write command. The Special Mode Register is used to load data into the Color Register or the Mask register. During the execution of the Special Mode Register Command, Bits A[6:5] determine if a new value is to be loaded into the Color and Mask registers.

Table 3. Special Mode Register

Bit	Attribute	Description
A[6]	WO	**Color Register:** 0 = Leave data unchanged for Color Register 1 = Load new data into Color Register
A[5:0]	Reserved	Reserved: For normal operation, these bits should always be "00000"

3.3 Color Register

Data is loaded into the Color Register through the Special Mode Register Write command. During the execution of the Special Mode Register Command, bit A[6] is used to determine if a new value is to be loaded into the Mask registers. If A[6] =1 during the special mode register command, then the value on DQ[31:0] is loaded into the Color Register. The color register supplies data for the block write command.

Table 4. Color Register

Bit	Default	Attribute	Description
31:0	00000000h	WO	**Color Register Data:** Data from these bits is used for Block Write Command.

4.0 Command Truth Table

Table 5. Command Truth Table

Function	Symbol	Command & Address								
		CS#	RAS#	CAS#	WE#	DSF	A8/ A9	DQM	A[7:0]	BA0, BA1
Mode Register Write	MRS	L	L	L	L	L	x	x	Data for Mode Register.	x
Special Mode Register Write	SMRWR	L	L	L	L	H	x	x	Data for SMR	x
CBR Refresh	CBR	L	L	L	H	L	x	x	x	x
Activate (Single Bank)	ACT	L	L	H	H	L	x	v	Row Address	Bank Address
Block Write	BLKWR	L	H	L	L	H	x	v	Column Address	Bank Address
Write	WRITE	L	H	L	L	L	x	v	Column Address	Bank Address
Write with Auto-precharge	WRITEAP	L	H	L	L	L	H	v	Column Address	Bank Address
Read	READ	L	H	L	H	L	L	x	Column Address	Bank Address
Read with Auto-precharge	READAP	L	H	L	H	L	H	x	Column Address	Bank Address
Burst Stop	BST	L	H	H	L	L	x	x	x	x
Precharge select Bank	PRE	L	L	H	L	L	L	x	x	Bank Address
Precharge All Banks	PALL	L	L	H	L	L	H	x	x	x
No Operation	NOP	L	H	H	H	L	x	x	x	x
Device Deselect	DSEL	H	x	x	x	x	x	x	x	x

Table 6. DQM Truth Table

Function	CKE n-1	CKE n	DQMx
Data write/output enable	H	X	L
Data mask/output disable	H	X	H
Byte x write mask	H	X	H

NOTE: H: High Level, L: Low Level, X: don't care, V: Valid data input

5.0 Operative Command Table

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Idle	H	X	X	X	L	X	DSEL	Nop or Power Down	3
	L	H	H	H	L	X	NOP	Nop or Power Down	3
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	ILLEGAL	4
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4
	L	L	H	H	L	BA,RA	ACT	Row Active	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	NOP	
	L	L	L	H	L	X	CBR/SELF	Refresh or Self refresh	5
	L	L	L	L	L	Op-code	MRS	Mode Register access	
	L	L	L	L	H	Op-code	SMRWR	Special Mode Register Write	
Row active	H	X	X	X	X	X	DSEL	NOP	
	L	H	H	H	L	X	NOP	NOP	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Begin read: Optional AP	6
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	Begin write: Optional AP	6
	L	H	L	L	H	BA,CA	BLKWR	Begin Block write:	6
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	L	BA, A8/A9	PRE/PALL	Precharge	7
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	OP-code	MRS	ILLEGAL	14
	L	L	L	L	H	OP-code	SMRWR	ILLEGAL	14
READ	H	X	X	X	X	X	DSEL	Continue burst to end -> Row active	
	L	H	H	H	L	X	NOP	Continue burst to end -> Row active	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Term burst, new read: Optional AP	8
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	Term burst, new wrtie: Optional AP	8,9
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	8,9
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	L	H	L	L	BA,A8	PRE/PALL	Term burst, precharge	
	L	H	H	L	L	X	BST	Term burst	
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
WRITE	H	x	x	x	x	X	DSEL	Continue burst to end ->Write recovering	
	L	H	H	H	L	X	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	L	BA,CA,A 8/A9	READ/ READAP	Term burst, start read: optional AP	8,9
	L	H	L	L	L	BA,CA,A 8/A9	WRIT/ WRITEAP	Term burst, new write: optional AP	8
	L	H	H	L	L	X	BST	ILLEGAL	
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	8
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	L	BA, A8/A9	PRE/PALL	Term burst precharging	10
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Read with auto precharge	H	X	X	X	X	X	DSEL	Continue burst to end -> precharging	
	L	H	H	H	L	X	NOP	Continue burst to end -> precharging	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Write with auto precharge	H	X	X	X	X	X	DSEL	Continue burst to end ->Write recovering with auto precharge	

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	H	H	L	X	NOP	Continue bust to end-> Write recovering with auto precharge	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	L	BA,A8	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Precharging	H	X	X	X	X	X	DSEL	NOP- Enter Idle after Trp	
	L	H	H	H	L	X	NOP	NOP-Enter Idle after Trp	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA,A8/ A9	PRE/PALL	NOP- Enter Idle after Trp	
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Row activating	H	X	X	X	X	X	DSEL	NOP- Enter row active after Trcd	
	L	H	H	H	L	X	NOP	NOP- Enter row active after Trcd	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,11,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Write Recovering	H	X	X	X	X	X	DSEL	NOP - Enter row active after Tdpl	
	L	H	H	H	L	X	NOP	NOP - Enter row active after Tdpl	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Start Read, optional AP	9
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	New Write, optional AP	
	L	H	L	L	L	BA,CA	BLKWR	Block Write	
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Write recovering with auto precharge	H	X	X	X	X	X	DSEL	NOP - Enter precharge after Tdpl	
	L	H	H	H	L	X	NOP	NOP - Enter precharge after Tdpl	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,9,13
Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Refreshing	H	X	X	X	X	X	DSEL	NOP - Enter idle after trc	
	L	H	H	H	L	X	NOP	NOP- Enter idle after trc	
	L	H	L	X	X	X	READ/ READAP	ILLEGAL	14
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	X	X	X	ACT/PRE/PALL	ILLEGAL	14
	L	L	L	X	X	X	CBR/SELF/ MRS	ILLEGAL	14

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Mode Register accessing	H	X	X	X	X	X	DSEL	NOP - Enter idle after tmrd	
	L	H	H	H	L	X	NOP	NOP - Enter idle after tmrd	
	L	H	L	X	X	X	READ/ WRITE/ READAP/ WRITEAP/ BLKWR	ILLEGAL	14
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	X	X	X	X	ACT/PRE/ PALL/ CBR/ SELF/MRS/ SMRWR	ILLEGAL	14

NOTES:
1. H: High Level, L: Low Level, X: don't care, V: Valid data input, BA: Bank Address, AP: (Auto Precharge), CA: (Column Address), RA: (Row Address)
2. All entries assume that CKE was active (high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive (low level), then in power down mode.
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
5. If both banks are idle and CKE is inactive (low level), then Self refresh mode.
6. Illegal if trcd is not satisfied.
7. Illegal if tras is not satisfied.
8. Must satisfy burst interupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tdpl.
11. Illegal if trrd is not satisfied.
12. Burst Stop command is disabled.
13. Ilegal for single bank, but legal for other banks in multi-bank devices.
14. Illegal for all banks.

6.0 Row/Column Addressing Per Memory Size/# Banks

Table 8. Row, Column and Bank addressing

Parameter	2x128kx32 (8Mb)	2x256kx32 (16Mb)
Bank Address	BA	BA
Row Address	A[8:0]	A[9:0]
Column Address	A[7:0]	A[7:0]
Auto-Precharge	A8	A9
Page Size	256x32	256x32

7.0 Functional Description

7.1 Power Up Sequence

The SGRAM should be initialized by the following sequence of operations:

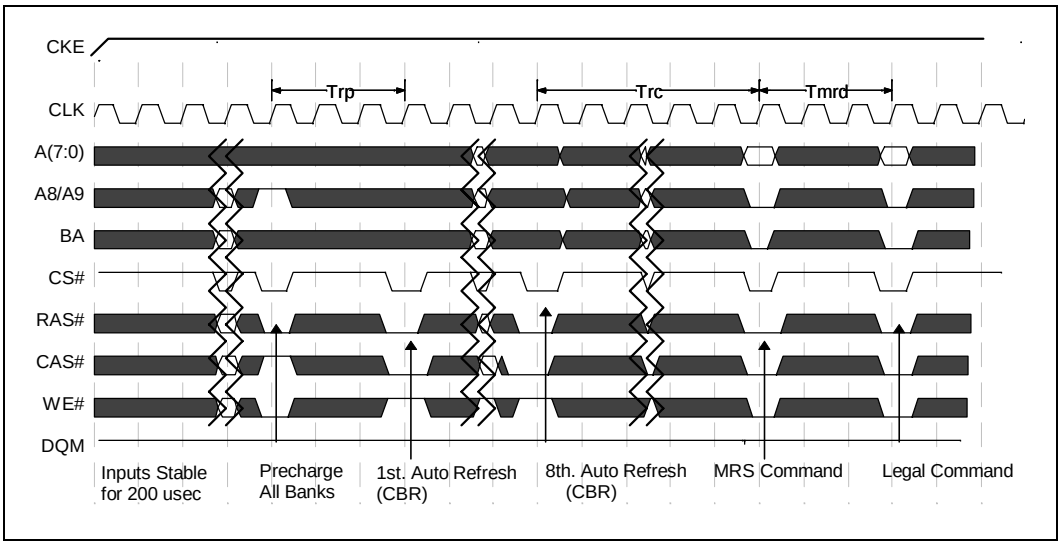
- Clock will be applied at power up along with power (clock frequency will be unknown).
- The clock will be stabilized within 100usec after power stabilizes.
- All the control inputs, RAS#, CAS#, WE#, CS# will be held in an undefined state during reset. After reset is complete RAS#, CAS#, WE#, and CS# will be held inactive before the first access to SGRAM is attempted.
- The levels on all the address inputs should be ignored. (All the addresses inputs can be indeterminate.)

Initialization Sequence

The initialization sequence can be issued at *anytime*. Following the initialization sequence, the device must be ready for full functionality. SGRAM devices are initialized by the following sequence:

- At least one NOP cycle will be issued after the 1msec device deselect.
- A minimum pause of 200usec will be provided after the NOP.
- A precharge all (PALL) will be issued to the SGRAM.
- 8 Auto refresh (CBR) refresh cycles will be provided.
- A mode register set (MRS) cycle will be issued to program the SGRAM parameters (e.g., Burst length, CAS# latency, etc.).
- After MRS, the device should be ready for full functionality within 3 clocks after T_{mrd} is met.

Figure 3. Power Up Initialization Sequence



7.2 Precharge Selected Bank

The precharge operation should be performed on the active bank when precharge selected bank command is issued. When the precharge command is issued with address A8/A9 low, BA selects the bank to be precharged. At the end of the precharge selected bank command the selected bank should be in idle state after the minimum T_{RP} is met.

7.3 Precharge All

All the banks should be precharged at the same time when this command is issued. When the precharge command is issued with address A8/A9 high, then all the banks will be precharged. At the end of the precharge all command all the banks should be in idle state after the minimum T_{RP} is met.

7.4 NOP and Device Deselect

The device should be deselected by deactivating the CS# signal. In this mode SGRAM should ignore all the control inputs. The SGRAM is put in NOP mode when CS# is active and by deactivating RAS#, CAS# and WE#. For both Deselect and NOP the device should finish the current operation when this command is issued.

7.5 Row activate

This command is used to select a row in a specified bank of the device. Read and write operations can only be initiated on this activated bank after the minimum T_{RCD} time is elapsed from the activate command.

7.6 Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating CS#, CAS# and de-asserting WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

7.7 Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating CS#, CAS# and WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

7.8 Block Write

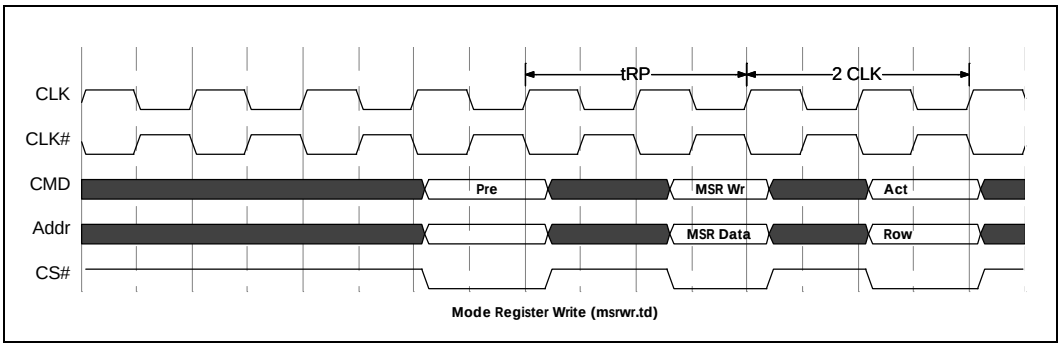
The Block Write command is used to write a block of data to an active row and bank within the device. The Block Write command is issued by driving CS# low, RAS# high, CAS# low, WE# low and DSF high. A Block Write command is a non-burst write command that writes data to 8 columns simultaneously. The data value contained in the Color Register (CR) is written to eight consecutive column locations addressed by A[7:3].

A Block Write access requires a minimum time of T_{BWC} to execute. No new commands can be executed until T_{WBC} is met except for Activate and Precharge command to the other banks.

7.9 Mode Register Set

This command is used to program the SGRAM for the desired operating mode. This command should be used after power up as defined in the power up sequence before the actual operation of the SGRAM is initiated. The functionality of the SGRAM device can be altered by re-programming the mode register through the execution of Mode Register Set command. All the banks should be precharged (i.e., in idle state) before the MRS command can be issued.

Figure 4. Mode Register Set Command

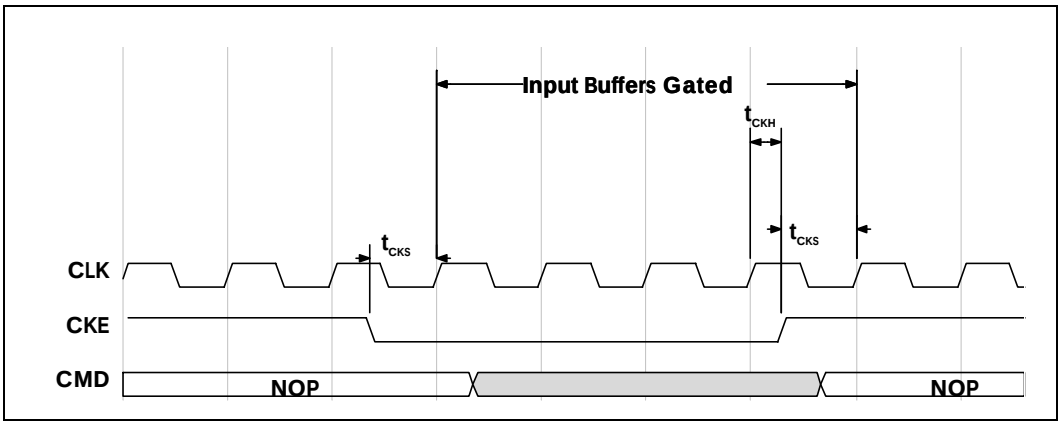


7.10 Power Down Mode

The Power down mode for PC SGRAM can be entered when both banks are in idle state (precharged) and CKE is asserted low. When in power down mode all input and output buffers are de-activated (except for CKE). If the device stays in the power down mode for more than 15.6 usec (refresh interval), then the PC SGRAM will loose data.

The power down mode can be exited by driving CKE high again. CKE assertion and de-assertion should meet the CKE setup and hold time (t_{CKS} and t_{CKH}).

Figure 5. Timing for Power Down Mode



8.0 Essential Functionality for the “PC SGRAM” device

The functionality that are essential for the “PC SGRAM” device are described below:

- Burst Read
- Burst Write
- Multi bank access
- Burst Read with Autoprecharge
- Burst Write with Autoprecharge
- Burst Read terminated with precharge
- Burst Write terminated with precharge
- Burst Read terminated with another Burst Read/Write
- Burst Write terminated with another Burst Write/Read
- DQM masking
- Fastest command to command delay of 1 clock
- Precharge All command
- Auto Refresh
- CL=2,3
- Burst Length 1,2, 4 & 8

8.1 Burst Read and Burst Write

Burst read and write commands are initiated as shown in the diagram below. The bank first needs to be activated (if not already activated) through the activate bank command and then the read or write command should be initiated. Read and write is distinguished by the WE# signal state as shown. T_{RCD} (RAS to CAS delay) must be met to initiate a command after the activate command.

8.2 Multi- bank ping pong access

Two bank ping pong access is described in the following diagram. Another bank can be activated while the first bank is being accessed as shown. RAS to RAS delay T_{RRD} must be met while activating another bank.

8.3 Read and Write with autoprecharge

Burst reads and writes with auto precharge commands are initiated *with autoprecharge if A8/A9 is to high* while the read or write commands are issued.

8.3.1 Precharge Command After a Burst Read

The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL - 2 clocks. The precharge command can be issued as soon as the tras time is met. The earliest time that precharge can be issued is shown for the CAS Latency = 3 devices.

8.3.1.1 Precharge Termination of a Burst Read

Burst Read (with no autoprecharge) can be terminated earlier using a precharge command along with the DQM. This terminates reads when the remaining data elements are not needed. It allows starting the precharge early. The remaining data is undefined. DQM should be used to mask.

8.3.1.2 Precharge Command After a Burst Write

The earliest time that precharge can be issued is T_{DPL} clocks after the last data.

8.3.1.3 Precharge Termination of a Burst Write

To terminate Burst Write early with precharge command DQM signal should be used as shown. Data sampled T_{DPL} clocks before precharge command will be written correctly. Data sampled after and before the precharge command is undefined. DQM should be used to prevent the location from being corrupted.

8.3.2 Read Terminated By Read

A Read Command should terminate the previous read command and the data should be available after CAS Latency for the new command. Fastest command to command delay is determined by T_{CCD}

8.3.3 Write Terminated By Write

A Write Command should terminate the previous write command and the new burst write command should start with the new command as shown. Fastest command to command delay is determined by T_{CCD} .

8.3.4 Read Terminated By Write

A Write Command should terminate the previous read command and the new burst write should start. The DQM must be held active to keep the output buffer in HiZ as shown to prevent the internal IO buffer conflict between the read data (in pipe) and the write data driven on the input pins.

8.3.5 Write Terminated By Read

A Read Command should terminate the previous write command and the new burst read should start as shown. In case of with T_{CCD} =1, CL=3 and tdqz=2, there is no loss of data bandwidth even if DQM is activated to mask the write data.

In the case of CL=2 and tdqz=2, the activation of DQM signal causes the first read data to be lost, if read command is issued (T_{CCD} =1). To preserve the first read data the issue of READ command has to be delayed (T_{CCD}=2). This implementation reduces the command bus utilization.

If a Precharge-All command is detected by SGRAM component in CLK(n), then there will be no commands presented to this component until CLK(n+tRP).

bank command.

8.4 Back to Back Command Support

Minimum command to command delay of 1 Clock should be supported.

8.5 Auto Refresh (CBR) Command

An auto refresh (CBR) should be used to refresh the SGRAM array explicitly. Refresh addresses should be generated internally by the SGRAM device and incremented after each auto refresh automatically. No commands (including another auto refresh) should be issued until a minimum T_{RC} is satisfied.

9.0 SGRAM AC/DC Parameters

9.1 DC Specifications for 100-166 MHz

Table 9. Absolute Maximum D.C. Rating

Symbol	Parameter	Min	Max	Units	Notes
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	V_{DD} + 0.5	V	
V_{DD}, V_{DDQ}	Voltage Supply pins pin w.r.t V_{SS}	-0.5	4.5	V	
Ts	Storage Temperature	-55	125	°C	

Table 10. D.C Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
VDD	Supply Voltage		3.135	3.6	V	
VDDQ	I/O Supply Voltage		3. 135	3.6	V	
Iil	Input Leakage Current	0 < Vin < VDDQ	-10	+10	µA	1,2
Cin	Input Pin Capacitance	@1MHz	2.5	5.0	pF	Target 3.75pf
CI/O	I/O Pin Capacitance	@1MHz	4.0	6.5	pF	Target 5.25pf
Cclk	Pin Capacitance	@1MHz	2.5	4.0	pF	Target 3.25pf
Lpin	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	65	°C	

NOTES:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

9.2 A.C. Specifications for 100-166 MHz

Table 11. Maximum AC Operating Requirements

Symbol	Parameter	Min	Max	Units	Notes
Vih	Input High Voltage	2.0	VDDQ+2.0	V	1,2
Vil	Input Low Voltage	VSSQ – 2.0	0.8	V	1,2

NOTES:
1. The overshoot and undershoot voltage duration is <=3ns with no input clamp diodes
2. The VDDQ and VSSQ are the operating parameters (not absolute max. parameters)

The refresh rate for all devices is assumed at a maximum of 15.6us per row per the table below.

Table 12. Refresh Rate

Symbol	Parameter	Min	Max	Units	Notes
Tref	Refresh rate / row	15.6		usec	1

NOTE:
1. The overall array refresh is determined by multiplying the specified row refresh rate by the number of rows in the total array.

9.3 A.C. Timing Parameters for 100-166 MHz

Table 13. 100, 125, 143MHz & 166MHz AC Timing Parameters

		100		125		143		166		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Clock Period	t_{CK}		10		8		7		6	ns
CAS Latency	CL	2	3	2	3	2	3	2	3	CLK
CLK to valid output delay (max)	T_{AC} (max)		7		6		6		5.5	ns
Output data hold time	T_{OH}	2.5		2.5		2.5		2.5		ns
Address & Command Input setup time	T_{AS}	2.5		2.5		2		1		ns
Address & Command Input hold time	T_{AH}	1		1		1		1		ns
Data Input setup time	T_{DS}	2.5		2		1.5		1		ns
Data Input hold time	T_{DH}	1		1		1		1		ns
Activate to Activate Delay (Different bank)	T_{RRD}	2		2		2		2		CLK
Read to Read Command Delay,Write to Write Command Delay	T_{CCD}	1		1		1		1		CLK
Activate to Read, Write or Block Write Delay	T_{RCD}	2		3		3		3		CLK
Precharge to Activate Delay (single bank precharge)	T_{RP}	2		3		3		3		CLK
Activate to Precharge Delay	T_{RAS}	5		6		7		7		CLK
Activat to Activate Delay (Same Bank), Refresh Cycle time	T_{RC}	7		9		10		11		CLK
Block Write to Precharge Delay	T_{BPL}	2		2		2		2		CLK
Block Write Cycle Time	T_{BWC}	2		2		2		2		CLK
Last write data in to precharge	T_{DPL}	1		1		1		1		CLK

NOTE:
1. Output I/O Timings measured with a 30pf load

9.4 DC Specifications for 166-250 MHz

Absolute Maximum D.C. Rating (TBD)

D.C Operating Requirements (TBD)

9.5 A.C. Specifications for 166-250 MHz

Maximum AC Operating Requirements (TBD)

Refresh Rate (TBD)

9.6 A.C. Timing Parameters for 166-250 MHz

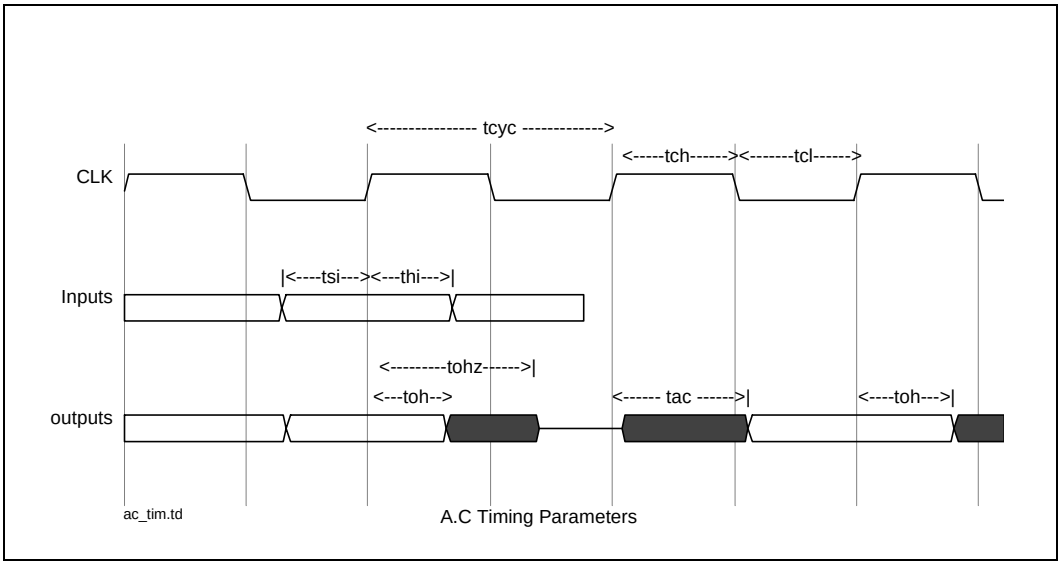
Table 14. 166, 200, 250 MHz & 166 MHz AC Timing Parameters

		166		200		250		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Period	t_{CK}	6		5		4		ns
CAS Latency	CL	2	3	2	3	2	3	CLK
CLK to valid output delay (max)	T_{AC} (max)		5.5	TBD		TBD		ns
Output data hold time	T_{OH}	2.5		TBD		TBD		ns
Address & Command Input setup time	T_{AS}	1		TBD		TBD		ns
Address & Command Input hold time	T_{AH}	1		TBD		TBD		ns
Data Input setup time	T_{DS}	1		TBD		TBD		ns
Data Input hold time	T_{DH}	1		TBD		TBD		ns
Activate to Activate Delay (Different bank)	T_{RRD}	2		TBD		TBD		CLK
Read to Read Command Delay,Write to Write Command Delay	T_{CCD}	2		TBD		TBD		CLK
Activate to Read, Write or Block Write Delay	T_{RCD}	3		TBD		TBD		CLK
Precharge to Activate Delay (single bank precharge)	T_{RP}	3		TBD		TBD		CLK
Activate to Precharge Delay	T_{RAS}	7		TBD		TBD		CLK
Activat to Activate Delay (Same Bank), Refresh Cycle time	T_{RC}	11		TBD		TBD		CLK
Block Write to Precharge Delay	T_{BPL}	2		TBD		TBD		CLK
Block Write Cycle Time	T_{BWC}	2		TBD		TBD		CLK
Last write data in to precharge	T_{DPL}	2		TBD		TBD		CLK

9.7 IBIS: I/V Characteristics for Input and Output Buffers

(TBD)

Figure 6. A.C Timing Parameters



NOTE:
1. Reference level is set at 1.5V, AC measurements are specified into 50pf load.
2. input edge rates are specified as 1.0v/ns minimum (0.8v to 2.0v)

9.8 IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

To download a copy of the specification, the golden parser, various public-domain models, the *IBIS Overview* in PostScript, and other information, either phone in by modem or use FTP.

FTP:	(IP address 198.31.14.3) login as "anonymous" password is your email address
Modem:	(408)945-4170 login as "guest" password is your email address

IBIS-related files are in the directory "/pub/ibis" and its sub-directories.

To get documents by email, send an email message to "archive@vhdl.org" with the following commands in the message body:

path <your_email_address>
send docs <name_of_document>

For direct modem access, dial-up to the vhdl.org system at (408) 945-4170. You can use any baud rate up to 14,400, any parity, start and stop bits, and any v.* settings. Log in using the "guest" account. Simple UNIX commands such as "cd", "ls", and "cat" are available and you can download files using "kermit", "zmodem", or "sz" (another zmodem application).

For Internet access, use "ftp vhdl.org" (or "ftp 198.31.14.3") and log in as user "anonymous". The gopher utility is available and highly recommended. Gopher to "vhdl.org". Set "binary" mode for transferring binary files (*.doc, *.fm, *.xls).

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**

SO-DIMM Module — Unbuffered SDRAM/SGRAM Graphics

64-bit (Non-ECC/Parity)
144-pin Module

Revision 0.91

February 1998

Order Number: Not Applicable

Revision 0.91

Contents

Figures

Tables

1.0 Unbuffered Graphics SO-DIMM Module

1.1 General Features

- 144-pin, small-outline, dual-in-line memory module (SO-DIMM).
- 64-bit data bus (non-ECC/Parity)
- Maximum of 8MB per module with extensions to 32MB
- SDRAM/SGRAM
- Single, 3.3V ±10% power supply
- LVTTL-compatible inputs and outputs
- Specification currently defines four module frequencies (speeds); 66 MHz (15 nS), 83 MHz (12 nS), 100 MHz (10 nS), and 125 MHz (8 nS).

1.2 Labeling

Four module frequencies are currently defined; they are:

- 66 MHz (15 nS).
- 83 MHz (12 nS).
- 100 MHz (10 nS).
- 125 MHz (8 nS).

For consistency, modules should be clearly marked indicating their rated frequency in MHz. The speed, in nano-seconds, is optional. This label should be consistent with the module speed setting used in the resistor strapping option.

To be compliant, a module must meet at least one complete table in the Memory Timing section of the “PC SGRAM” specification.

2.0 Mechanical Outline

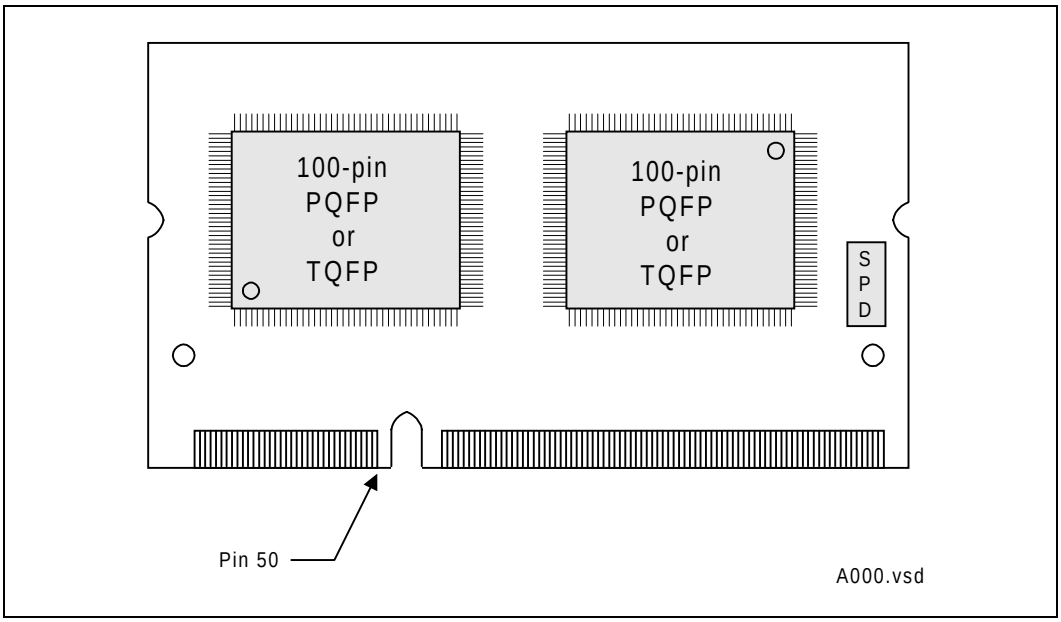
- Dimensions: 67.6 mm (length) X 25.4-50.8 mm (height) X 1.0 mm (thickness)
- 144-pin (0.8 mm pitch zig-zag)

For mechanical specifications of SO-DIMM modules, refer to the JEDEC Committee Ballot

JC-42.5-95-171 144-pin SDRAM SO-DIMM Item 708.4
(herein referred to as the JEDEC SO-DIMM specification).

The key position has been shifted to prevent this module from being inserted into a typical main-memory SDRAM socket.

Figure 1. SDRAM SO-DIMM Module



3.0 Environmental Requirements

Table 1. Environmental Requirements

Operating Temperature	0^{o}C to +65^{o}C
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10.106 PSI (up to 10,000 ft.)
Storage Temperature	-40^{o}C to +70^{o}C
Storage Humidity	5% to 95% without condensation
Storage Pressure	1.682 PSI (up to 50,000 ft.) at 50^{o}C

4.0 Pin Assignments

Table 2. SO-DIMM Module Pin Assignments

PIN #	Front	PIN #	Back	PIN #	Front	PIN #	Back
1	Vss	2	Vss	73	CLK1	74	CLK0
3	DQ63	4	DQ62	75	Vcc	76	Vcc
5	DQ61	6	DQ60	77	RSVD	78	RSVD
7	DQ59	8	DQ58	79	RSVD (A11)	80[1]	A10
9	DQ57	10	DQ56	81[1]	A9	82[1]	A8
11	Vcc	12	Vcc	83	A7	84	A6
13	DQ55	14	DQ54	85	Vss	86	Vss
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	Vss	22	Vss	93	Vcc	94	Vcc
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	Vcc	28	Vcc	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	Vss	104	Vss
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	Vss	38	Vss	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	Vcc	114	Vcc
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	Vcc	48	Vcc	119	Vss	120	Vss
49	RSVD	50	RSVD	121	DQ15	122	DQ14
51	RSVD	52	RSVD	123	DQ13	124	DQ12
53	RSVD	54	RSVD	125	DQ11	126	DQ10
55	Vss	56	Vss	127	DQ9	128	DQ8
57	DSF	58	RFU	129	Vcc	130	Vcc
59	RFU	60	RFU	131	DQ7	132	DQ6
61	RFU	62	SBA	133	DQ5	134	DQ4
63	Vcc	64	Vcc	135	DQ3	136	DQ2
65	CS1	66	CS0	137	DQ1	138	DQ0
67	/RAS	68	/CAS	139	Vss	140	Vss
69	/WE	70	CKE	141	SDA	142	SCL
71	Vss	72	Vss	143	Vcc	144	Vcc

NOTE:
1. Refer to Table 3 “Address Translation” on page 9 for determining SO-DIMM to SGRAM device (256Kx32 or 512Kx32) connections for pins 80, 81 and 82.

5.0 Graphics SO-DIMM Block Diagram

Figure 2 through Figure 5 illustrate the electrical connectivity of several SO-DIMM configurations. The series termination resistors on CLK0 and CLK1 are not currently used and should be set to 0 ohms. Table 3 “Address Translation” on page 9 should be followed for connecting 256Kx32 and 512Kx32 devices.

Figure 2. 256K/512 x 64 SGRAM SO-DIMM Block Diagram (1 bank of two 256K/512K x 32)

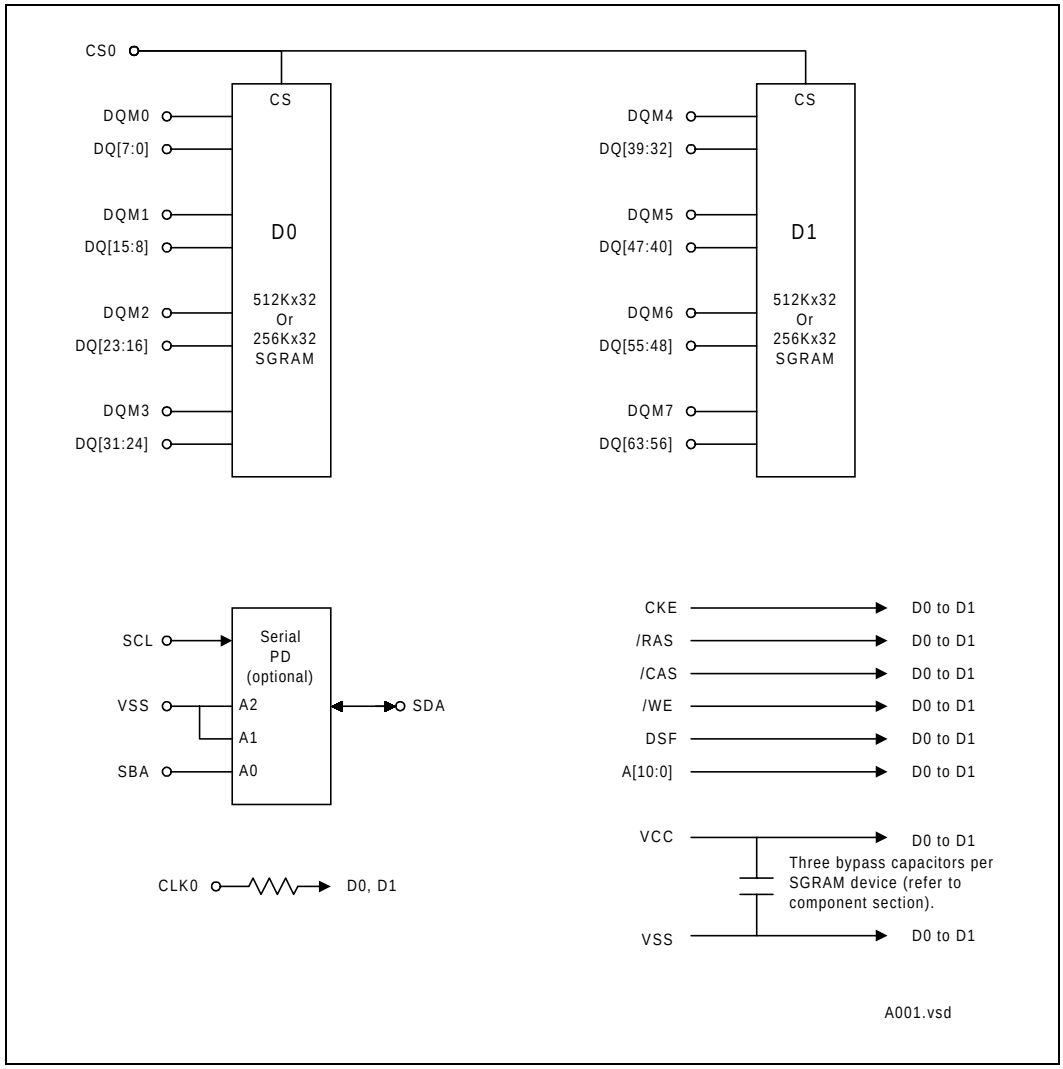


Figure 3. 512K/1M x 64 SGRAM SO-DIMM Block Diagram (2 banks of two 256K/512K x 32)

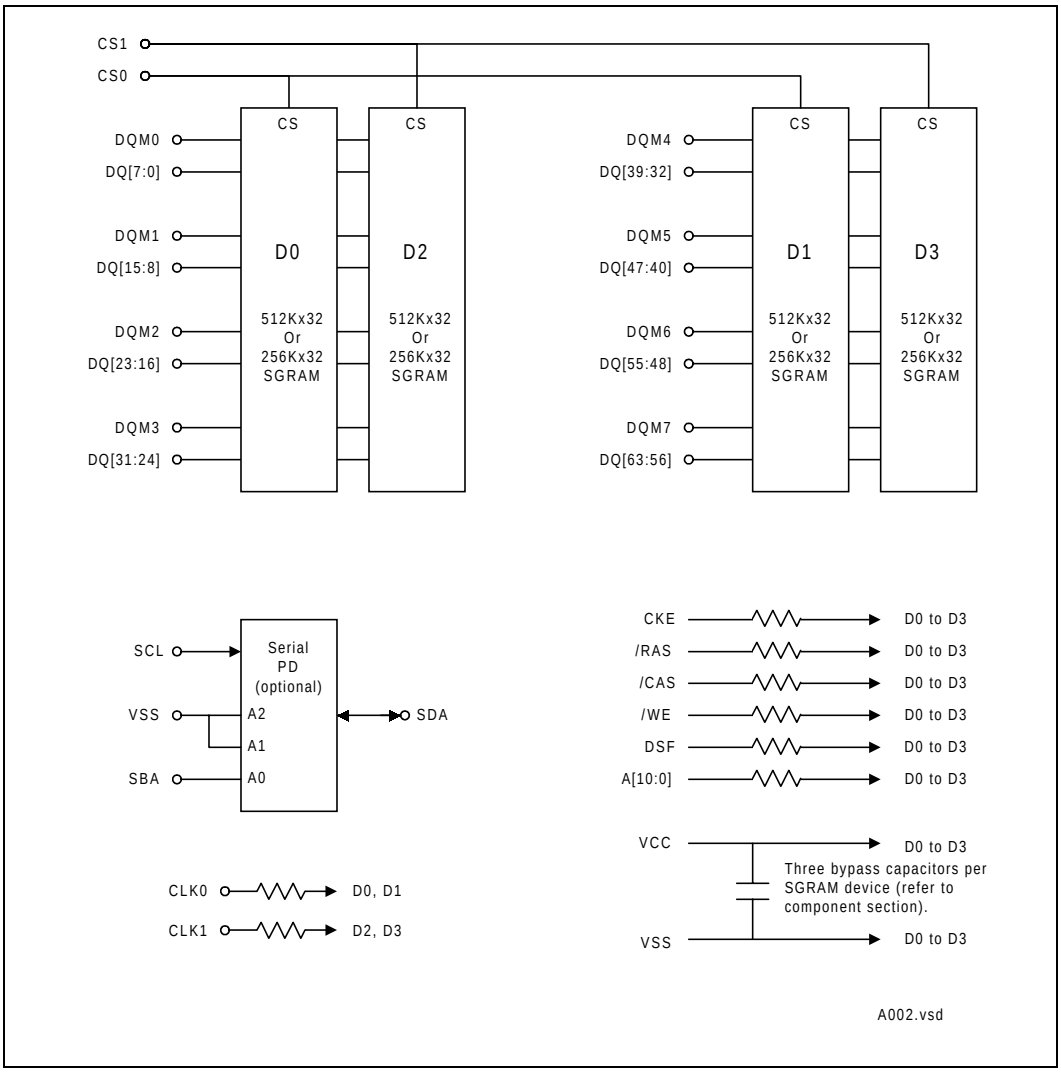


Figure 4. 256K/512K x 32 SGRAM SO-DIMM Block Diagram (1 bank of one 256K/512K x 32)

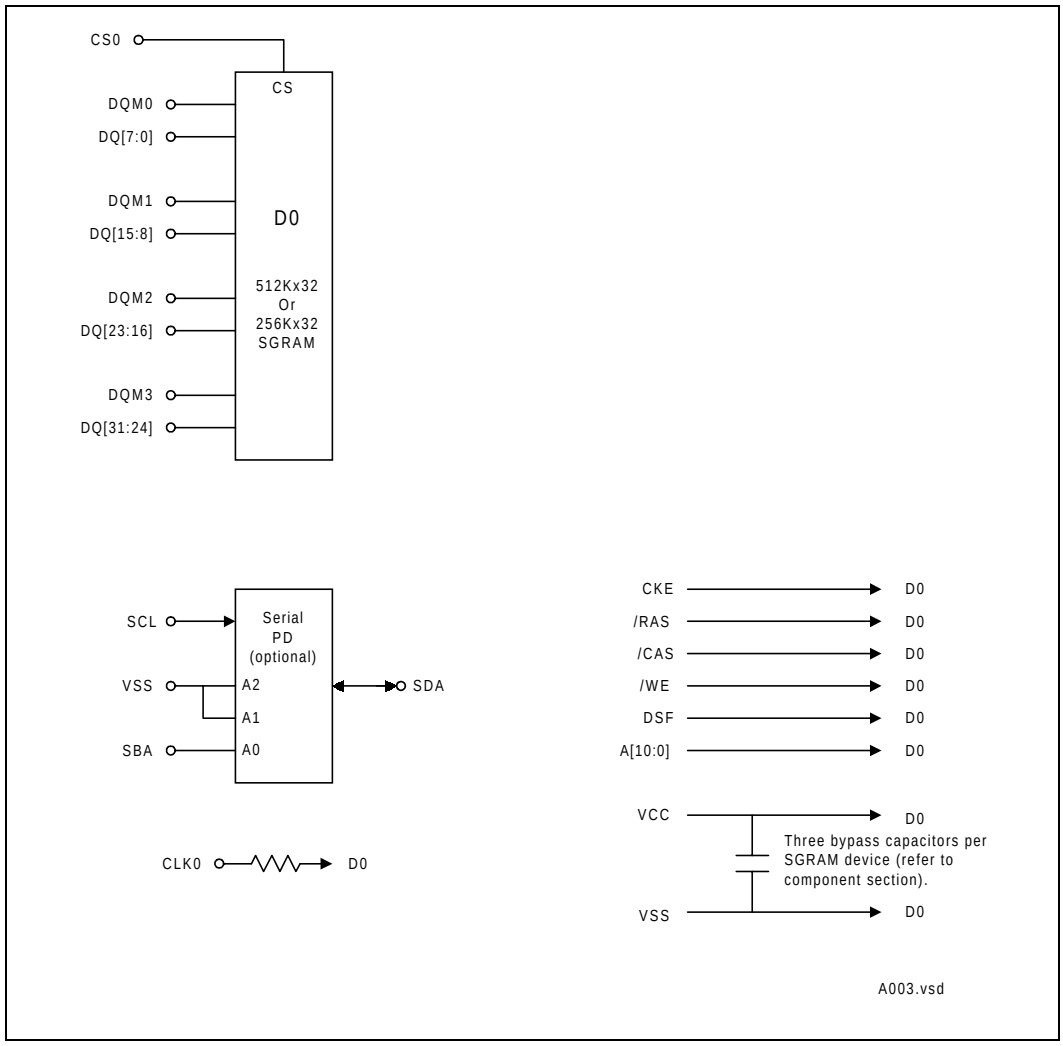
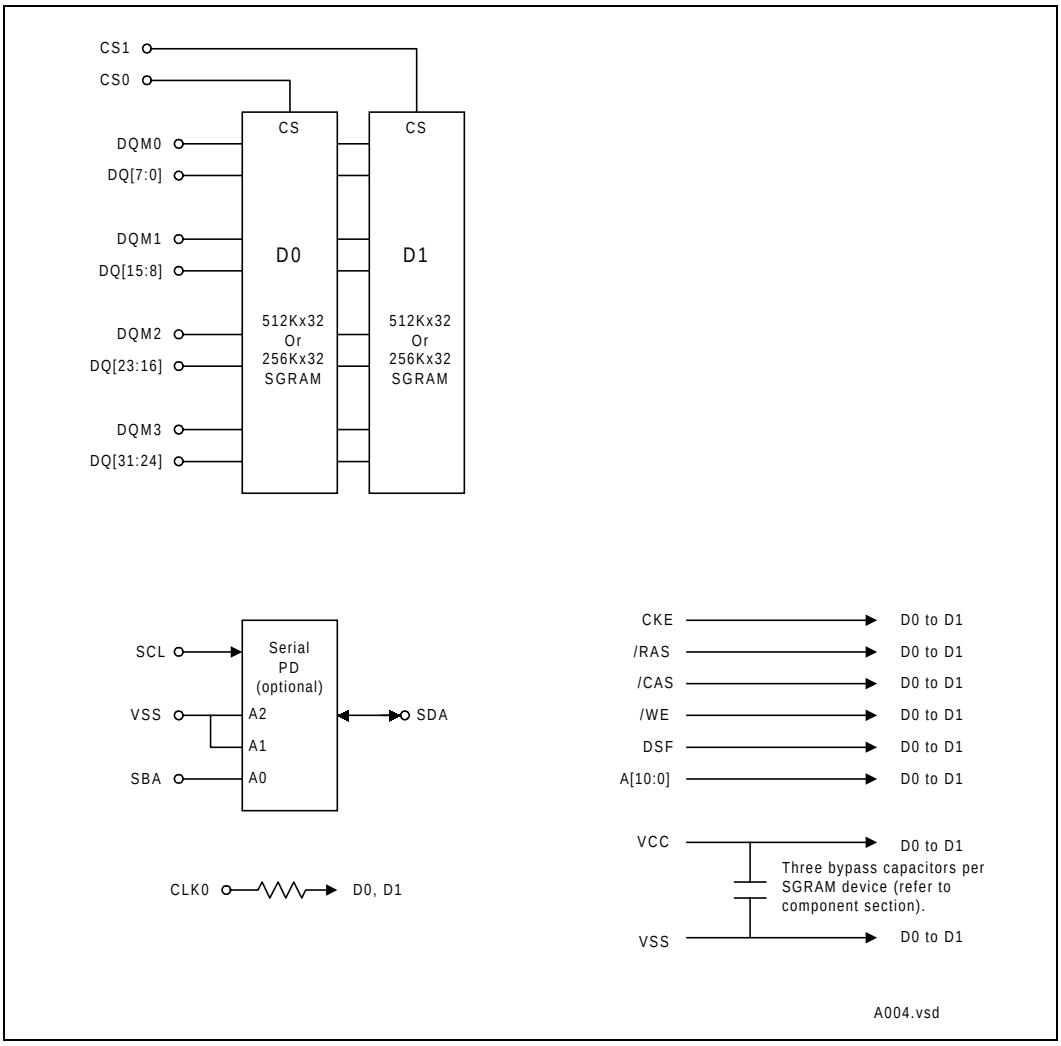


Figure 5. 512K/1M x 32 SGRAM SO-DIMM Block Diagram (2 banks of one 256K/512K x 32)



6.0 Address Translation

Table 3 should be followed for 256Kx32 and 512Kx32 SGRAM devices. This table specifies the SGRAM device to SO-DIMM connector connections for a 256Kx32 and 512Kx32 devices.

Table 3. Address Translation

SODIMM		256Kx32		512Kx32	
Pin #	Functionality	Pin #	Functionality	Pin #	Functionality
92	A0	31	A0	31	A0
91	A1	32	A1	32	A1
90	A2	33	A2	33	A2
89	A3	34	A3	34	A3
88	A4	47	A4	47	A4
87	A5	48	A5	48	A5
84	A6	49	A6	49	A6
83	A7	50	A7	50	A7
82	A8	51	A8/AP	51	A9/AP
81	A9	29	A9/BA	29	A10/BA
80	A10	No Connect	No Connect	30	A8
79	A11/Reserved	No Connect	No Connect	No Connect	No Connect

NOTES:
1. The names for pin 80, 81 and 82 are different for 256Kx32 and 512Kx32 device connection.
2. SO-DIMM's pin 80 (which is labeled as A10) is a no connect for 256Kx32 device and is connected to pin 30 (labeled as A8) of 512Kx32 device.
3. SO-DIMM's pin 81 (which is labeled as A9) is connected to pin 29 (labeled as A9/BA) of 256Kx32 device and is connected to pin 29 (labeled as A10/BA) of 512Kx32 device
4. SO-DIMM's pin 82 (which is labeled as A8) is connected to pin 51 (labeled as A8/BA) of 256Kx32 device and is connected to pin 51 (labeled as A9/AP) of 512Kx32 device.

6.1 Configuration

Graphic controllers can determine the module capabilities one of three ways; they are:

- Using the default parameters with power-up testing
- Using resistor strapping options on the data lines
- Using an optional Serial Presence Detect EEPROM

Modules are required to include resistor support (3 resistors); the Serial Presence Detect EEPROM is optional.

6.2 Default Parameters

All memory modules must meets these baseline component requirements.

Table 4. Module Baseline Component Requirements

Parameter	Min.	Max.	Unit	Notes
Clock Period	15.0		nS	
Clock High Time	5.0		nS	Rated @ 1.4V
Clock Low Time	5.0		nS	
DQM#/CS# Input Setup Time	3.0		nS	
Other Input Setup Time	3.0		nS	
DQM#/CS# Input Hold Time	1.0		nS	
Other Input Hold Time	1.0		nS	
Output Valid from Clock		11.0	nS	Rated @ 30pf
Output Hold from Clock	2.5		nS	Rated @ 30pf
CAS Latency	2	2	Tclk	
CAS to CAS Delay	1		Tclk	
CAS Bank Delay	1		Tclk	
CKE to Clock Disable	1	1	Tclk	
RAS Precharge Time	3		Tclk	
RAS Active Time	4		Tclk	
Activate to Command Delay (RAS to CAS Delay)	2		Tclk	
RAS to RAS Bank Activate Delay	2		Tclk	
RAS Cycle Time	7		Tclk	
DQM to Input Data Delay	0	0	Tclk	
Write Cmd. to Input Data Delay	0	0	Tclk	
Mode Register set to Active delay	3		Tclk	
Precharge to O/P in High-Z	2		Tclk	
DQM to Data in HiZ for read	2	2	Tclk	
Data in to Precharge	2		Tclk	
Data in to Activate/Refresh	5		Tclk	
DQM to Data mask for write	0	0	Tclk	
Number of Banks per SDRAM/SGRAM device	2	2	Banks	

Module should follow the AC timings specified in the “PC SGRAM” specification.

The graphic controller must assume that the memory is SDRAM unless it can determine that SGRAM functions (block write and write-per-bit) are available. This can be done at power-up using the DSF pin. Modules which do not support SGRAM special functions must disable the DSF pin.

The graphic device must determine the data width of the module, number of row addresses, and number of column addresses.

6.3 Resistor Strapping Options

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing. Timing information for each clock frequency is indicated in the section titled *Memory Timing*. Memory modules must meet all timing requirements within the specified operating environment.

6.3.1 Clock Frequency and Memory Timing

Cycle Time	DQ30	DQ29
15 nS	0	0
12 nS	0	1
10 nS	1	0
8 nS	1	1

6.3.2 CAS Latency

CAS Latency	DQ31
3	0
2 and 3	1

A logic low (0) indicates that the resistor strapping is tied to ground (Vss). A logic high (1) indicates that the resistor strapping is tied to Vcc. Resistors should be a 4.7 Kohm resistor on the DQ lines.

6.4 Serial Presence Detect EEPROM

This EEPROM is optional on the module. For additional information, refer to the Intel document *66 MHz Unbuffered SDRAM SO-DIMM Specification*.

7.0 Electrical Characteristics

The module electrical characteristics are carefully controlled to allow system configurations with two separate memory arrays. This allows one module to be present, plus memory soldered directly to the motherboard or add-in card PCB. Currently, two modules are not being supported. Routing on the main board will generally be done as a T-topology. The module's electrical characteristics (as well as the main board's characteristics) must be carefully implemented to insure a balanced T-topology.

The board must have a characteristic impedance between 50 and 85 ohms.

The following table lists the suggested flight time budgets for a typical graphic system using an early/late memory clock.

7.1 15 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	15.0		nS
Early/Late Clock	Tcsk	0.35	1.6	nS
Output Valid from Clock	Tac		11.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	3.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.1	0.365	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.2 12 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	12.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		9.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	3.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.3 10 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	10.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		7.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	2.5		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.4 8 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	8.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		6.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	2.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.5 A.C Timing Diagrams

Figure 6. Address/Control A.C. Timing Parameters

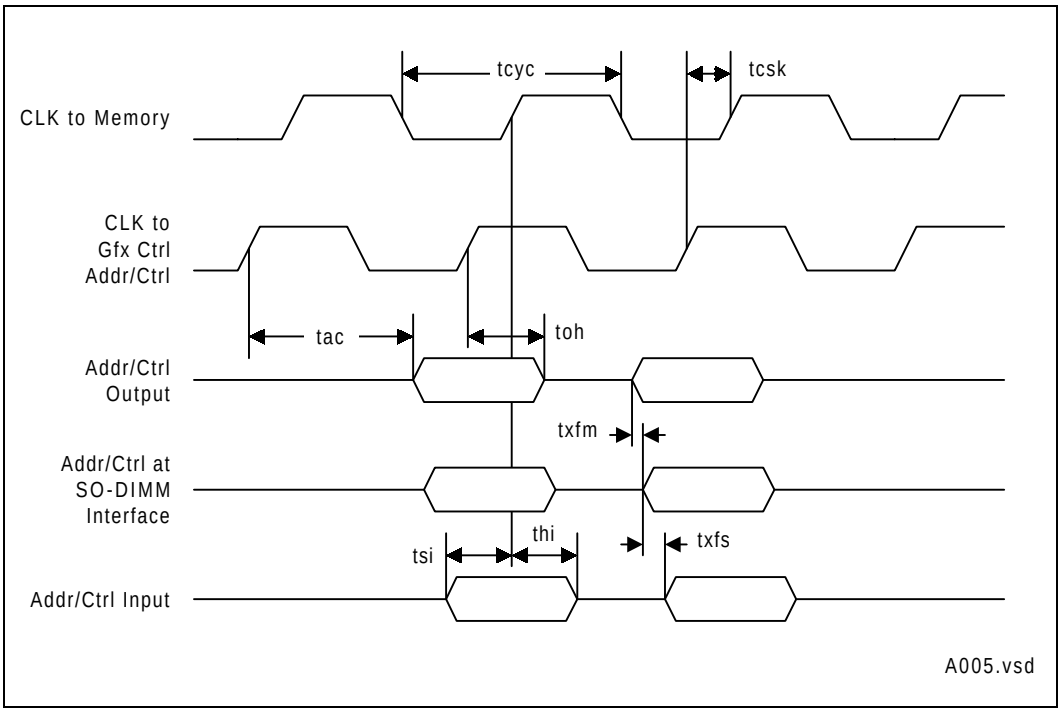


Figure 7. Data Write A.C. Timing Parameters

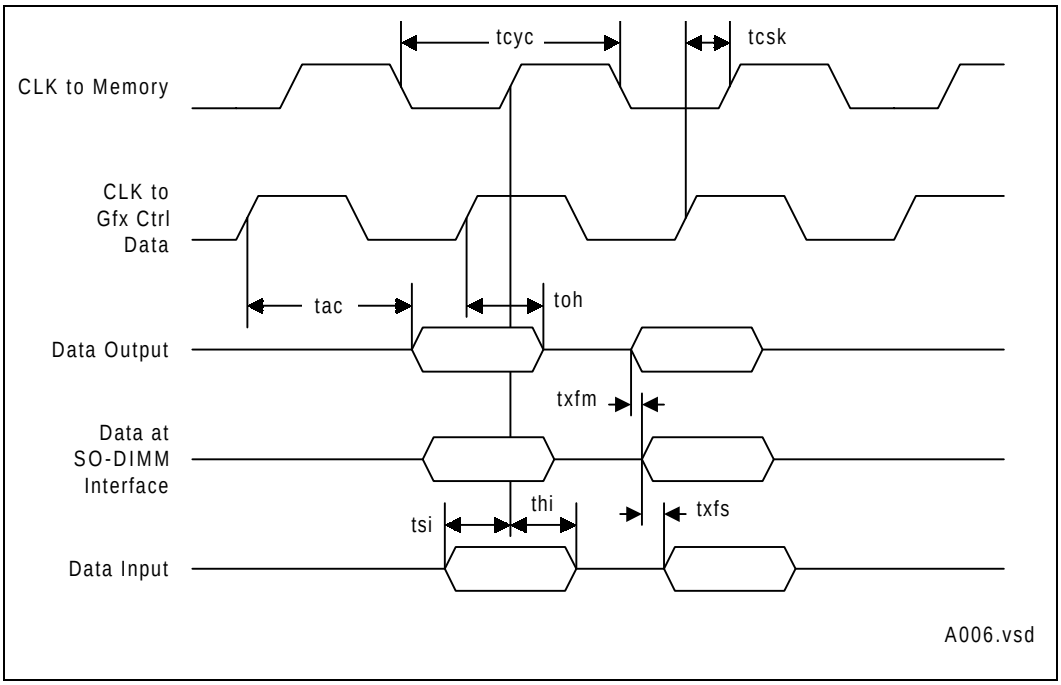
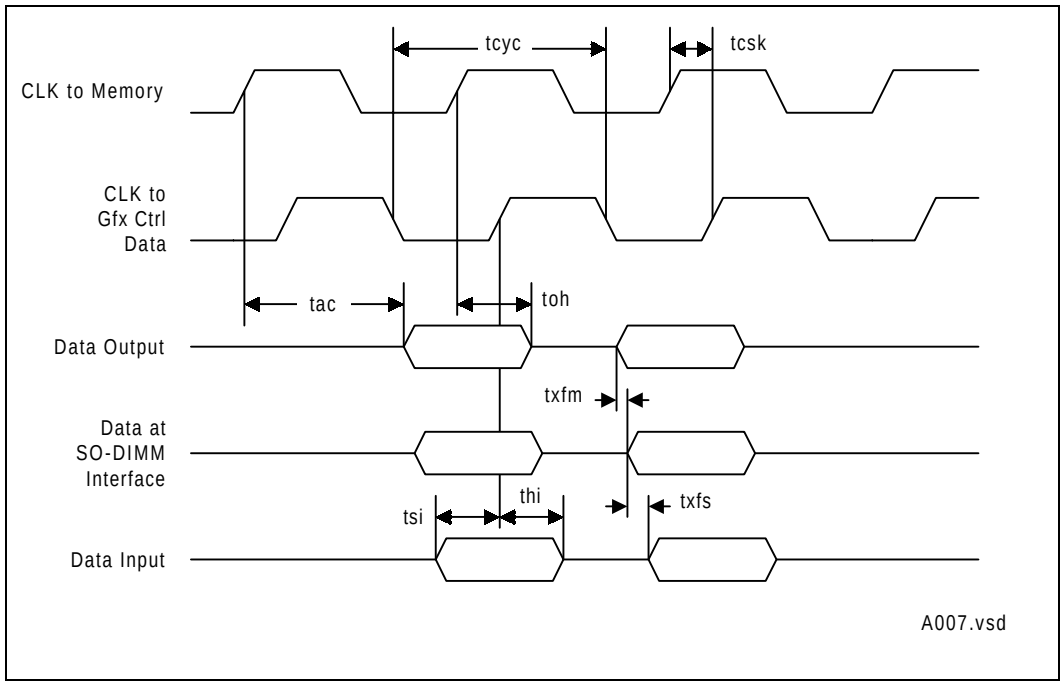


Figure 8. Data Read A.C. Timing Paramters



8.0 PCB Layout Considerations

To insure proper signal integrity, the module routing must be taken under careful considerations. This section outlines PCB layout considerations for the SO-DIMM module.

Each section looks at three separate topologies; one for clocks, one for control/address, and one for data. The assumed loading for this configuration is:

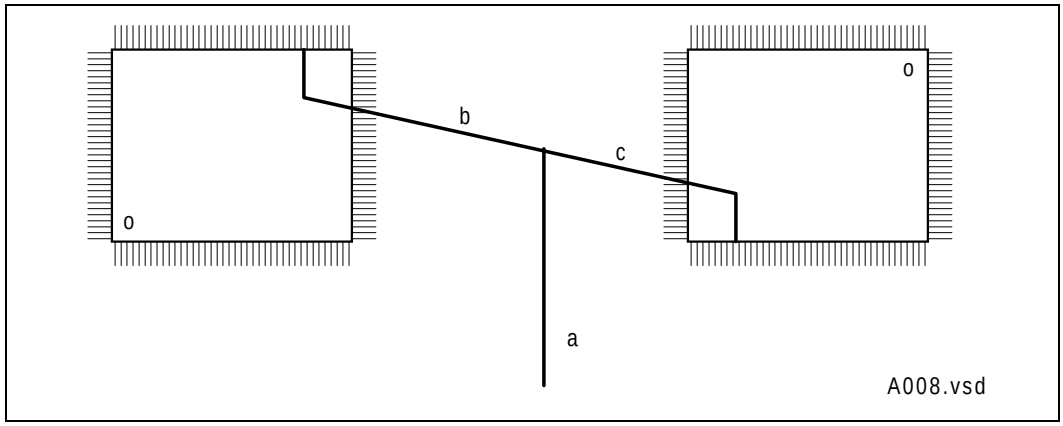
Table 5. Signal Loading

Signal	32-bit		64-bit	
	Single-sided	Double-sided	Single-sided	Double-sided
clocks	1 load	1 load	2 loads	2 loads
address/control	1 load	2 loads	2 loads	4 loads
data	1 load	2 loads	1 load	2 loads

8.1 Clock Routing and Chip Selects

Clock and chip select loading is two loads per line, maximum. Routing should be performed using a T-topology, as shown below:

Figure 9. T-Topology Clock Routing



The following table lists the allowable stub lengths for the clock and chip select routing.

Table 6. Stub Lengths (Clock and Chip Select Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	75	150	75	150	75	150	75	150	pS
b	0	115	0	115	0	115	0	115	pS
c	0	115	0	115	0	115	0	115	pS
b+c	0	225	0	225	0	225	0	225	pS
Total Length (clock)	100	365	175	325	175	325	175	325	pS
Total Length (chip select)	0	365	0	365	0	365	0	365	pS

8.2 Address/Control Routing

The following table lists the allowable stub lengths for the address/control routing.

Figure 10. Address and Control Routing

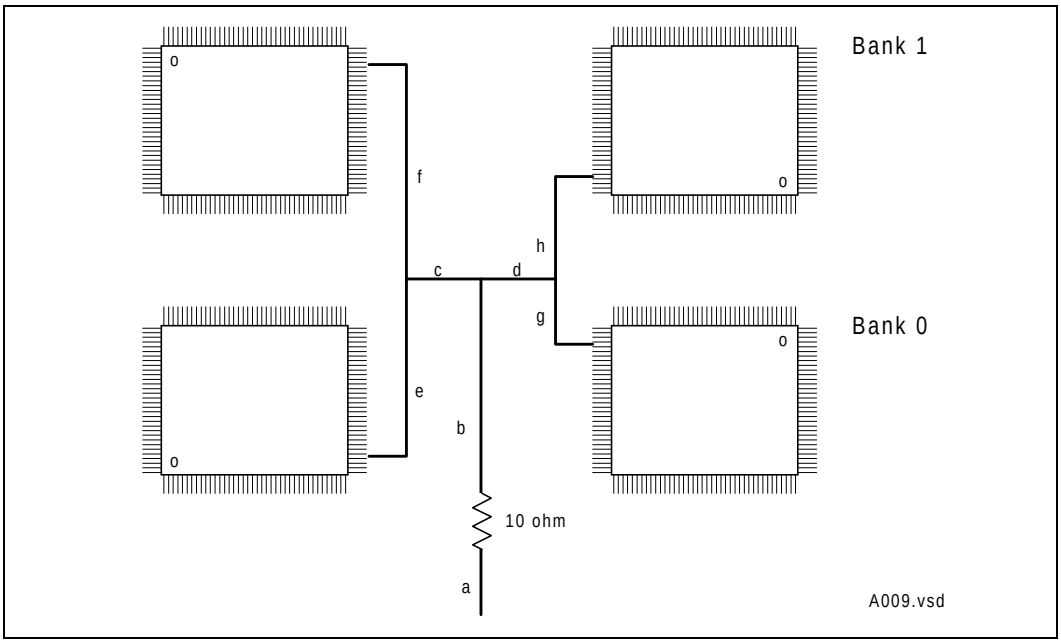


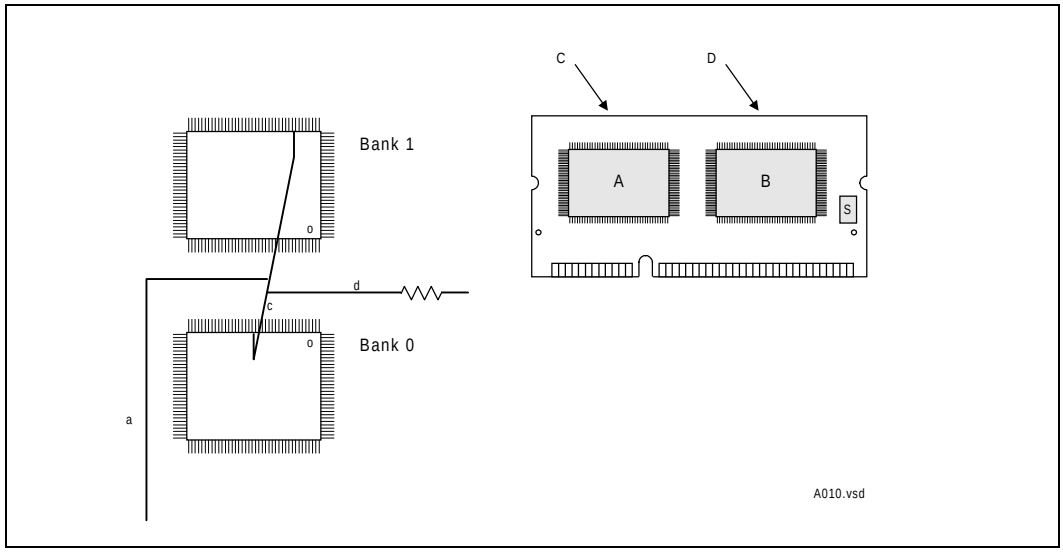
Table 7. Stub Lengths (Address/Control Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	0	37	0	37	0	37	0	37	pS
b	0	190	0	190	0	190	0	190	pS
c	0	115	0	115	0	115	0	115	pS
d	0	115	0	115	0	115	0	115	pS
e	0	115	0	115	0	115	0	115	pS
f	0	115	0	115	0	115	0	115	pS
g	0	115	0	115	0	115	0	115	pS
h	0	115	0	115	0	115	0	115	pS
b-c	-75	75	-75	75	-75	75	-75	75	pS
b-d	-75	75	-75	75	-75	75	-75	75	pS
c+e	0	190	0	190	0	190	0	190	pS
c+f	0	190	0	190	0	190	0	190	pS
d+g	0	190	0	190	0	190	0	190	pS
d+h	0	190	0	190	0	190	0	190	pS
total length	0	375	0	375	0	375	0	375	pS

8.3 Data Routing

Data lodading is two loads per line, maximum. Routing should be performed using a T-topology, as shown below.

Figure 11.Data Routing



Byte-ordering (along with the respective Data Mask, DQM) within the SDRAM/SGRAM should be swapped to optimize routing.

Table 8. Byte Ordering

Module Byte	Front-Side Memory Byte	Back-Side Memory Byte	*n* value
BYTE 0	Memory B; BYTE 0	Memory D; BYTE 3	*n* = 115 pS
BYTE 1	Memory B; BYTE 3	Memory D; BYTE 0	*n* = 35 pS
BYTE 2	Memory B; BYTE 1	Memory D; BYTE 2	*n* = 35 pS
BYTE 3	Memory B; BYTE 2	Memory D; BYTE 1	*n* = 115 pS
BYTE 4	Memory A; BYTE 1	Memory C; BYTE 2	*n* = 115 pS
BYTE 5	Memory A; BYTE 2	Memory C; BYTE 1	*n* = 35 pS
BYTE 6	Memory A; BYTE 0	Memory C; BYTE 3	*n* = 35 pS
BYTE 7	Memory A; BYTE 3	Memory C; BYTE 0	*n* = 115 pS

The following table lists the allowable stub lengths for the data line routing.

Table 9. Stub Lengths (Data Line Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	n	n+75	n	n+75	n	n+75	n	n+75	pS
b	0	75	0	75	0	75	0	75	pS
c	0	75	0	75	0	75	0	75	pS
d	0	125	0	125	0	125	0	125	pS
total length	0	n+150	0	n+150	0	n+150	0	n+150	pS

Stub *d* is used for the strapping resistors on DQ29-DQ31, and is optional.

9.0 Electrical Specifications

The following information is from the Intel *PC SDRAM* Specification, version 1.1, April 1996. It is provided here for convenience

9.1 SDRAM/SGRAM Component Absolute Maximum D.C. Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	VCC + 0.5	V
VCC, VCC_Q	Voltage Supply pins w.r.t V_{SS}	-0.5	4.5	V
Ts	Storage Temperature	-55	125	°C
PD	Power Dissipation		1	W

9.2 SDRAM/SGRAM Components D.C. Operating Requirements

Table 11. D.C. Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units	Notes
VCC	Supply Voltage		3.0	3.6	V	
VCCQ	I/O Supply Voltage		3. 0	3.6	V	
Iil	Input Leakage Current	0 < Vin < VCCQ	-5	+5	µA	1,2
Voh	Output High Voltage	Ioh = -4 mA	2.4		V	
Vol	Output Low Voltage	Iol = 4 mA		0.4	V	
Cin	Input/Clock Pin Capacitance			5	pF	
CI/O	I/O Pin Capacitance			7	pF	
Lpin	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	65	°C	

NOTES:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

9.3 SDRAM/SGRAM Components Absolute Maximum A.C. Operating Requirements

Table 12. Absolute Maximum A.C. Operating Requirements

Symbol	Parameter	Min.	Max.	Units	Notes
Vih	Input High Voltage	2.0	VCCQ + 1.5	V	1
Vil	Input Low Voltage	VSSQ – 1.5	0.8	V	1

NOTE: The overshoot and undershoot voltage duration is ≤5ns with no input clamp diodes.

9.4 Memory Timing

Individual DRAM component devices are required to follow the AC timings specified in the Intel “PC SGRAM” specification. Devices which can not meet the minimum timing set forth. must program a lower clock speed.

Appendix A PCB Layout

This section show an example of a PQFP/TQFP SO-DIMM module routed as a six-layer PCB.

Figure 12.Silk Screen - Primary Side

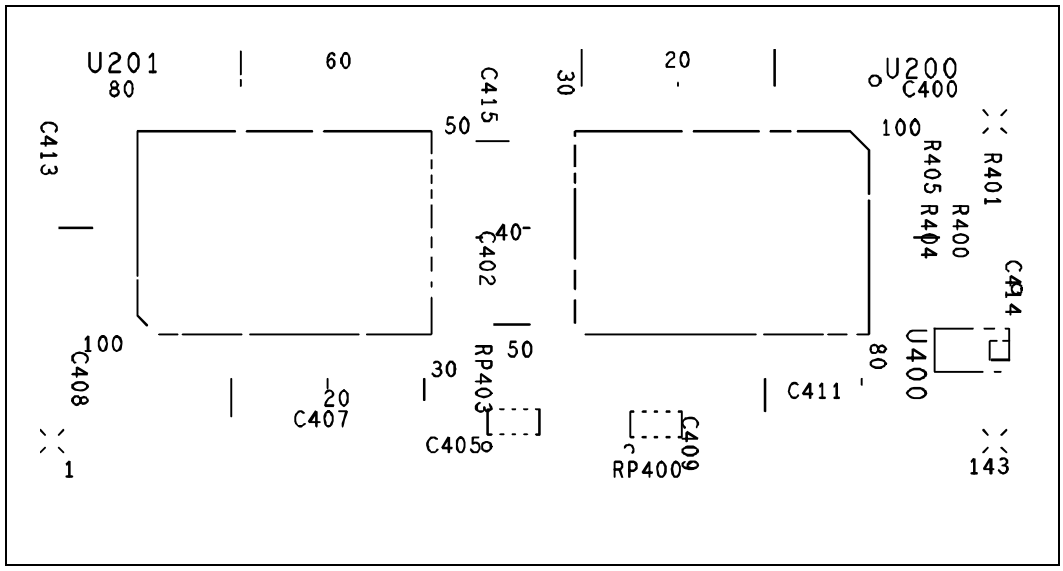


Figure 13.Silk Screen - Secondary Side

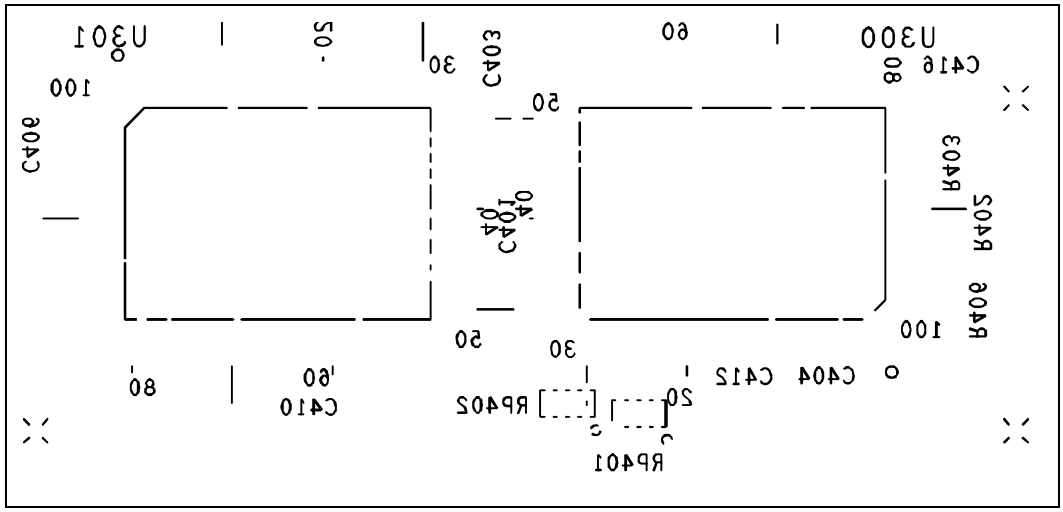


Figure 14.Primary Side (layer 1)

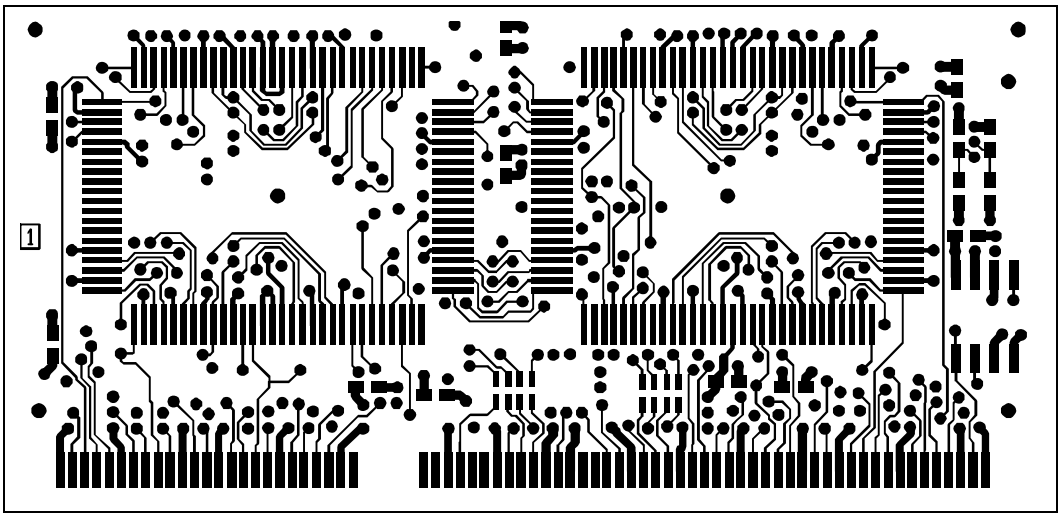


Figure 15.VCC Plane (layer 2)

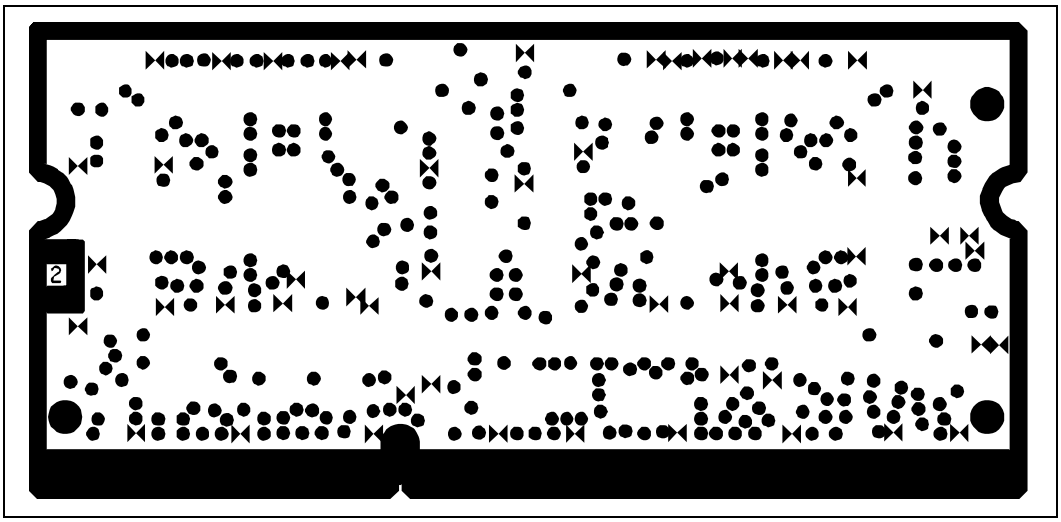


Figure 16.Inner-Signal (layer 3)

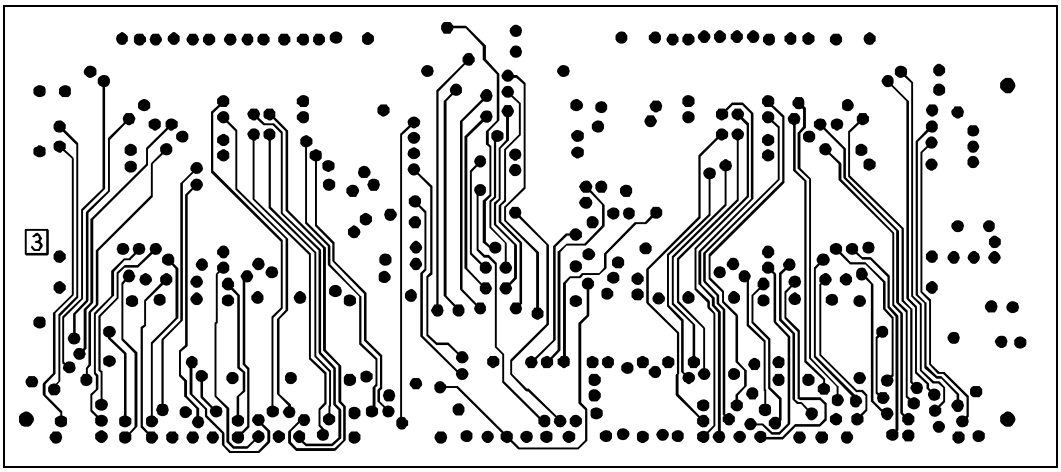


Figure 17.Inner-Signal (layer 4)

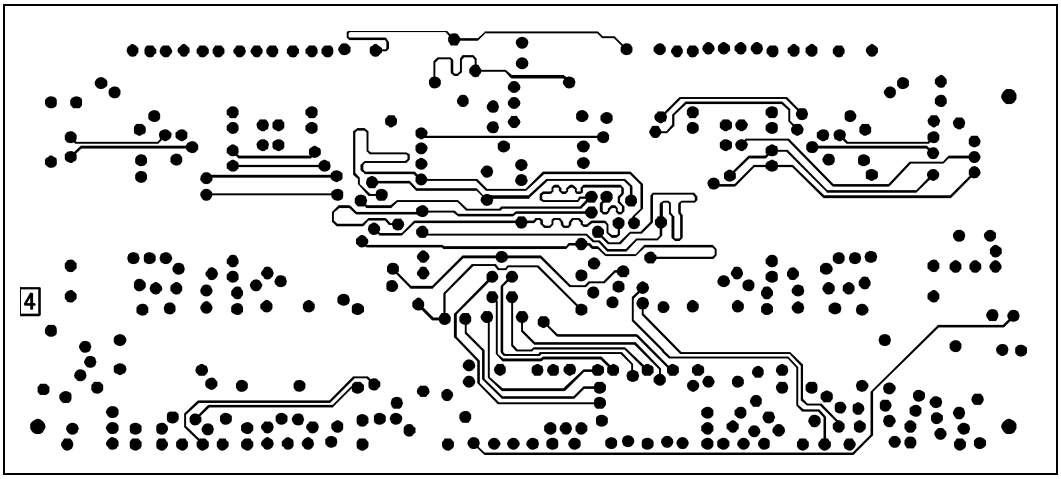


Figure 18.Ground Plane (layer 5)

Figure 19.Secondary Side (layer 6)