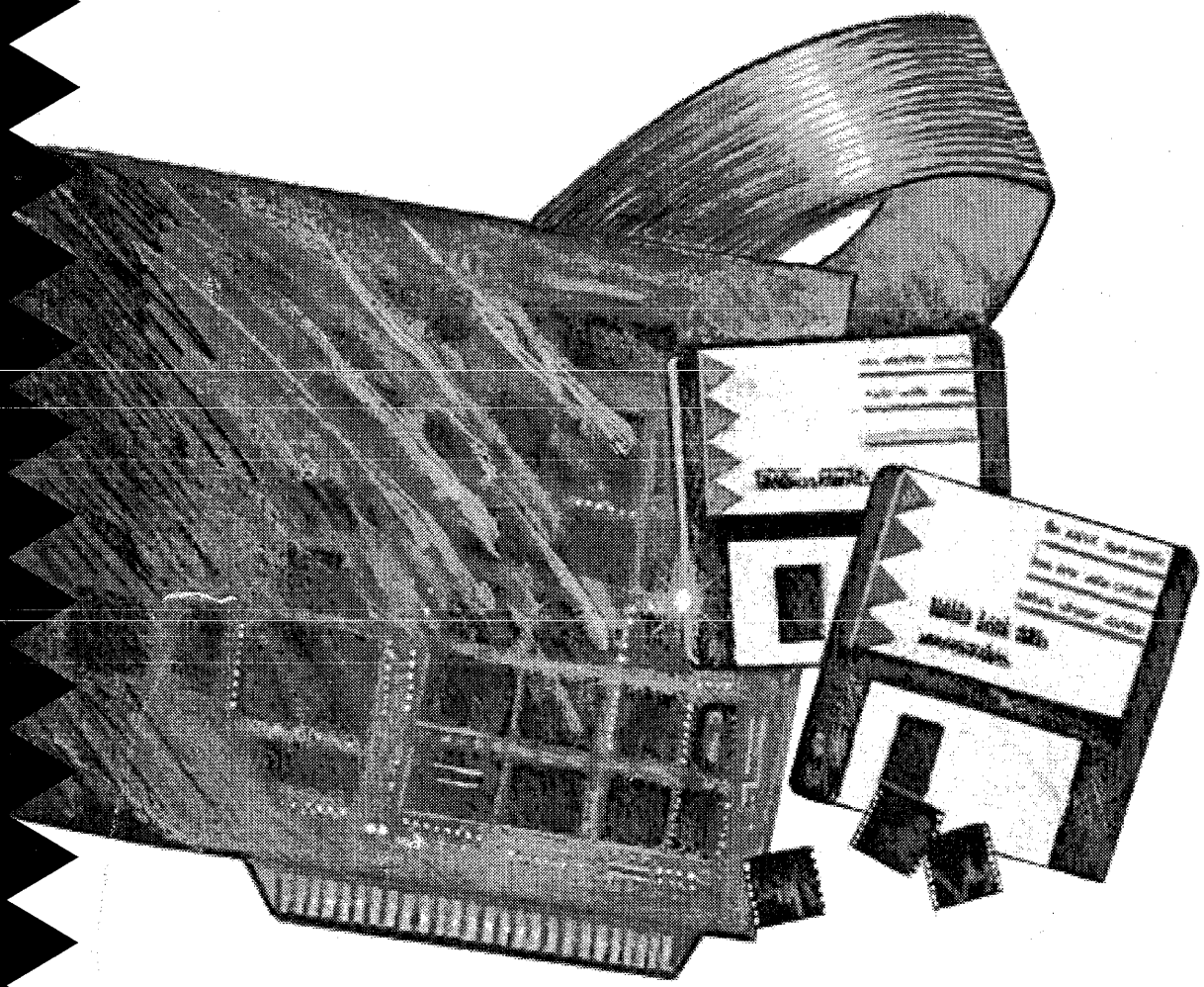
Data Book



AIC-7890A/7891, Rev. C

PCI Bus Master Ultra2 SCSI Host Adapter Chip

Stock Number: 511683-00, Rev B. 8/98

adaptec®

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Printed in Singapore
STOCK NO: 511683-00, Rev B. SG 8/98

▼▼▼▼▼ Adaptec AIC-7890A/7891

PCI Bus Master Ultra2 SCSI Host Adapter Chip

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1

Introduction

This *Data Book* documents the "C" version of the AIC-7890A and AIC-7891 single-chip host adapters. The AIC-7890A/7891 "C" version introduces several features and functions that were not available in earlier "A" version of the chip. The version level of the chip is indicated by the first character in the third line of the text on the chip package as shown in Figure 1-1.

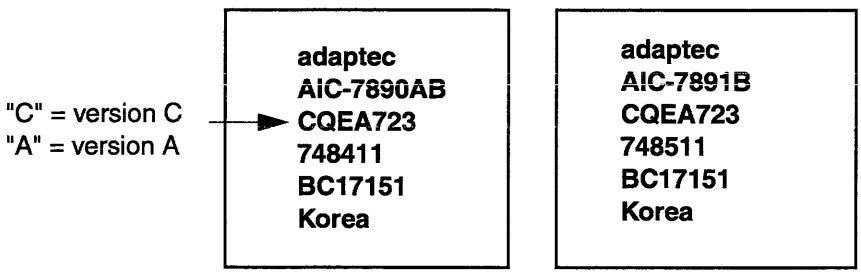


Figure 1-1. AIC-7890A/7891 Chip Package

The new features of version "C" of the AIC-7890A/7891 chip are:

- Enhanced Microsoft PC98 compliance
- Support for changeable PCI IDs through software and hardware

The AIC-7890A and AIC-7891 provide advanced host adapter features in a single 272-pin Ball Grid Array (BGA) chip. The AIC-7890A provides an Ultra2 SCSI bus controller combined with a full-featured PCI 2.1-compliant 32-bit bus master capable of supporting zero wait state 32-bit memory data transfers at 133 MBytes/sec data burst rate. The AIC-7891 provides an Ultra2 SCSI bus controller combined with a full-featured PCI 2.1-compliant 64-bit bus master capable of supporting zero wait state 64-bit at 267 MBytes/sec data burst rate. The PCI interface of the AIC-7891 can also function as a PCI 2.1-compliant 32-bit bus master with zero wait state 32-bit memory transfers at 133 MBytes/sec data burst rate. The AIC-7890A and AIC-7891 are identical devices with the exception of the 64-bit capability of the AIC-7891. Hereinafter they are referenced as the AIC-7890A/7891. The AIC-7890A/7891 Ultra2 SCSI controllers comply with SCSI-3 standard and are compatible with single ended (SE) or dual mode Low Voltage

Differential (LVD) SCSI I/O. Support for external High Voltage Differential (HVD) transceivers is provided.

Note: This document describes the functionality and features of the "C" revision of the AIC-7890A and AIC-7891 chips.

The data channel DMA engine in the AIC-7890A/7891 supports data transfer rates up to 80 MBytes/sec on a wide (16-bit) SCSI bus using LVD SCSI I/Os. The AIC-7891's 64-bit PCI interface supports up to 267 MBytes/sec transfer rates. A 512-byte data FIFO is embedded in the AIC-7890A/7891 to buffer data between the PCI bus and Ultra2 SCSI bus. The 512 byte data FIFO allows more efficient utilization of both the PCI and SCSI bus by reducing the number of unnecessary wait states on the PCI bus or disconnects on the SCSI bus. The data FIFO can serve as a temporary storage for the sequencer.

Beside the data channel DMA engine, a dedicated command channel DMA engine in the AIC-7890A/7891 can be used to bring in SCSI commands described by Sequencer Control Blocks (SCBs) and the scatter/gather lists associated with each SCB. The SCB data structure and scatter/gather lists contain all the information needed for the execution of the command. This command channel can allow new commands to be brought into the chips while the data channel is executing the existing commands. The command channel provide a 128-byte buffer for the scatter/gather lists and a 64-byte buffer as a temporary SCB storage which allows more efficient utilization of the PCI bus.

The AIC-7890A/7891 provide an improved version of the internal RISC-based sequencer, which is capable of executing instructions at 20 MIPS. The sequencer executes SCBs to initiate data transfers between the PCI and SCSI interfaces. The AIC-7890A/7891 sequencer supports variable execution speeds of 10/20 MIPS and provides 768x32 bits of SRAM microcode storage.

In addition to the 64/32-bit PCI interface, Ultra 2 SCSI interface, 512-byte Data FIFO, command channel, and RISC based sequencer, the AIC-7890A/7891 provide 80 bytes of scratch SRAM, embedded storage for 16 SCBs, and a FLEX Port. The FLEX Port can be used to access external SRAM/ROM/FLASH EPROM/SEEPROM/external logic. The SCB array containing the 16 SCBs can be expanded to 256 SCBs with external SRAM accessed through the FLEX Port.

The components of the AIC-7890A/7891 combines to provide a full feature Ultra 2 SCSI host adapter with a 64-bit PCI interface on the AIC-7891 and a 32-bit on the AIC-7890A in a single 272-pin BGA chip which is compatible to current generation 32-bit PCI architecture and existing SCSI-2 and Ultra SCSI peripherals.

Feature Summary

PCI Interface

- Supports programmable PCI configuration registers, Subsystem ID and Subvendor ID, through external pinor software (BIOS or BDK)
- Direct pin out connection to PCI 64/32-bit bus interfaces
- PCI 64-bit bus master with zero wait state 64-bit memory data transfers up to 267 MBytes/sec for AIC-7891

- PCI 32-bit bus master with zero wait state 32-bit memory data transfers up to 133 MBytes/sec for AIC-7890A
- PCI down-shift 64 to 32-bit bus master with zero wait state 32-bit memory data transfers up to 133 MBytes/sec for AIC-7891
- Supports both single and dual address cycle
- Supports PCLK frequencies from 0 to 33.3 MHz
- Supports programmable Latency Timer, Cache Size, and Interrupt Line Select registers
- Supports PCI Power Management
- PCI bus access of AIC-7891 or AIC-7890A device registers from both PCI I/O address space and PCI Memory address space
- Medium PCI target device-select response time, DAC cycles support for target
- Capable of streaming PCI enhanced memory data Read and Write commands as PCI bus master
- PCI bus address and data parity generation and checking
- Supports PCI PERR# and SERR# requirements
- Master data transfers are initiated by selected cacheline size and Data FIFO threshold
- PCI bus address phase and data phase error generation for checking system and device error support
- PCI configuration space register accessible through PCI I/O or Memory address space
- PCI target latency of 16 clocks maximum for first target access cycle (revision 2.1 support)
- Hardware PCI bus utilization monitor
- Supports external ROM system byte/word/dword read access and byte write access

SCSI Interface

- SCSI data transfers up to 40 Mega-transfers/sec.
- 8- or 16-bit SCSI data path
- SCAM level 2 support
- SCSI Offsets to 127 transfers
- Compatible with single ended or dual mode Low Voltage DIfferential (LVD) SCSI I/O
- Supports for external High Voltage Differential (HVD) transceivers
- Extensive hardware support for disconnect/reconnect and scatter/gather
- Full support for both initiator and target operations
- Multi target I.D. lets chip respond to multiple I.Ds as a SCSI target
- Hardware SCSI bus utilization monitor

Sequencer

- Variable execution speed of 10/20 MIPS RISC design
- Internal 3 KByte SRAM for microcode storage with parity protection and RAM Built-In-Self-Test (BIST) function
- Fifteen instruction group types
- Operation can be paused by the software driver
- Diagnostic instruction single-step and hardware address breakpoint

Command Channel

- Dedicate DMA engine to fetch SCBs from system memory and to post command done status to the system memory
- 128 bytes of internal RAM with parity protection for holding scatter/gather list elements for current command execution
- 64 bytes of internal RAM with parity protection for holding SCBs temporarily before moving to on or off chip SCB array SRAM

Data FIFO

- 512-byte data FIFO with BIST function
- Parity protection for each byte transferred

Sequencer Control Block / FlexPort

- 80 bytes of dual-ported scratch RAM with parity protection and BIST function
- Internal 1-KByte SCB array with parity protection and BIST function for storage of sixteen SCBs
- SCB array expandable to 256 SCBs with external 16-KByte SRAM
- Single ported 8- or 9-bit SRAM (20 ns access) with direct connection for 16 KBytes
- Single ported 8-bit ROM/EEPROM (150 ns access) with direct connection for 128 KBytes
- Serial SEEPROM with register based access with hardware timer support
- Multi-device arbitration (two wire) for sharing FLEXPort connected devices
- SRAM, ROM, EEPROM three line interface for read/write control
- SEEPROM four line interface
- External eight line interface for general read/write purpose

AIC-7890A/7891 Block Diagram

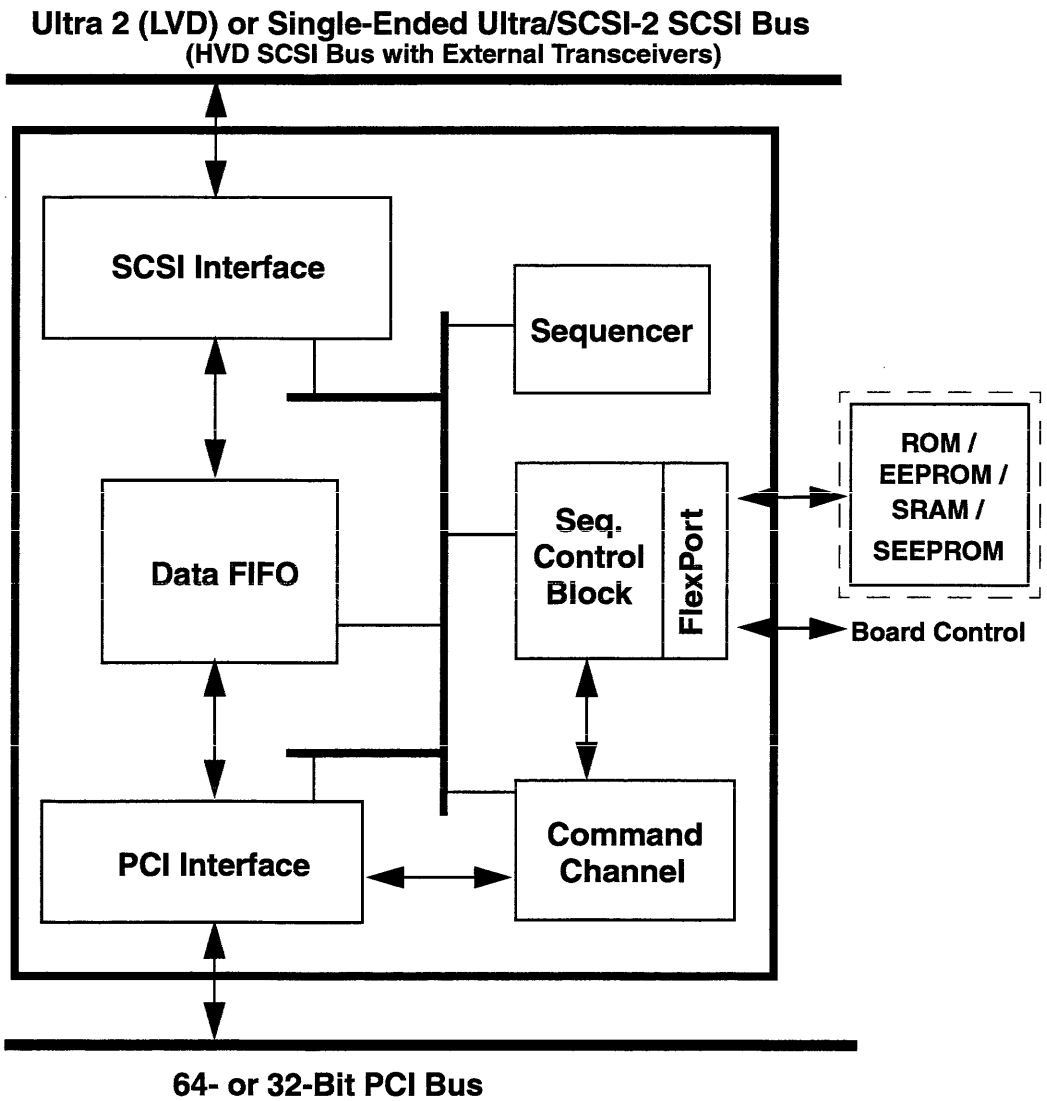


Figure 1-2. AIC-7890A/7891 Block Diagram

2

Pin Description

Pin Signal Summary

The pins are summarized here, listing the name, pin number, if the pin is an input, and the type and drive of the outputs. The type definitions are listed in Table 2-1.

Table 2-1. Pin Type Definitions

Type	Definition
analog-in	**Analog Input**.
analog-out	**Analog output**.
Dual Mode I/O	**Dual Mode LVD SCSI I/O Pins**. They are organized in pairs, two pins per SCSI signal. This pins act as either Low-Voltage-Differential (LVD) SCSI or Single Ended (SE) SCSI depending on the voltage on the DIFFSENSE input.
gnd	**Ground**.
in	**Input** indicates that this pin has a standard input receiver.
ts/#	**Three-state** is an output signal with control enabled output driver. # is the min drive current in mA.
sts/#	**Sustained Three-state** is a bidirectional signal, active low three-state signal and driven by one, and only one agent at a time. The agent that drives an in-sts signal low must drive it high for at least one PCLK before letting it float. A new agent cannot start driving an in-s/t/s signal any sooner than one clock after the previous owner floats it. A pull-up sustains the inactive state until another agent drives it and is provided by the PCI bus central resource. # is the min drive current in mA.
od/#	**Open Drain** is an open drain output. The system board provides a light pull-up for o/d signals. Multiple devices share the signal as a wire-OR. The signal is asserted synchronous with PCLK for one PCLK period. The signal deassertion period is determined by the RC time period provided by the pull-up. # is the min drive current in mA.
pu	**Pull-up** indicates that this pin has an internal pull-up resistor. The resistor is approximately 50 Kohms.
pwr	**Power**.

PCI Host Interface Pins

Table 2-2. PCI Host Interface Pins

Signal Name	Pin Number	PCI Master I/O Driver Type	PCI Target I/O Driver Type	Notes
ACK64#	M1	in	in	2
AD[31:00]	T1, V2, U1, W2, V1, W3, W1, W4, Y2, W6, Y3, W7, Y4, W8, Y6, W9, W14, Y15, W15, Y16, W16, Y18, W17, Y19, W20, W19, V20, V19, U20, U19, T20, T19	in-ts/6	in-ts/6	
AD[63:32]	N3, V6, P4, V7, P3, V8, R3, V9, T4, V10, T3, V11, U5, V12, U7, V13, U9, V14, U11, V15, U12, V16, U14, V17, U16, V18, T17, U18, R18, T18, P17, R19	in-ts/6	in-ts/6	2
CBE[3:0]#	Y1, Y8, Y14, W18	in-ts/6	in-ts/6	
CBE[7:4]#	V3, M4, V4, M3	in-ts/6	in-ts/6	2
DEVSEL#	Y10	in	sts/6	1
FRAME#	W10	sts/6	in	1
GNT#	U2	in	NA	
IDSEL	W5	NA	in	
IRDY#	Y9	in-sts/6	in	1
PAR	W13	in-ts/6	in-ts/6	
PAR64	V5	in-ts/6	in-ts/6	2
PCLK	L3	in	in	
PERR#	Y12	in-sts/6	in-sts/6	1
PREQ#	R1	ts/6	NA	
REQ64#	U3	ts/6	NA	2
PCIRST#	T2	in	in	
SERR#	Y13	in	od/6	1
STOP#	W12	in	sts/6	1
TRDY#	W11	in	sts/6	1
IRQA#	R2	od/6	ts/6	1

[1] Signal requires external pull-up resistors.

2 Those signals are for AIC-7891 only, and are not required to be connected for 32-bit PCI systems. Those pins do not exist for AIC-7890A, and are defined as N/C.

SCSI Interface Pins

Table 2-3. SCSI Interface Pins

Signal Name	Pin Number	I/O Driver Type	Notes
SCDP15-SCDP8	J4, J2, K3, L1, C12, B11, A11, B10	Dual Mode I/O	
SCDM15-SCDM8	J3, J1, K1, L2, B12, C11, A10, C10	Dual Mode I/O	
SCDP7-SCDP0	B2, B1, D3, C1, E3, F3, F2, G2	Dual Mode I/O	
SCDM7-SCDM0	A2, C2, E4, D1, E2, G4, F1, G1	Dual Mode I/O	
SCDPHP, SCDPHM	H2, H1	Dual Mode I/O	
SCDPLP, SCDPLM	C4, B3	Dual Mode I/O	
CDP, CDM	A8, B8	Dual Mode I/O	
IOP, IOM	A9,B9	Dual Mode I/O	
MSGP, MSGM	A6,C7	Dual Mode I/O	
REQP, REQM	C9, D9	Dual Mode I/O	
ACKP, ACKM	C6, B5	Dual Mode I/O	
RESETP, RESETM	B6, A5	Dual Mode I/O	
SELP, SELM	A7, B7	Dual Mode I/O	
BSYP, BSYM	A4, C5	Dual Mode I/O	
ATNP, ATNM	B4, A3	Dual Mode I/O	
DIFFSENSE	A15	analog-in	
EXTXCVR#	C16	in-pu	
LED#	A19	ts/24	
LVREXT	C13	analog-out	1
SEREXT	A14	analog-out	2
STPWCTL	C15	ts/4	
WIDEPS#	B16	in-pu	
EXPACT	A16	in	3

[1] A 10K +/- 1% ohms resistor should be connected between pins C13 and D12.
[2] A 11.8K +/- 1% ohms resistor should be connected between pin A14 and the analog ground.
[3] This signal must be pulled low by an external resistor or by tying to ground when this signal is not connected to AIC-3860.

FlexPort (Memory) Interface Pins

Table 2-4. FlexPort (Memory) Interface Pins

Signal Name	Pin Number	I/O Driver	Notes
BRDOE#	B17	ts/4-pu	
BRDWE	B18	out/4	
EXTARBACK#	E18	in-pu	
EXTARBREQ#	E17	ts/4-pu	
EXTPAUSE#	A17	in-pu	
MA[15:0]	B20, C19, C20, D19, D20, E19, E20, F19, F20, G19, H19, H20, J19, K19, K20, L20	ts/8-pu	
MD[7:0]	G17, G18, H18, J17, J18, K17, K18,	in-ts/8-pu	
MDP	C18	in-ts/8-pu	
MRW	M20	ts/8-pu	
RAMCS#	M19	ts/24-pu	
RAMPS#	N20	in-ts/4-pu	
ROMCS#	M18	ts/8-pu	
SEECS	M17	ts/4	1

[1] This signal requires an external pull-down resistor.

Clock and Miscellaneous Pins

Table 2-5. Clock and Miscellaneous Pins

Signal Name	Pin Number	I/O Driver	Notes
CLKIN	D16	in	
SCLKIN	D14	in	1
IDDAT	N19	in-pu	
EXTPAUSE#	A17	in-pu	
PULLUP1	M1	in	2
PULLUP2	U3	in	2

[1] This signal must be tied high or low if not used.
[2] AIC-7890A only. This signal must be pulled up to PVCC with a 10 Kohm resistor.

Test Pins

Table 2-6. Test Pins

Signal Name	Pin Number	I/O Driver	Notes
TCK	N1	in	1
TDI	P2	in	1
TDO	P1	ts/6	
TMS	N2	in	1
TRST#	M2	in	2
PDPUDIS#	R20	in	3
TESTMODE#	P19	in	4

[1] This signal must be tied high or low if not used.
[2] This signal must be tied low if not used.
[3] This signal must be tied to a known state. See *Pin Signal Description* for more details.
[4] This signal must be tied high during normal operation.

Power and Ground Pins

Table 2-7. Power and Ground Pins

Signal Name	Pin Number	I/O Driver	Notes
AVCC1-AVCC0	B14, C14		
CVCC7-CVCC0	B19, C3, B15, A18, P20, Y7, L4, G3		
MVCC6-MVCC0	C17, D18, F18, G20, J20, L19, N18		
PVCC	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15		1
SVCC8-SVCC0	D5, D7, C8, D10, A12, K2, H3, E1, D2		
AGND2-AGND0	D12, A13, B13		2
GND	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17		3

[1] These BGA ball pads are connected to the power potential ring in the package.
[2] A 10K +/- 1% ohms resistor should be connected between pins C13 and D12. D12 should not be connected to pins A13 and B13 on the board.
[3] These BGA ball pads are connected to the die pad and the ground potential ring in the package.

Spare Pins

Table 2-8. Spare Pins

Signal Name	Pin Number	Notes
N/C	Y5, Y11, Y17, Y20, A20, P18	AIC-7890A and AIC-7891
N/C	M3, M4, N3, P3, P4, R3, T3, T4, V3, V4, U5, V5, V6, U7, V7, V8, U9, V9, V10, V11, U11, V12, U12, V13, V14, U14, V15, V16, U16, V17, V18, U18, T17, T18, R18, P17, R19	AIC-7890A only

Pin Signal Description

The logical state of a signal name that does not end in a # symbol is asserted or active when high and is deasserted or inactive when low. The logical state of a signal name that ends in a # symbol is asserted or active when low and is deasserted or inactive when high.

PCI Host Interface Pins

Table 2-9. PCI Host interface Pins

Symbol	Type	Definition
ACK64# (AIC-7891 only)	in	**PCI Acknowledge 64-bit Transfer Input** is an active low signal that indicates the target is willing to transfer data using 64-bit. As a target, AIC-7891 doesn't transfer data in 64-bit; therefore, ACK64# is never driven by the AIC-7891.
AD[31:0] (AIC-7890A)	in-ts/6	**PCI Address and data** are multiplexed on the same PCI bus pin. During the first clock of a transaction, AD[31:00] contain a physical byte address of (32 bits) called low address 31:00 for Single Address Cycles (SAC). During subsequent clocks, AD[31:00] contain data of (32-bits) called low data 31:00, except for Dual Address Cycles (DAC) where both the first (low address 31:00) and second (high address 63:32) clocks of a transaction contain address and the remaining clocks contain data (low data 31:00). The turn-around PCLK period for AD[31:00] is the idle cycle between transactions. A PCI read or write bus transaction consist of one Address phase (SAC) or two Address phases (DAC) followed by one or more Data phases. Each PCI Data phase may consist of one or more PCLK periods. Little-endian byte ordering is used. AD[07:00] define the least significant byte and AD[31:24] the most significant byte. All 32 AD[31:00] bits must be driven to stable values (excluding turn around PCLK periods) during every Address and Data phase, to enable even-parity checking. All AD[31:00] bits must be decoded for memory and I/O phases to allow for future address expansion. The use of AD[01:00] varies in the Address phase of the three different PCI address spaces: ■ In the PCI Configuration address space, AD[01:00] identify the type of configuration space the access is intended for. A value of 0h identifies the configuration space as type 0; a value of 1h identifies it as type 1. Values of 2h and 3h are reserved. Type 0 configuration accesses are not propagated beyond the local PCI bus and must be claimed by a local device or terminated with master-abort. Type 1 configuration accesses are for targets that do not reside on the local PCI bus. For type 0, AD[07:02] define a 32-bit register address within the configuration address space. Thus, configuration address space defaults to Double Word (DWD) addressing aligned to the DWD boundary. Targets with multiple functions must contain a configuration space for each function. The value supplied on AD[10:08] is used to point to each space. The AIC-7890A, as a single function target supporting type 0 address space, accesses with a single configuration space. As a target, the AIC-7890A uses positive address decoding over AD[10:02], along with CBE[3:0]# (command is CRDC or CWRC), IDSEL, AD[01:00] = 0h and FRAME# to validate the configuration register address decode, then asserts DEVSEL# to claim the transaction. AD[10:08] must be "000" to enable configuration access of the AIC-7890A. IDSEL is normally connected to an ADn signal in the range of AD[31:11] of the PCI bus.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
		■ In the IO address space, all 32 AD lines are used to provide for direct byte address decoding. The AIC-7890A as a target uses positive address decoding over BASEADR0 register (stored value), AD[31:08] (for mapping), CBE[3:0]# (for command), AD[07:00] (for register address) and FRAME# to validate the Device Space register 256 decodes. When the AIC-7890A as a target is enabled to allow access to its Device Space registers from the PCI I/O address space, the use of AD[01:00] during the Address phase allows the AIC-7890A to validate the register address decode and claim the transaction (assert DEVSEL# = medium speed). TRDY# is deasserted for the first Data phase to allow the Data phase CBE value to become valid for byte steering to the internal 8-bit register path for a three PCLK data transfer cycle for register write. For register read, TRDY# is deasserted for the required AD[31:00] turn-around cycle, plus an additional PCLK for H/W registers, plus one or more to enable internal or external RAM data to become valid. Note, additional PCLKs are required for some addresses, due to mode conditions. Many AIC-7890A registers are also accessed by the internal RISC PhaseEngine (sequencer). ■ In the PCI memory address space, AD[01:00] are excluded from the address decode and as such, the address defaults to Double Word (DWD) addressing aligned to the DWD boundary. The value AD[01:00] are used in the memory address space to indicate different Memory Address Transfer modes. A value of 0h indicates linear address increment mode, 1h is reserved (disconnect after first data phase), 2h indicates Cache Line Wrap mode, and 3h is reserved. The AIC-7890A as a master or target only supports the linear address increment mode. When the AIC-7890A as a target is enabled to allow access to its Device Space registers from the PCI memory address space, it will use positive address decoding over BASEADR1 register (stored value), AD[31:02], CBE[3:0]# (command) and FRAME# to obtain the DWD access decode and claim the transaction by asserting (DEVSEL# = medium speed). Then use the CBE[3:0]# (data) value to complete the Device Space register decode. TRDY# is deasserted for the first Data phase to allow the Data phase CBE value to become valid for byte steering to the internal 8-bit register path for a three PCLK data transfer cycle for register write. For register read TRDY# is deasserted for the required AD[31:00] turn-around cycle, plus an additional PCLK for H/W registers, plus one or more to enable internal or external RAM data to become valid. Note, additional PCLKs are required for some addresses due to mode conditions. Many AIC-7890A registers are also accessed by the internal RISC PhaseEngine (sequencer) When the AIC-7890A as a target is enabled to allow access to the expansion ROM address space through the AIC-7890A memory port to a local 8-bit ROM/EEPROM, the AIC-7890A will use positive address decoding over EXROMCTL register (stored value), AD[31:02], CBE[3:0]# (command) and FRAME# to obtain the DWD access decode and claim the transaction by asserting (DEVSEL# = medium speed).

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
		For Memory Read commands, the AIC-7890A will perform a burst of four read accesses of the external ROM/EEPROM to assemble a 32-bit value for the PCI Read command, regardless of the CBE[3:0]# value for the requested data. TRDY# is deasserted for additional PCLKs for the required AD[31:00] turn-around cycle and to enable the external ROM (150 nsec per cycle) data to become valid, and will be asserted when the 32-bits are valid. For Memory Write commands, the AIC-7890A will write only the byte associated with the single asserted CBE[3:0]# to the external EEPROM. When no CBE[3:0]# are asserted, the write will be treated as an NOP. TRDY# will be deasserted for the external EEPROM write cycle access time (150 nsec) then will be asserted to terminate the PCI write access. **Note:** The ROM/EEPROM type and its connection to the AIC-7890A should be such that inadvertent writing when the type is ROM will not allow contention of the memory data bus. For both Read or Write commands, access will be extended with TRDY# deasserted until EXTARBACK# becomes active. When a PCI burst is indicated it will be disconnected after the first Data phase. The use of AD[31:00] varies in the Data phase of transactions as follows when the AIC-7890A is a bus master or a bus target: ■ Bus target Data phase transactions to the AIC-7890A's 8-bit Device Space registers will use the AD[31:00] byte indicated by a single asserted CBE# for all registers. Should more than one CBE# be asserted (indicates a non-supported data width), the AIC-7890A will indicate Target Abort. When more than one Data phase is indicated (burst operation), the AIC-7890A will indicate Disconnect and only accept the first Data phase. When no CBE bits are asserted, the AIC-7890A will not store the associated data for (write) and will supply all AD[31:00] bytes with 0h value for (read). ■ Bus target Data phase transactions to the AIC-7890A's configuration space supports up to (32-bit) data transfers on AD[31:00] with the valid data bytes indicated with the CBE[3:0]# value for (write), for (read) the AIC-7890A will always source all bytes of the addressed register. Reading reserved configuration space register bytes/bits always return zero for the value. Data written to reserved configuration space register bits or bytes is discarded No error indication is made for reading or writing to reserved registers. When more than one Data phase is indicated (burst operation), the AIC-7890A indicates Disconnect and only accepts the first Data phase. ■ The AIC-7890A as a master will always transfer leading offset data bytes, if they exist, to reach the next DWD boundary in the first Data phase of a transaction, if the byte count is sufficient. Then four bytes will be transferred at a time from DWD boundary to DWD boundary until the last Data phase, which will transfer any trailing offset bytes that may exist, to expire the byte count.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
AD[63:00] (AIC-7891 only)	in-ts/6	**PCI Address and Data** are multiplexed on the same PCI bus pin. If REQ64# was not detected at the end of the reset(32-bit bus) or ACK64# was not asserted by the intended target, during the first clock of a transaction AD[31:00] contain a physical byte address of (32-bits) called low address 31:00 for Single Address Cycles (SAC) command. During subsequent clocks, AD[31:00] contain data (32-bits) called low data 31:00, except for Dual Address Cycles (DAC) command where both the first (low address 31:00) and second (high address 63:32) clocks of a transaction contain address and the remaining clocks contain data (low data 31:00). The turn-around PCLK period for AD[31:00] is the idle cycle between transactions. A PCI read or write bus transaction consist of one Address phase (SAC) or two Address phases (DAC) followed by one or more Data phases. Each PCI Data phase may consist of one or more PCLK periods. Little-endian byte ordering is used. AD[07:00] define the least significant byte and AD[31:24] the most significant byte. All 32 AD[31:00] bits must be driven to stable values (excluding turn around PCLK periods) during every Address and Data phase, to enable even-parity checking. All AD[31:00] bits must be decoded for memory and I/O phases to allow for future address expansion. If REQ64# was detected at the end of the reset(64-bit bus) and ACK64# was asserted by the intended target, during the first clock of a Single Address Cycles (SAC) command, AD[31:00] contain a physical byte address of (32-bits) called low address 31:00. During subsequent clocks, AD[63:00] contain data (64-bits) called low data 63:00. During the first clock of a transaction of a Dual Address Cycles (DAC) command, AD[63:00] contain a physical byte address (64-bits) called address 63:00, and during second clocks of a transaction, both AD[31:00] and AD[63:32] contain upper 32-bit address. During subsequent clocks, AD[63:00] contain data (64-bits) called data 63:00 The use of AD[01:00] varies in the Address phase of the three different PCI address spaces: ■ In the PCI Configuration address space, AD[01:00] are used to identify the type of configuration space the access is intended for. AD[01:00] are a value of 0h to identify the configuration space as type 0 and a value of 1h for type 1, with values of 2h and 3h reserved. Type 0 configuration accesses are not propagated beyond the local PCI bus and must be claimed by a local device or terminated with master-abort. Type 1 configuration accesses are for targets that do not reside on the local PCI bus. For type 0, AD[07:02] define a 32-bit register address within the configuration address space. Thus, configuration address space defaults to Double Word (DWD) addressing aligned to the DWD boundary. Targets with multiple functions must contain a configuration space for each function. The value supplied on AD[10:08] is used to point to each space. The AIC-7891, as a single function target supporting type 0 address space, accesses with a single configuration space. The AIC-7891 as a target, uses positive address decoding over AD[07:02] along with CBE[3:0]# (command is CRDC or CWRC), IDSEL, AD[01:00] = 0h, AD[10:08] = 00Xb and FRAME# to validate the configuration register address decode, then asserts DEVSEL# to claim the transaction.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
		■ In the IO address space, all 32 AD lines are used to provide for direct byte address decoding. The AIC-7891 as a target uses positive address decoding over BASEADR0 register (stored value), AD[31:08] (for mapping), CBE[3:0]# (for command), AD[07:00] (for register address) and FRAME# to validate the Device Space register 256 decodes. ■ When the AIC-7891 as a target is enabled to allow access to its Device Space registers from the PCI IO address space, the use of AD[01:00] during the Address phase allows the AIC-7891 to validate the register address decode and claim the transaction (assert DEVSEL# = medium speed). TRDY# is deasserted for the first Data phase to allow the Data phase CBE value to become valid for byte steering to the internal 8-bit register path for a three PCLK data transfer cycle for register write. For register read, TRDY# is deasserted for the required AD[31:00] turn-around cycle, plus an additional PCLK for H/W registers, plus one or more to enable internal or external RAM data to become valid. **Note**: Additional PCLKs are required for some addresses, due to mode conditions. ■ In the PCI memory address space, AD[01:00] are excluded from the address decode and as such, the address defaults to Double Word (DWD) addressing aligned to the DWD boundary. The value AD[01:00] are used in the memory address space to indicate different Memory Address Transfer modes. A value of 0h indicates linear address increment mode, a value of 1h indicates Address Cache Line Toggle mode, and the values of 2h and 3h are reserved. The AIC-7891 as a master or target only supports the linear address increment mode. When the AIC-7891 as a target is enabled to allow access to its Device Space registers from the PCI memory address space, it will use positive address decoding over BASEADR1 register (stored value), AD[31:02], CBE[3:0]# (command) and FRAME# to obtain the DWD access decode and claim the transaction by asserting (DEVSEL# = medium speed). Then use the CBE[3:0]# (data) value to complete the Device Space register decode. TRDY# is deasserted for the first Data phase to allow the Data phase CBE value to become valid for byte steering to the internal 8-bit register path for a three PCLK data transfer cycle for register write. For register read TRDY# is deasserted for the required AD[31:00] turn-around cycle, plus an additional PCLK for H/W registers, plus one or more to enable internal or external RAM data to become valid. Note, additional PCLKs are required for some addresses due to mode conditions. When the AIC-7891 as a target is enabled to allow access to the expansion ROM address space through the AIC-7891 memory port to a local 8-bit ROM/EEPROM, the AIC-7891 will use positive address decoding over EXROMCTL register (stored value) in Configuration space, AD[31:02], CBE[3:0]# (command) and FRAME# to obtain the DWD access decode and claim the transaction by asserting (DEVSEL# = medium speed).

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
		For Memory Read commands, the AIC-7891 will perform a burst of four read accesses of the external ROM/EEPROM to assemble a 32-bit value for the PCI Read command, regardless of the CBE[3:0]# value for the requested data. TRDY# is deasserted for additional PCLKs for the required AD[31:00] turn-around cycle and to enable the external ROM (150 nsec per cycle) data to become valid, and will be asserted when the 32-bits are valid. For Memory Write commands, the AIC-7891 will write only the byte associated with the single asserted CBE[3:0]# to the external EEPROM. When no CBE[3:0]# are asserted, the write will be treated as an NOP. TRDY# will be deasserted for the external EEPROM write cycle access time (150 nsec) then will be asserted to terminate the PCI write access. Note: The ROM/EEPROM type and its connection to the AIC-7891 should be such that inadvertent writing when the type is ROM will not allow contention of the memory data bus. For both Read or Write commands, access will be extended with TRDY# deasserted until EXTARBACK# becomes active. When a PCI burst is indicated it will be disconnected after the first Data phase. The use of AD[63:00] varies in the Data phase of transactions as follows when the AIC-7891 is a bus master or a bus target: ■ Bus target Data phase transactions to the AIC-7891's 8-bit Device Space registers will use the AD[31:00] byte indicated by a single asserted CBE[3:0]# for all registers. Should more than one CBE[3:0]# be asserted (indicates a nonsupported data width), the AIC-7891 will indicate Target Abort. When more than one Data phase is indicated (burst operation), the AIC-7891 will indicate Disconnect and only accept the first Data phase (except for SCB double word write, where bursting is allowed, with linear burst order only). When no CBE bits are asserted, the AIC-7891 will not store the associated data for (write) and will supply all AD[31:00] bytes with 0h value for (read). ■ Bus target Data phase transactions to the AIC-7891's configuration space supports up to (32-bit) data transfers on AD[31:00] with the valid data bytes indicated with the CBE[3:0]# value for (write), for (read) the AIC-7891 will always source all bytes of the addressed register. Reading reserved configuration space register bytes/bits always return zero for the value. Data written to reserved configuration space register bits or bytes is discarded No error indication is made for reading or writing to reserved registers. When more than one Data phase is indicated (burst operation), the AIC-7891 will indicate Disconnect and only accept the first Data phase. ■ The AIC-7891 as a master will always transfer leading offset data bytes, if they exist, to reach the next DWD boundary for 32-bit bus or QWD boundary for the 64-bit bus in the first Data phase of a transaction, providing the byte count is sufficient. Then multiple of 4 or 8 bytes are transferred depending on the bus width until the last Data phase, which will transfer any trailing offset bytes that may exist, to expire the byte count.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
CBE[3:0]# (AIC-7890A)	in-ts/6	**Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the Address phase of a transaction, CBE[3:0]# contain a Bus command that defines the function to be performed during the transaction. CBE[3:0]# command encodings are viewed on the bus where a 1 indicates a high voltage and 0 is a low voltage. During the Data phase of a transaction, CBE[3:0]# define which data bytes of AD[31:00] contain valid data. CBE0# applies to AD[07:00] and CBE3# to AD[31:24]. The AIC-7890A asserts CBE[3:0]# when in master mode to indicate the location of the first byte in a 32-bit boundary space and to match the data width being transferred. CBE[3:0]# are asserted (=0) by the system board or a bus master to access the AIC-7890A as a bus slave. No more than one CBE# may be asserted at a time for transactions to the AIC-7890A's 8-bit Device registers without causing a Target Abort reply. **Note:** Data phases that do not have at least one asserted CBEn# do not transfer data, however all data bytes must be stable so that parity may be developed, and appear as NOPs on the bus.
CBE[7:0]# (AIC-7891 only)	in-ts/6	**Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the Address phase of a transaction, CBE[3:0]# contain a Bus command that defines the function to be performed during the transaction. CBE[3:0]# command encodings are viewed on the bus where a 1 indicates a high voltage and 0 is a low voltage. During an address phase of a DAC command with REQ64# asserted, the actual bus command is transferred on CBE[7:4]#; otherwise, these signals are reserved and indeterminate. During the Data phase of a transaction, CBE[3:0]# define which data bytes of AD[31:00] contain valid data. CBE0# applies to AD[07:00] and CBE3# to AD[31:24]. When both REQ64# and ACK64# are asserted, CBE[7:4] define which data bytes of AD[63:32] contain valid data. CBE4# applies to AD[39:32] and CBE7# to AD[63:56]. When in the master mode, if REQ64# was not detected at the end of the reset by the AIC-7891 or the AIC-7891 only intends to access the lower 32-bit space (AD[63:32] are zero), the AIC-7891 asserts CBE[3:0]# to indicate the location of the first byte in a 32-bit boundary space and to match the data width being transferred. If REQ64# was detected at the end of the reset by the AIC-7891 and the AIC-7891 intends to access the upper 32-bit space (AD[63:32] are not zero), the AIC-7891 asserts CBE[7:0]# to indicate the location of the first byte in a 64-bit boundary space and to match the data width being transferred. CBE[3:0]# are asserted (=0) by the system board or a bus master to access the AIC-7891 as a bus slave. No more than one CBE[3:0]# may be asserted at a time for transactions to the AIC-7891's 8-bit Device registers without causing a Target Abort reply. Note that AIC-7891 supports 32-bit only as a PCI target. **Note:** Data phases that do not have at least one asserted CBEn# do not transfer data, however all data bytes must be stable so that parity may be developed, and appear as NOPs on the bus.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
DEVSEL#	in-sts/6	**Device Select#.** When asserted, indicates the driving device has decoded its address as the selected target of the current bus transaction. DEVSEL# once asserted cannot be deasserted until FRAME# is sampled deasserted, except for the target-abort case. Also DEVSEL# must be asserted for one or more PCLKs before a target-abort condition may be signaled. The AIC-7890A/7891 as a slave asserts DEVSEL# with medium speed timing when responding as a result of a valid and supported command directed to the AIC-7890A/7891's Configuration register space, and when enabled, to the Device register space, or to the external ROM. The AIC-7890A/7891 as a master, samples DEVSEL# when initiating a transaction to a selected target to determine if the target is capable of proceeding with the current transaction. In the case when DEVSEL# is not asserted by the selected target for six PCLKs (SAC) or seven PCLKs (DAC) after FRAME# is asserted, the AIC-7890A/7891 will perform a master-abort (on PCLK seven (SAC) or eight (DAC) deassert FRAME# on the next PCLK (if still asserted) and on the next PCLK deassert IRDY#). Alternately where FRAME# was deasserted after one PCLK (indicates only one Data phase in the transaction), the AIC-7890A/7891 will perform a master-abort (on PCLK seven (SAC) or eight (DAC) deassert IRDY#). The AIC-7890A/7891 will not retry transactions that resulted in a master-abort (no response from target) and will generate an interrupt to the driver with RMA status active set in the respective configuration space register. Intervention is required for the AIC-7890A/7891 to continue with bus master transactions after a master abort is generated. The turn-around PCLK period for DEVSEL# is the Address phase of a transaction. The AIC-7890A/7891 as a master never asserts DEVSEL#.
FRAME#	in-sts/6	**Frame#.** Asserted by the current master to indicate the duration of a bus transaction. The assertion of FRAME# identifies an Address phase of a transaction. The deassertion of FRAME# identifies the final data phase of the transaction (FRAME# cannot be deasserted while IRDY# is deasserted for the final data phase). An idle cycle (PCI bus free) occurs when both FRAME# and IRDY# are deasserted. The turn-around PCLK period for FRAME# is the idle cycle between transactions. See DEVSEL# for the AIC-7890A/7891 Master-Abort conditions. The AIC-7890A/7891 as a target never asserts FRAME#. The AIC-7890A/7891 asserts FRAME# with the same PCLK that asserts an address value on AD[31:00] for SAC or DAC. When the transaction is a DAC, FRAME# remains asserted for the second PCLK Address phase and for all Data phases that follow, until the last data phase where FRAME# will be deasserted.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
GNT#	in	**Grant#**. Asserted indicates to a master that a bus transaction may be performed. This is a point-to-point signal with every master having its own GNT# signal. Only one GNT# may be asserted by the PCI System Board Central Resource Arbitrator at a time. The Arbitrator may deassert GNT# at any time (one PCLK period minimum assertion) and may also assert GNT# when the master is not asserting PREQ# (park the bus) to require the master to drive bus signals AD[31:00] (AD[63:00] for 64-bitbus), CBE[3:0]# (CBE[7:0]# for 64-bit bus) and PAR delayed by one PCLK within eight PCLK (recommended value is by two to three PCLKs) to prevent bus float conditions. In the case where GNT# is deasserted and FRAME# is asserted on the same PCLK, the bus transaction is valid and will continue. One GNT# can be deasserted coincident with another GNT# being asserted if the bus is not idle. Otherwise a one PCLK delay is required between the deassertion of one GNT# and the assertion of the next GNT#. The newly granted master may not start a transaction until an IDLE cycle (FRAME# and IRDY# deasserted) is sampled. GNT# is held in a tri-stated condition while PCIRST# is asserted. The AIC-7890A/7891 extends an asserted PCIRST# internally and thus will not recognize GNT# in any state until after the extension expires. Except for the PCIRST# condition, the AIC-7890A/7891 will drive AD[31:00] (AD[63:00] for 64-bit bus) and CBE[3:0]# (CBE[7:0]# for 64-bit bus) on the first PCLK, GNT# is sampled asserted with the PCI bus idle, then PAR one PCLK later.
IDSEL	in	**Initialization Device Select**. Used in lieu of the upper 24 ADn address signals and is valid only during configuration read and write transactions and is validated with FRAME# assertion, valid AD[10:8], and CBEn# values. IDSEL is a point-to-point signal with each agent having its own IDSEL. PCI convention is to connect a different AD[31:11] line to IDSEL input of each device on the bus.
IRDY#	in-sts/6	**Initiator Ready#**. Asserted to indicate the current master's ability to complete the current Data phase of a transaction. During a write, IRDY# indicates that the master is asserting valid data on AD[31:00] (AD[63:00] in the 64-bit transfer). During a read, it indicates the master is prepared to accept data on AD[31:00] (AD[63:00] in the 64-bit transfer). It is used in conjunction with TRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. A Data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. An idle cycle (PCI bus free) occurs when both FRAME# and IRDY# are deasserted. The turn-around PCLK period for IRDY# is the Address phase of a transaction. The AIC-7890A/7891 as a master asserts IRDY# with the same PCLK that starts a Data phase on AD[31:00] (AD[63:00] in the 64-bit transfer).

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
PAR	in-ts/6	**Parity.** The even-parity bit that protects both AD[31:00] and C/BE[3:0]# signals. PAR is generated by the agent that is sourcing the 32-bit address of the transaction and/or the data of the transaction and includes the CBE[3:0] values even if not sourcing them. The state of PAR is valid for the value on AD[31:00] and CBE[3:0] during the previous PCLK period for address and for the PCLK that transferred data, excluding PAR turn-around PCLK periods which occur in the PCLK following the turn-around PCLK period of AD[31:00]. The agent detecting parity errors will set the DPE bit in the Configuration Status register without regard for the state of PERRESPEN bit. The AIC-7890A/7891 as a target indicates SERR for address parity error detection when both PERRESPEN and SERRESPEN are active. The AIC-7890A/7891 as a target will assert PERR for data parity errors when PERRESPEN is active.
PAR64 (AIC-7891 only)	in-ts/6	**Parity.** The even-parity bit that protects both AD[63:32] and C/BE[7:4]# signals. PAR64 is generated by the agent that is sourcing the upper 32-bit PCI address of the transaction and/or the upper 32-bit data of the transaction and includes the CBE[7:4] values even if not sourcing them. The state of PAR64 is valid for the value on AD[63:32] and CBE[7:4] during the previous PCLK period for address and for the PCLK that transferred data, excluding PAR64 turn-around PCLK periods which occur in the PCLK following the turn-around PCLK period of AD[63:32]. The agent detecting parity errors will set the DPE bit in the Configuration Status register without regard for the state of PERRESPEN bit. The AIC-7891 as a target indicates SERR for address parity error detection when both PERRESPEN and SERRESPEN are active. The AIC-7891 as a target will assert PERR for data parity errors when PERRESPEN is active.
PCLK	in	**PCI Bus Clock Input.** Provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCLK, and all parameters are defined with respect to this edge. PCLK is a controlled skew, point-to-point signal to each agent and is only driven by the PCI System Board Central Resource. The PCLK signal for the AIC-7890A/7891 is a maximum rate of 33.3 MHz. When POWRDN is active, the AIC-7890A/7891 restricts the use of PCLK to only Configuration address space and the AIC-7890A/7891 Device registers which are accessible only from the PCI bus (not from the internal sequencer). PCLK signal used by other logic is maintained in the active state (=1) when POWRDN is active. Note, all internal logic is static allowing the PCLK and the CLKIN signals to be stopped externally if desired when no active SCSI commands are in process for maximum power down mode.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
PERR#	in-sts/6	**Parity Error#.** May be asserted (pulsed for one PCLK period for each detected error, provided that the Parity Error Response bit, PERRESPEN, is active in the Configuration Command register) only by the agent receiving the data. Also, a target cannot assert PERR# until it has claimed the access by asserting DEVSEL# and completing the data transfer. The turn-around PCLK for PERR# is the third PCLK period after the last address PAR and/or PAR64 period of an agent. PERR# is asserted for detected errors two PCLK periods after the data that contained the error as per the following sequence: 1 From PCLK N that transfers the data (both TRDY# and IRDY# are asserted) that data parity is to be generated for. 2 From PCLK N+1 PAR is asserted for the data asserted in PCLK N. 3 From PCLK N+2 assert PERR# when an even-parity error was indicated on the PCLK N+1 sample of data. 4 From PCLK (N+2)+1 deassert PERR# and when the last PERR# cycle wait for one more PCLK period before floating PERR#. The AIC-7890A/7891 asserts PERR# only for detected data parity errors for received data when PERRESPEN is active but always sets DPE bit active in the Configuration Status register. The DPE bit is set in the Configuration status register if the parity error was detected for either the data of command channel.
PREQ#	ts/6	**PCI Request#.** When asserted, indicates to the PCI System Board Arbitrator that a master desires use of the bus. This is a point-to-point signal with every master having its own PREQ#. Arbitration for the PCI bus is performed either when the bus is idle or in parallel with the transaction in process. When only a single Data phase is to be performed, PREQ# should be deasserted with the same PCLK that asserts FRAME#. When a transaction is terminated by a target, the master must deassert its PREQ# for a minimum of two PCLK periods (one period must include the bus idle period). This allows another agent to use the bus while the previous target (that requested the STOP) prepares to continue. **Note:** This is not required where the master deasserted FRAME# indicating the last Data phase of a transaction is in process. In this case, provided GNT# is still asserted, the master could start another transaction without deasserting PREQ#. PREQ# is asserted by the AIC-7890A/7891 to become a bus master provided that the MASTEREN bit is active in the PCI configuration Command register.
REQ64# (AIC-7891 only)	in-ts/6	**Request 64#.** It is used by AIC-7891 to determine if it is connected to a 64-bit data path when PCIRST# is asserted. During the normal operation, AIC-7891 uses this signal to indicate to the target that AIC-7891 desires to transfer data using 64 bits.
PCIRST#	in	**PCI Reset#.** When asserted forces agents to a known initialization state. PCIRST# may be asynchronous to PCLK when asserted or deasserted. Deassertion is guaranteed to be a clean, bounce-free edge. ■ All tri-state and sustained tri-state are forced to a high impedance state. ■ All o/d type signals are forced to float. ■ All agent internal registers (Device and Configuration) are forced to specified states. ■ All internal RAM data values should be considered indeterminate.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
SERR#	in-od/6	**System Error#.** May be asserted by a PCI agent that detects an address parity error (provided that PERRESPEN and SERRESPEN are active) during the Address phase of a transaction or for data parity errors on special cycles and for any other system error where the result will be a catastrophic error. The transaction master is solely responsible for reporting master or target aborts; targets do not assert SERR# when using target-abort termination. SERR# is restored only by a weak pull-up on the system board, and may take several PCLK periods to recover to a deasserted state. SERR# is asserted (pulsed for one PCLK period) for detected address errors two PCLK periods after the address that contained the error as per the following sequence: 1 From PCLK N for the address that is being asserted, for which parity is to be generated for. 2 From PCLK N+1 PAR is asserted for the address asserted in PCLK N. 3 From PCLK N+2 assert SERR# when an even-parity error was indicated on the PCLK N+1 sample of the address. 4 From PCLK (N+2)+1 deassert SERR#. The AIC-7890A/7891 as a target only asserts SERR# for all detected address parity errors when PERRESPEN and SERRESPEN are active.
STOP#	in-sts/6	**Stop.** When asserted, indicates the current target is requesting the master to stop the current Data phase of a transaction in process. STOP#, once asserted, must remain asserted until FRAME# is deasserted and data may or may not be transferred in the final Data phase of the transaction. The turn-around PCLK period for STOP# is the Address phase of a transaction. The AIC-7890A/7891, when attempting to perform a transaction to a target that responds with Target-Stop (disconnect) or Target-Retry, will retry the transaction with the next address to be transferred. When the response is Target-Abort, the AIC-7890A/7891 will not retry and will set the RTA bit in the Configuration Status register active and generate an interrupt IRQA#. See the Device CLRINT register for clearing this interrupt. **Note:** For Target-Abort this means the SCSI data segment transfer will stall and software/firmware intervention is required.) The AIC-7890A/7891 as a target asserts STOP# (disconnect with data transferred) when FRAME# is indicating burst cycles. This is not an error condition.

Table 2-9. PCI Host interface Pins (Continued)

Symbol	Type	Definition
TRDY#	in-sts/6	**Target Ready#**. Asserted to indicate the current slave's ability to complete the current Data phase of a transaction. During a read, TRDY# indicates that the slave is asserting valid data on AD[31:00] (AD[63:00] in the 64-bit transfer). During a write it indicates the slave is prepared to accept data. It is used in conjunction with IRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. Wait cycles should be minimized, when more than eight are expected, except for the first transfer, the transaction should be disconnected by the target and retried by the master. A Data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. The turn-around PCLK period for TRDY# is the Address phase of a transaction. The AIC-7890A/7891 as a target will always have TRDY# deasserted in the first PCLK period of the first Data phase so that the asserted CBE# value may be decoded for internal byte steering and for read access required AD[31:00] (AD[63:00] in the 64-bit transfer) turn-around. TRDY# will also be deasserted for additional PCLKs for RAM data to become valid, and when PAUSEACK is not active and the access is to a register that requires it to be active for the host driver to access the register (see PAUSE[ACK] bit in the Device HCNTRL register), for SCB access (when INTSCBRAMSEL is asserted), or for ROM/EEPROM access (see EXTARBREQ#/ EXTARBACK#). When TRDY# is not asserted within eight PCLKs for Data phases, the AIC-7890A/7891 will respond with Disconnect when the data transfers. Additionally, should TRDY# not be asserted within sixteen PCLKs for the first data transfer, the AIC-7890A/7891 will respond with Retry as per PCI specification 2.1 requirement. Also see EXTARBACK#.
IRQA#	od/6	**Interrupt Request**. IRQA# assertion state changes are synchronized to PCLK for PCI type errors and parity errors. The AIC-7890A/7891 interrupt conditions cannot assert IRQA# when the INTEN bit is not active or the POWRDN bit is active in the HCNTRL register. For information on IRQA# assertion conditions see *Interrupt Status (INTSTAT)* on page 4-120 and *Error Reporting and Interrupt Handling* on page 3-12. Note that IRQA# output is floated when PCIRST# is asserted.

SCSI Interface Pins

Table 2-10. SCSI Interface Pins

Symbol	Type	Definition
SCDM7-SCDM0	dual mode I/O	**SCSI Differential Minus Data [7:0]**. The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages. SCDM[7:0] are used for 8-bit data transfers. In LVD mode, these are the minus side of the differential signals.
SCDM15-SCDM8	dual mode I/O	**SCSI Differential Minus Data [15:8]**. The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages. When the narrow SCSI is used, SCDM[15:8] are floated with their inputs disabled. In LVD mode, these are the minus side of the differential signals.
SCDP7-SCDP0,	dual mode I/O	**SCSI Differential Plus Data [7:0]**. The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages. In the LVD mode, SCDP[7:0] are used for 8-bit data transfers, and are the plus side of the differential signals. In the SE mode, SCDP[7:0] are grounded internally.
SCDP15-SCDP8	dual mode I/O	**SCSI Differential Plus Data [15:8]**. The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages. In the LVD mode, SCDP[15:8] are the plus side of the differential signals. And, when the narrow SCSI is used, SCDP[15:8] are floated with their inputs disabled. In the SE mode, SCDP[15:8] are grounded internally.
SCDPHP, SCDPHM	dual mode I/O	**SCSI High Byte Parity**. This differential pair provide odd parity for SCSI data bits 15-8. In the LVD mode, SCDPHP is floated for 8-bit data transfers with its input disabled. In the SE mode, SCDPH is grounded internally.
SCDPLP, SCDPLM	dual mode I/O	**SCSI Low Byte Parity**. This differential pair provide odd parity for SCSI data bits 7-0. In the SE mode, SCDPLP is grounded internally.
CDP, CDM	dual mode I/O	**Command/Data**. This pair of differential control lines are received when in Initiator mode or driven when in Target mode. They indicate Command or Message phase when asserted, and Data phase when deasserted. These control signals are used for 8 or 16-bit transfers. In the SE mode, CDP is grounded internally.
IOP, IOM	dual mode I/O	**In/Out**. This pair of differential control lines are received when in Initiator mode or driven when in Target mode. They indicate the In direction when asserted, and the Out direction when deasserted. These control signal are used for 8 or 16-bit transfers. In the SE mode, IOP is grounded internally.
MSGP, MSGM	dual mode I/O	**Message**. This pair of differential control lines are received when in Initiator mode or driven when in Target mode. They indicate a Message phase when asserted, and a Command or Data phase when deasserted. These control signal are used for 8 or 16-bit transfers. In the SE mode, MSGP is grounded internally.

Table 2-10. SCSI Interface Pins (Continued)

Symbol	Type	Definition
REQP, REQM	dual mode I/O	**Request**. This pair of differential control lines are received by the device when in Initiator mode and driven when in Target mode. A Target will assert REQ to indicate a byte is ready or is needed by the Target. These control signals are used for 8 or 16-bit transfers. In the SE mode, REQP is grounded internally.
ACKP, ACKM	dual mode I/O	**Acknowledge.** This pair of differential control lines are received by the device when in Target mode and driven when in Initiator mode. An Initiator will assert ACK to indicate a byte is ready for or was received from the Target. These control signals are used for 8 or 16-bit transfers. In the SE mode, ACKP is grounded internally.
RESETP, RESETM	dual mode I/O	**Reset**. This pair of differential lines are received and/or driven. It is interpreted as a hard reset and will clear all commands pending on the SCSI bus. These control signals are used for 8 or 16-bit transfers. In the SE mode, RESETP is grounded internally.
SELP, SELM	dual mode I/O	**Select**. This pair of differential lines are driven after a successful arbitration to Select as an Initiator or Reselect as a Target, and otherwise it is received. These control signals are used for 8 or 16-bit transfers. In the SE mode, SELP is grounded internally.
BSYP, BSYM	dual mode I/O	**Busy.** This pair of differential lines are driven by the Initiator as a handshake during arbitration, and received for the rest of the transfer. As a Target, they are driven also as a handshake during Arbitration, and then is driven for the rest of the transfer. These control signals are used for 8 or 16-bit transfers. In the SE mode, BSYP is grounded internally.
ATNP, ATNM	dual mode I/O	**Attention.** This pair of differential lines are driven as an Initiator when a special condition occurs. They are received by the Target. These control signals are also used for 16-bit transfers. In the SE mode, ATNP is grounded internally.
DIFFSENSE	in	**Differential Sense Input**. Use DIFFSENSE line as defined in the SPI-2 specification to select the SCSI operating mode of LVD port. SPI-2 defines the meaning of different DIFFSENSE voltages as follows: DIFFSENSE < 0.5V ==> select single ended (SE) mode 0.7V < DIFFSENSE < 1.9V ==> select low voltage differential (LVD) mode 2.4V < DIFFSENSE ==> select high voltage differential (HVD) mode
LVREXT	in	**LVD External Precision Resistor**. A 10K +/- 1% ohms resistor should be connected between pins C13 and D12.
SEREXT	in	**Single-Ended External Precision Resistor**. A 11.8K +/- 1% resistor should be connected between pin A14 and the analog ground.

Table 2-10. SCSI Interface Pins (Continued)

Symbol	Type	Definition
EXPACT	in	**Expander Active.** Allows software to see the level of the AIC-7891 EXPACT input pin. The intended use is to identify, when AIC-7891 is communicating with a SCSI device, whether the SCSI device is on the other side of an AIC-3860 SCSI expander chip. If this pin is not connected to the AIC-3860, it must be pulled low or tied to ground externally.
EXTXCVR#	in-pu	**External High Voltage Differential Driver Device Present.** When asserted (=0) indicates that high voltage differential driver device(s) is present. EXTXCVR# input contains an internal pull-up and only needs to be connected for HVD operation.
LED#	ts/24	**LED#.** Output provides three functions: 1 To indicate (when asserted =0) that the AIC-7890A/7891 is actively connected to the SCSI bus. LED asserted state is latched with the ORed result of active bits SELINGO, SELDI and SELDO in the SSTAT0 register and deasserted by the following SCSI bus free condition. LED# may be used to provide system status of the AIC-7890A/7891 SCSI bus activity and may directly drive an indicator (LED) providing the current is limited to a maximum of 20 mA. 2 As a clock to (20 MHz) shift-in an external device ID value from input IDDAT, to replace the internal default Subsystem ID and/or Subvendor ID value. This use of LED# is triggered as a result of PCIRST# assertion. See IDDAT pin for details. 3 For diagnostic support or general purpose output control bit, see Device SBLKCTL register. Note the LED# output is floated when PCIRST# is asserted. After PCIRST# is deasserted the specified IDDAT clocking occurs, then LED# will be asserted continuously until cleared by software/firmware, to provide an indication that normal run mode has been entered. Should a PCI target access be attempted to the AIC-7890A/7891 while the IDDAT shift-in process is active, a RETRY response will be returned. Note the fourth IDDAT clock present on LED# internally samples the input state of RAMPS# to store the MPORTMODE state.
STPWCTL	ts/4	**SCSI Termination Power Down Control.** Provides the capability to enable or disable the external SCSI bus termination power source. The enable/disable polarity of STPWCTL may be selected with the STPWLEVEL bit in the Configuration DEVCONFIG register and the actual enable/disable state is selected with the STPWEN bit in the Device SXFRCTL1 register. CHIPRST forces STPWCTL to the selected disabled state and STPWEN to the inactive state. While PCIRST# assertion forces STPWCTL to be floated, and both STPWLEVEL and STPWEN to be inactive. STPWCTL may also be used for a general purpose output control bit.
WIDEPS#	in-pu	**Wide Present.** When asserted (=0) indicates that a wide (16-bit) cable connector is present. WIDEPS# input contains an internal pull-up and only needs to be connected for 16-bit operation. See the SBLKCTL register for more details.

FlexPort (Memory) Interface Pins

Table 2-11. FlexPort (Memory) Interface Pins

Symbol	Type	Definition
BRDOE#	ts/4-pu	**Board Control Output Enable.** This active low tri-state output controls the output enable of the tri-state drivers that drive the signals on to MD[7:3] and MDP pins. This allows the MD[7:3] and MDP to be read from BRDDAT[7:2] bits of the BRDCTL register. BRDOE# is active (=0) when BRDRW bit of BRDCTL register is asserted (=1), and SEEMS and EXTARBACK# are active. This output is floated when PCIRST# is asserted. See the definition of BRDCTL register for more details.
BRDWE	ts/4	**Board Control Write Enable.** This active high output is used to strobe the data on the MD[7:3] and MDP pin into external storage devices such as latches and flip-flops. BRDWE is active (=1) when BRDRW bit is deasserted, BRDSTB bit is asserted, and SEEMS and EXTARBACK# are active. This output is floated when PCIRST# is asserted. See the definition of BRDCTL register for more details.

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
EXTARBACK#	in-pu	**External Arbitration Acknowledge**. A status input to the AIC-7890A/7891 with an internal pull-up. When EXTARBACK# is asserted (=0) it indicates to the AIC-7890A/7891 that it may drive its memory port outputs and access externally connected devices (SEEPROM, ROM/EEPROM, SRAM, board logic devices). EXTARBACK#, once asserted, is expected to remain asserted until some other user needs access to the memory port external shared devices, which is detected by the external memory port arbitrator (a separate device). EXTARBACK# has two operational modes as follows and also used in test modes: ■ Single-user memory mode: EXTARBACK# is permanently asserted (external connection). No external arbitrator is required and no arbitration overhead is experienced in this mode. The memory port is continuously driven (PCIRST# is not asserted and CHIPRST is not written =1) unless a read cycle is to be performed. This mode of operation may be determined following PCIRST# assertion by reading the MPORTMODE value (=1) in the DEVCONFIG register. The current value of EXTARBACK# may also be determined by reading SEECTL register bit 7. ■ Multiuser mode: Requires an external arbitration controller (a separate component) and may require termination for the memory port signal lines (MD[7:0], MDP, RAMCS#, and ROMCS# lines may require pull-up termination. The SEECS line must have a pull-down termination). Each device connected to the arbitration controller requires individual point-to-point EXTARBACK# pin. The external arbitration controller and other devices (i.e. multiple AIC-7880s/AIC-7890A/7891s) must use the rising edge of the same 40 MHz clock source, as connected to the AIC-7890A/7891's CLKIN pin. This mode of operation may be determined following PCIRST# assertion by reading the MPORTMODE value (=0) in the DEVCONFIG register. The current value of EXTARBACK# may also be determined by reading SEECTL register bit 7. This indicates a multiuser configuration and the memory port is not driven by a user until a request is made with its EXTARBREQ# assertion (first user) and use granted by its EXTARBACK# assertion (first user) as a response from the arbitrator. When the external arbitrator asserts EXTARBACK# (first user) to one of the multiusers it will continue to assert it until another multiuser makes a request by asserting its EXTARBREQ# (second user). When the arbitrator samples a new additional request it will deassert its asserted EXTARBACK# (first user) and wait for the associated EXTARBREQ# (first user) to be deasserted. This indicates that the first (old) user has stopped driving the memory port. The arbitrator now asserts the EXTARBACK# associated with the second (new) user. When the new user samples its EXTARBACK# asserted it will drive the memory port and perform accesses until sampling its EXTARBACK# deasserted.

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
		This clock interlocked protocol insures the present user's current access is completed before deasserting its EXTARBREQ#, prevents memory port drive contention, and reduces the arbitration overhead for multiple accesses by the same user. Memory port access by a user is expected to be bursty (i.e. loading new SCBs). **Note:** When an EXTARBACK# is deasserted it cannot be re-asserted until the associated EXTARBREQ# is deasserted. Minimum arbitration overhead for this mode is two CLKIN periods, plus that portion of the current users cycle when a memory port cycle is in process. The cycle proceeds as follows: 1 The AIC-7890A/7891 requires an access of the memory port and asserts EXTARBREQ# with a rising edge of CLKIN. 2 The arbitrator samples EXTARBREQ# asserted and when all other EXTARBACK#s are deasserted, asserts the EXTARBACK# for the related EXTARBREQ# with a rising edge of CLKIN. 3 When the AIC-7890A/7891 samples its EXTARBACK# asserted with a rising edge of CLKIN, the AIC-7890A/7891 enables drive to its memory port outputs as required for the current access. 4 The AIC-7890A/7891 can now perform accesses to the memory port as required until sampling its EXTARBACK# deasserted with a rising edge of CLKIN. When EXTARBACK# is deasserted and a current cycle is in process, EXTARBREQ# will be deasserted with the same rising edge of CLKIN that completes the cycle. If no cycle is in process, the AIC-7890A/7891 will deassert its EXTARBREQ# and stop driving the memory port outputs with the same rising edge of CLKIN that sampled EXTARBACK# deasserted.
EXTARBREQ#	ts/4	**External Arbitration Request**. A status output that when asserted (low) indicates to an external Arbitrator that the AIC-7890A/7891requires access to the memory port external devices (SRAM(SCB) /ROM/EEPROM /SEEPROM /board logic devices). Each device (i.e. the AIC-7880s/AIC-7890A/7891s) desiring access to the shared external devices requires individual point-to-point EXTARBREQ# pin. All sequencer or host requests for memory port access will be delayed (stretched) until access is initially granted by sampling EXTARBACK# asserted. EXTARBREQ# will remain asserted until EXTARBACK# is sampled deasserted (see EXTARBACK#). EXTARBREQ# output is floated during assertion of PCIRST# or CHIPRST written (=1).

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
MA[15:0]	ts/8-pu	**Memory Address [15:0]**. The memory port address bus outputs to the externally connected devices. MA[15:0] outputs are floated during assertion of PCIRST# and become driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion, they will continue to be driven. If EXTARBACK# becomes deasserted, they will be driven until EXTARBREQ# is deasserted. MA[15:0] (along with MDP which is used as MA16) are used to directly address ROM/EEPROM devices up to 128 KBytes for access through the stored expansion ROM address range when the AIC-7890A/7891 is a target When SEEMS is active MA[15:0] are not used (see SEECTL and BRDCTL registers).
MD[7:0]	in-ts/8-pu	**Memory Data[7:0]**. The memory port data bus is used to read or write external ROM/EEPROM byte data when the AIC-7890A/7891 is the PCI target, to read or write external SRAM SCB page byte data by the sequencer or when the AIC-7890A/7891 is the PCI target, to read or write external SEEPROM bit data or board control device data by the sequencer or when the AIC-7890A/7891 is the PCI target. MD[7:0] outputs are floated during assertion of PCIRST# and become driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion, they will continue to be asserted. If EXTARBACK# becomes deasserted, they will be asserted until EXTARBREQ# is deasserted. Whenever a read cycle is to be performed the MD[7:0] outputs are floated during that cycle. For SEEPROM/board logic cycles, SEEMS is actively generating a request for arbitration. This request is synchronized to CLKIN rising edge and EXTARBREQ# is asserted. When EXTARBACK# is sampled asserted, MD[2:0] are reconfigured for access and control through the SEECTL register. Normally, MD2 is used for a SEEPROM shift clock, MD1 is used to output serial data bits to the SEEPROM, and MD0 is used to input serial data bits from the SEEPROM (a pull-up resistor on MD0 is required for this usage). See SEECTL register for control and use information. MD[7:3] are reconfigured for access and control through the BRDCTL register to access external board logic devices (pull-up resistors on MD[7:5] are required for this usage). See BRDCTL register for control and use information. **Note:** When BRDCTL/SEECTL operations are being performed bidirectional pins may be in the input state for long periods of time and might need to be terminated.

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
MDP	in-ts/ 8-pu	**Memory Data Parity**. Optionally used for parity protection of SCB data stored in the external SRAM (9-bit device). Odd-parity data will always be generated and parity checking is enabled when EXTSCBPEN is active in the Configuration DEVCONFIG register. MDP output is floated during assertion of PCIRST# and becomes driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion, they will continue to be asserted if EXTARBACK# becomes deasserted until EXTARBREQ# is deasserted. Whenever a SRAM read cycle is to be performed, the MDP output is floated during that cycle. When the external SRAM is an 8-bit device, EXTSCBPEN must be inactive and a pull-up resistor might be present to prevent float condition. **Note:** When BRDCTL/SEECTL operations are being performed, bidirectional pins may be in the input state for long periods of time and might need to be terminated. When SEEMS is active, MDP is reconfigured for access and control through the BRDCTL register to access external board logic devices. See BRDCTL register for control and use information. A pull-up resistor might be required on MDP for this usage. When ROM/EEPROM accesses are being performed, MDP is reconfigured to become MA16 and will contain the value provided by AD16.
MRW	ts/8-pu	**Memory Port Read Write**. Determines whether the memory port cycle is a read or write cycle and is driven when the AIC-7890A/7891 has been granted the arbitration for an access to the external SRAM/ROM/EEPROM memory devices. A read cycle will result when output MRW is at a high level (=1) while RAMCS# or ROMCS# is asserted. A write cycle will result when output MRW is at a low level (=0) while RAMCS# or ROMCS# is asserted. A read cycle, a write cycle, or a read-modify-write cycle may be performed by the sequencer with memory port timed control of MRW and RAMCS# in a single sequencer instruction cycle access of the memory port. The AIC-7890A/7891 as a target may only perform a read or a write cycle access through the memory port with timing following the source of the access time. MDP output is floated during assertion of PCIRST# and becomes driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion they will continue to be asserted. If EXTARBACK# becomes deasserted, they will be asserted until EXTARBREQ# is deasserted.

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
RAMCS#	ts/ 24-pu	**RAM Chip Select#.** Driven when the AIC-7890A/7891 has been granted the arbitration for an access to the external memory SRAM device and is asserted (=0) for an access to the external SRAM. RAMCS# is in a float condition and becomes driven only after EXTARBACK# is asserted due to the AIC-7890A/7891 EXRARBREQ# being asserted or when MPORTMODE is active. RAMCS# output is floated during assertion of PCIRST# and becomes driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion they will continue to be asserted. If EXTARBACK# becomes deasserted, they will be asserted until EXTARBREQ# is deasserted. RAMCS# might require an external pull-up resistor to control the external SRAM chip select when the AIC-7890A/7891 output RAMCS# is in a float condition. The SRAM cycle access time is 20 nsec.
RAMPS#	in-ts/4-pu	**RAM Present#.** Asserted (=0) to indicate an external SRAM for expanded SCB Array data storage. When RAMPS# is deasserted, the internal AIC-7890A/7891 SCB Array RAM is used for SCB storage of 16 SCBs (0-15), the SCBPTR register maximum stored value is restricted to 0Fh. The upper four bytes of SCBPTR register are ignored When RAMPS# is asserted, an external SRAM is required. The size of the SRAM is 8 KBytes for 128 SCBs and 16 KBytes for 256 SCBs. The software driver must scan to determine the actual installed SRAM size (i.e. 8 or 16 KBytes). Also, when RAMPS# is asserted, the SCBPTR register maximum stored value is FFh. RAMPS# input has an internal pull-up and only needs to be connected when an external SRAM is present. Alternately, RAMPS# may be forced low during PCIRST# assertion then placed at a high =1 level prior to the fourth IDDAT clock provided by LED# after a PCIRST# assertion. The fourth IDDAT clock internally samples the input state of RAMPS# and only when high will start sourcing a buffered PCLK which may be used by external board logic. The state of RAMPS# during PCIRST# assertion is remembered in the RAMPSM bit. The state of RAMPSM along with the INTSCBRAMSEL bit determines the SCB configuration to be internal (=0) or external (=1).

Table 2-11. FlexPort (Memory) Interface Pins (Continued)

Symbol	Type	Definition
ROMCS#	ts/8-pu	**ROM Chip Select#**. Driven when the AIC-7890A/7891 has been granted the arbitration for an access to the external ROM/EEPROM and is asserted (=0) for access of the external memory ROM/EEPROM device. ROMCS# is in a float condition and becomes driven only after EXTARBACK# is asserted due to the AIC-7890A/7891 EXTARBREQ# being asserted or when MPORTMODE is active. ROMCS# output is floated during assertion of PCIRST# and become driven only after EXTARBACK# is asserted (with RST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion, they will continue to be asserted. If EXTARBACK# becomes deasserted, they will be asserted until EXTARBREQ# is deasserted. The cycle access time is hardware controlled for a 150 nsec device. **Note:** The external ROM control interface should be such that when MRW is low (write access), then ROMCS# is asserted, that the ROM's data outputs are not also enabled, then the cycle becomes a NOP with no contention with the AIC-7890A/7891's driven MD[7:0] outputs. ROMCS# requires an external pull-up resistor to control the external ROM/EEPROM chip select when the AIC-7890A/7891 output ROMCS# is in a float condition.
SEECS	ts/4	**Serial EEPROM Chip Select**. Asserted (=1) provided SEEMS is active and the AIC-7890A/7891 has been granted the arbitration for an access to the external memory SEEPROM device. SEECS output may now be controlled by the state stored in bit SEECS in the SEECTL register. SEECS output is floated during assertion of PCIRST# and becomes driven only after EXTARBACK# is asserted (with PCIRST# deasserted and CHIPRST not written (=1)). Once they have become driven due to EXTARBACK# assertion they will continue to be asserted. If EXTARBACK# becomes deasserted, they will be asserted until EXTARBREQ# is deasserted. SEECS requires an external pull-down resistor to control the external SEEPROM chip select when the AIC-7890A/7891 output SEECS is in a float condition. See the SEECTL and BRDCTL registers for additional information.

Clock and Miscellaneous Pins

Table 2-12. Clock and Miscellaneous Pins

Symbol	Type	Definition
CLKIN	in	**Clock Input.** Standard input (AIC-7890A/7891) - 40 MHz nominal input frequency. Used internally by the SCSI, sequencer, Data FIFO, memory port and the PCI host blocks for timing.
SCLKIN	in	**SCSI Clock Input.** This clock is used by the SCSI circuit instead of the internally generated 80MHz clock when XFERRATE[6:0] of the SCSIRATE register is set to 14h, and the DISABEXT66 bit of the SCSITEST register in the alternate mode is not set. See SCSIRATE and SCSITEST registers for more details.
IDDAT	in-pu	**Identification Data.** The Identification Data input provides for shifting-in an external subsystem ID and subsystem vendor ID value to replace the internal default subsystem ID and subsystem vendor ID value, which can be read from the SUBSYSTEM_ID[1:0] and SUBVENDOR_ID[1:0] Configuration space registers, respectively. The external IDDAT data source should be initialized (loaded) with the desired identification data to be shifted-in when PCIRST# is asserted. The loaded data will be shifted-in with the rising edge of 33 IDDAT shift clocks (20 MHz rate) provided on LED# commencing (1 to 3 CLKINs periods) after sampling PCIRST# deasserted. LED# transitions after the 33 IDDAT shift clocks are ignored by the IDDAT data load logic. The first bit of the first 16 IDDAT data bits is shifted-in as the MSB (bit-3) of the least significant nibble which is referenced to bit 3 of SUBSYSTEM_ID. The 16th shifted bit is referenced to bit 12 of SUBSYSTEM_ID. The order is as follows:

Shifted-in Order	Bit Replaced
1	SUBSYSTEM_ID[03]
2	SUBSYSTEM_ID[02]
3	SUBSYSTEM_ID[01]
4	SUBSYSTEM_ID[00]
5	SUBSYSTEM_ID[07]
6	SUBSYSTEM_ID[06]
7	SUBSYSTEM_ID[05]
8	SUBSYSTEM_ID[04]
9	SUBSYSTEM_ID[11]
10	SUBSYSTEM_ID[10]
11	SUBSYSTEM_ID[09]
12	SUBSYSTEM_ID[08]
13	SUBSYSTEM_ID[15]
14	SUBSYSTEM_ID[14]
15	SUBSYSTEM_ID[13]
16	SUBSYSTEM_ID[12]

Table 2-12. Clock and Miscellaneous Pins (Continued)

Symbol	Type	Definition
		If the value of any shifted in nibble(4 bits) is 'F', the referenced 4 bit of the internal registers remain unchanged. If pins TESTMODE# and PDPUDIS# are high, SUBSYSTEM_ID[03:00] is copied to DEVICE_ID[03:00]. If pin PDPUDIS# is low, DEVICE_ID[03:00] is always defaulted to Fh. Note that DEVICE_ID[15:4] is always 001h. The 17th shifted bit is called the *Shift _Disable_of_SUBVENDOR_D.* When this bit is '1', then the following 18th up to 33th shifted bits will be totally ignored. This allows the IDDAT pin (with its internal pull-up) to be left floating (no external logic) to use the internal default value. If this bit is '0', then the 18th shifted bit will overwrite the value of bit 3 in SUBVENDOR_ID, while the last 33th shifted bit will overwrite the value of bit 12 in SUBVENDOR_ID. This makes possible to replace the SUBVENDOR_ID by any value from '0' up to 'F'. The order is as follows:

Shifted-in Order	Bit Replaced
18	SUBVENDOR_ID[03]
19	SUBVENDOR_ID[02]
20	SUBVENDOR_ID[01]
21	SUBVENDOR_ID[00]
22	SUBVENDOR_ID[07]
23	SUBVENDOR_ID[06]
24	SUBVENDOR_ID[05]
25	SUBVENDOR_ID[04]
26	SUBVENDOR_ID[11]
27	SUBVENDOR_ID[10]
28	SUBVENDOR_ID[09]
29	SUBVENDOR_ID[08]
30	SUBVENDOR_ID[15]
31	SUBVENDOR_ID[14]
32	SUBVENDOR_ID[13]
33	SUBVENDOR_ID[12]

If pins TESTMODE# and PDPUDIS# are high, SUBVENDOR_ID[15:00] is copied to VENDOR_ID[15:00]. If pin PDPUDIS# is low, SUBVENDOR_ID[15:00] is always defaulted to 9005h.

A 33-bit shift register is required for both words to be changed. Should a PCI target access be attempted to the AIC-7890A/7891 while the IDDAT shift-in process is active, a RETRY response will be returned.

EXTPAUSE#	in-pu	**External Sequencer Pause.** This active low signal is used to pause the AIC-7890A/7891's internal Sequencer. This pin is used for the system diagnostic only, and should not be used for any other purpose.

Test Pins

Table 2-13. Test Pins

Symbol	Type	Definition
TCK	in	**Test Clock for the IEEE Standard 1149.1.** This clock is used to clock state information and test data into and out of the device during operation of the TAP controller. This pin must be pulled high or low externally if is not used.
TDI	in	**Test Data Input for the IEEE Standard 1149.1.** This input signal is used to serially shift the test data and test instructions into the device during operation of the TAP controller. This pin must be pulled high or low externally if is not used.
TDO	out	**Test Data Output for the IEEE Standard 1149.1.** This output signal is used to serially shift test data and test instruction out of the device during operation of the TAP controller.
TMS	in	**Test Mode Select for the IEEE Standard 1149.1.** This input signal is used to control the state of the TAP controller in the device. This pin must be pulled high or low externally if is not used.
TRST#	in	**Test Reset for the IEEE Standard 1149.1.** This active low signal is used to provide an asynchronous initialization of the TAP controller. This pin must be pulled low externally if is not used.
TESTMODE#	in	**Test Mode.** When this signal is low, the chip is under the internal full-scan & IDDQ tests. When this signal is high, it changes the definition of PDPUDIS# to ID_Copy_En. See PDPUDIS# for more details.
PDPUDIS#	in	**Pull-Down and Pull-up Diable.** This signal works conjunction with TESTMODE# to control the mode of operation in the chips. See table below for summary:

TESTMODE#	PDPUDIS#	Mode of Operation
1	1	Normal mode, ID_Copy_En = 1
1	0	Normal mode, ID_Copy_En = 0
0	1	Internal SCAN mode
0	0	IDDQ mode

In revision 0 chips, when ID_Copy_En is active (=1), DEVICE_ID[3:0] = SUBSYSTEM_ID[3:0] & VENDOR_ID[15:0] = SUBVENDOR ID[15:0]. When ID_COPY_EN is inactive (=0), DEVICE_ID[3:0]= Fh & VENDOR_ID[15:0] = 9005h.

In other revisions of the chip, when ID_COPY_EN is active (=1), DEVICE_ID[3:0]= SUBSYSTEM_ID[3:0]. When ID_COPY_EN is inactive (=0), DEVICE_ID[3:0]= Fh.

Note: If DEVICE_ID is modified through the PCI interface by software, the ID_COPY_EN bit has no effect.

Power and Ground Pins

Table 2-14. Power and Ground Pins

Symbol	Type	Definition
AVCC1-AVCC0	pwr	Analog Power.
CVCC7-CVCC0	pwr	Core Logic Power.
PVCC14-PVCC0	pwr	PCI I/O Power.
MVCC5-MVCC0	pwr	Memory (FlexPort) I/O Power.
SVCC8-SVCC0	pwr	SCSI I/O Power.
AGND2-AGND0	gnd	Analog Ground.
GND	gnd	Ground for the core, PCI, SCSI and FlexPort circuits.

Spare Pins

Table 2-15. Spare Pins

Symbol	Type	Definition
N/C		No Connect. Those pins are spare pins and should not tie to any other signals including power and ground.

3

Functional Description

The AIC-7890A/91 architecture consists of a complete Ultra2 SCSI controller on a single chip. The Ultra2 SCSI controller has a 20-MIPS SCSI sequencer, a DMA Command Channel, a DMA Data Channel with a 512-byte Data FIFO, and an onboard 3-KByte SRAM. The Ultra2 SCSI controller can access off-chip SRAM, ROM, EEPROM, Serial EPROM, and FEPROM through the onboard FLEXPort. The Ultra2 SCSI controller accesses the PCI bus through a full-featured PCI 2.1-compliant, 32-bit bus master for the AIC-7890 and a 64-bit bus master for the AIC-7891.

The 20-MIPS SCSI sequencer provides the AIC-7890A/91 processing intelligence. The sequencer offloads I/O from the host CPU by independently handling entire SCSI data transfer operations. Figure 3-1 is a block diagram of the AIC-7890A/91 SCSI controller.

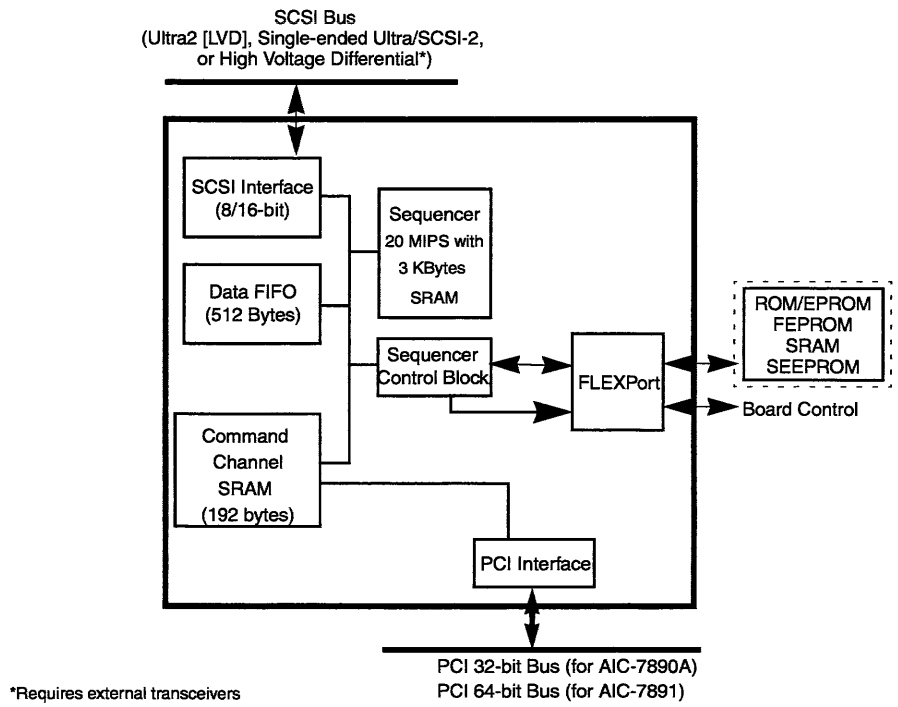


Figure 3-1. AIC-7890A/91 Block Diagram

The SCSI sequencer is programmable and uses its own self-contained microcode. The host downloads the microcode to the sequencer at initialization. In operation, the host processor initiates an I/O service by programming the AIC-7890A/91 to transfer a SCSI Command Block (SCB) from system memory to the internal RAM of the sequencer. The SCB contains all the information the sequencer needs to perform the entire SCSI operation, including a pointer to the scatter/gather (S/G) list.

The Ultra2 SCSI controller uses its DMA Data Channel to move data between system memory and its 512-byte Data FIFO. The DMA Command Channel prefetches SCSI Command Blocks (SCBs) from system memory to onboard SRAM. The DMA Command Channel performs other functions such as moving S/G list elements from system memory to the 128 bytes of onboard-SRAM. The DMA command and data channels allow the AIC-7890A/91 to exploit available PCI bus bandwidth.

The AIC-7890A/91 FLEXPort interface allows the Ultra2 SCSI controller to access off-chip memory resources. The FLEXPort interface supports PCI-mapped BIOS ROM/EPROM, serial EEPROM, SRAM, and general purpose I/O ports.

PCI Interface

The AIC-7890A connects directly to a PCI 32-bit bus as a bus master and slave without additional logic and works at the full 33.3 MHz PCI clock rate, delivering data bursts up to the 133 MBytes/sec, 32-bit-wide data burst rate.

The AIC-7891 connects to a PCI 64-bit bus as a bus master and slave without additional logic and works at the full 33.3 MHz PCI clock rate to deliver data bursts up to the 267 MBytes/sec, 64-bit-wide data burst rate.

In addition to providing on each Ultra2 SCSI channel an interface to the 512 byte Data FIFO, the command channel SRAM, and internal device control registers, the PCI interface supports a PCI mapped BIOS ROM/EPROM/FEPROM through the AIC-7890A/91 FLEXPort interface

PCI Signals

The AIC-7890A supports all required PCI-32 signals, and the AIC-7891 supports all PCI-64 signals. Figure 3-2 shows the PCI interfaces. Full parity is maintained on the entire data path through the chip. Both the AIC-7890A and AIC-7891 operate using INTA# and INTB# resources.

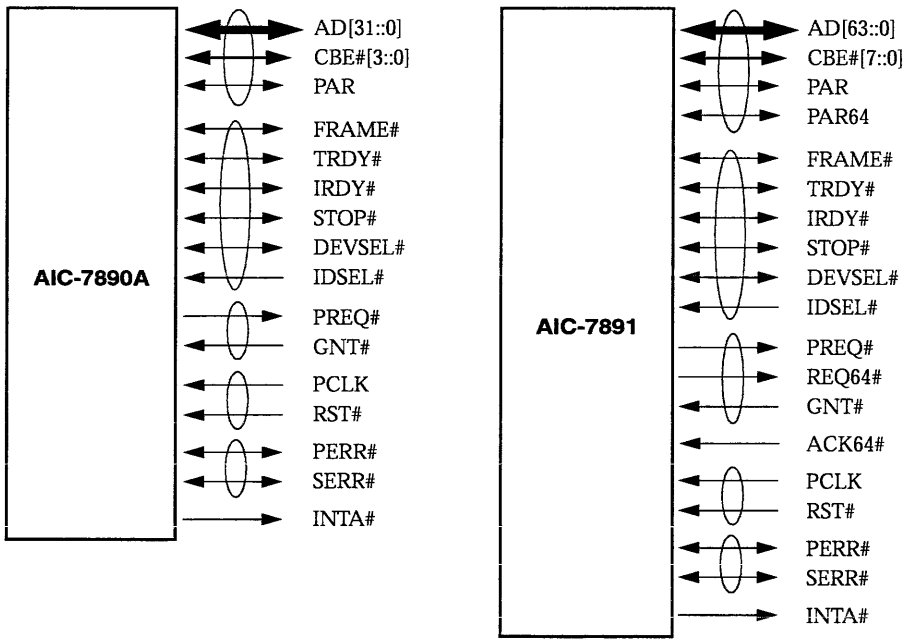


Figure 3-2. PCI Interface

PCI Protocol

Configuration

The configuration VENDOR_ID will be hard-wired registers with a value of (9005h) for Adaptec. The configuration DEVICE_ID registers have a default value of 001Fh. All chip setup will take place by the controlling BIOS or driver at initialization time.

Data Transfer

Data transfer is enabled by setting up the SCSI and Data Channel DMA engine with regard to direction, pointers and count values. The data FIFO should be cleared, and then the HDMAEN, and SCSIEN bits in DFCNTRL should be set to one. Transfers may be disabled by clearing any of these bits, but they should be polled for zero before the transfers are guaranteed to have stopped. In addition to these bits, HDONE and SDONE have been implemented to indicate the end of the transfer. DMADONE is also implemented and is the logical AND of HDONE and SDONE. DMADONE is intended to be one bit which will determine the end of transfer in either direction.

PCI Bus Commands

PCI bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on signals CBE[3:0]# during the Address phase of the transaction except that for AIC-7891 in 64-bit PCI bus, when using the DAC command and when REQ64# is asserted, the actual bus command is also transferred on CBE[7:4]#. The sense of values present on CBE[3:0]# for Bus commands during the Address phase is the same as that used on AD[31:00] (i.e., one = high level and zero = low level). This is the

reverse of when CBE[3:0]# are used for valid byte indicators (=0) during Data phases. The AIC-7890A/91 supports the following PCI Bus commands:

Interrupt Acknowledge Command (IAC) CBE[3:0]#=0000: is a Read command implicitly addressed to the system Interrupt controller. The command is defined only by the CBE[3:0]# value. The ADN value during Address phase value is not used and the CBE[3:0]# value in the Data phase determines the requested valid data width response expected on ADN.

- **The** AIC-7890A/91 **as Target:** ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

Special Cycle Command (SCC) CBE[3:0]#=0001: is a Message Broadcast command to pass status to all PCI agents on the PCI bus or for logical sideband signaling between PCI agents on the bus that recognize the passed message. The SCC contains no explicit destination address. Each agent on the PCI bus that accepts an SCC must determine whether the message is applicable to it. DEVSEL# and TRDY# are never asserted to an SCC. Command timing is controlled by FRAME# and IRDY# during the Address phase ADN are stable, with don't care value, with correct parity. During the single Data phase AD[07:00] encode 64 specified *fixed* messages, AD[23:08] are 128 reserved message values (reserved value is 00h and *must not be aliased or used*) and AD[31:24] encode 64 optional *soft* messages that are agent dependent (=00h when not used).

The current specified messages are:

AD[07:00]	Message
00h	Shutdown
01h	Halt
02h	RSVD
03h - 3Fh	RSVD

- **The** AIC-7890A/91 **as Target:** ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

IO Read Command (IORDC) CBE[3:0]#=0010: is a command to read data from an addressed Target's Device register space, which has been mapped into system IO Address space and enabled for access with ISPACEEN active.

- **The** AIC-7890A/91 **as Target:** supports IORDC only for 8-bit transfers for all registers in its Device register space. Note, Disconnect will be returned when a data burst is indicated for all registers. When more than one CBE[3:0]# is asserted, a target-abort condition will be returned. When no CBE[3:0]# signal is asserted, the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. TRDY# will not be asserted until the addressed register access and data is valid. The period before TRDY# is asserted will vary depending on the address (internal/external) and state of PAUSEACK and/or EXTARBACK#.
- **The** AIC-7890A/91 **as Master:** not generated.

IO Write Command (IOWRC) CBE[3:0]#=0011: is a command to write data to a Device register space, which has been mapped into system IO address space and enabled for access with ISPACEEN active.

- **The** AIC-7890A/91 **as Target:** supports IOWRC only for 8-bit transfers for all registers in its Device register space. Note, Disconnect will be returned when a data burst is

indicated for all registers. When more than one CBE[3:0]# is asserted, a target-abort condition will be returned. When no CBE[3:0]# signal is asserted the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. TRDY# will not be asserted until the addressed register access is valid. The period before TRDY# is asserted will vary depending on the address (internal/external) and state of PAUSEACK and/or EXTARBACK#.

- **The** AIC-7890A/91 **as Master:** not generated.

RSVD CBE[3:0]#=0100

- **The** AIC-7890A/91 **as Target:** ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

RSVD CBE[3:0]#=0101

- **The** AIC-7890A/91 **as Target:** ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

Memory Read Command (MRDC) CBE[3:0]#=0110: is a command used to read data from an addressed target mapped in the system Memory Address space with its MSPACEEN active in the Configuration Command register. MRDC is not cache line referenced and may contain any length of Data phases. MRDC may be used for transfers not starting on cache line boundaries to reach a boundary after which the MRDC command could be continued or either a MRDLC or MRDMC could be used to improve system memory performance.

- **The** AIC-7890A/91 **as Target:** supports MRDC only for 8-bit transfers for all registers in its Device register space. The AIC-7890A/91 supports 32-bit MRDC transfers only from the external ROM/EEPROM. Note, Disconnect will be returned when a data burst is indicated for all registers. When more than one CBE[3:0]# signal is asserted (except for ROM/EEPROM read where any value is acceptable), a target-abort condition will be returned. When no CBE[3:0]# signal is asserted, the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. TRDY# will not be asserted until the addressed register access and data is valid. The period before TRDY# is asserted will vary depending on the address (internal/external) and state of PAUSEACK and/or EXTARBACK#.
- **The** AIC-7890A/91 **as Master:** supports MRDC for transfers from system memory. It will be issued whenever the starting address is not on the selected cache line boundary, a byte offset condition exists, or remaining count is less than the cache line size. Also see MRDCEN.

Memory Write Command (MWRC) CBE[3:0]#=0111: is a command used to write data to a target mapped in the system Memory Address space with its MSPACEEN active in the Configuration Command register. MWRC is not cache line referenced and may contain any length of Data phases. MWRC must be used for transfers not starting on cache line boundaries to reach a boundary after which the MWRC command could be continued or a MWRIC could be used to improve system memory performance.

- **The** AIC-7890A/91 **as Target:** supports MWRC only for 8-bit transfers for all registers in its Device register and external ROM/EEPROM spaces. Disconnect will be returned when a data burst is indicated for all registers. When more than one CBE[3:0]# is asserted, a target-abort condition will be returned. When no CBE[3:0]# signal is asserted, the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. TRDY# will not be asserted until the addressed register access is valid. The period before TRDY# is asserted and will vary

depending on the address (internal/external) and state of PAUSEACK and/or EXTARBACK#.

- **The** AIC-7890A/91 **as Master:** supports MWRC for transfers to system memory. It will be issued whenever the starting address is not on the selected cache line boundary, a byte offset condition exists, remaining count is less than the cache line size.

RSVD CBE[3:0]#=1000

- **The** AIC-7890A/91 **as Target:** is ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

RSVD CBE[3:0]#=1001

- **The** AIC-7890A/91 **as Target:** ignored after checking the address parity.
- **The** AIC-7890A/91 **as Master:** not generated.

Configuration Read Command (CRDC) CBE[3:0]#=1010: is a command used to read data from a device's Configuration space or spaces mapped into the system Memory Address space by connecting one of AD[31:11] address lines to the device IDSEL input. All devices are required to support this command.

- **The** AIC-7890A/91 **as Target:** supports CRDC access for all registers in its single function Configuration register space. Note, Disconnect will be returned when a data burst is indicated for all registers. All 32-bits are always provided without regard for the CBE[3:0]# value. When no CBE[3:0]# signal is asserted, the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. For valid accesses TRDY# is asserted one PCLK following DEVSEL# assertion.
- **The** AIC-7890A/91 **as Master:** not generated.

Configuration Write Command (CWRC) CBE[3:0]#=1011: is a command used to write data to a device's Configuration space or spaces mapped into the system Memory Address space by connecting one of AD[31:11] address lines to the device IDSEL input. All devices are required to support this command.

- **The** AIC-7890A/91 **as Target:** supports CWRC for all registers in its single function Configuration register space. Note, Disconnect will be returned when a data burst is indicated for all registers. Any combination of CBE[3:0]# value assertion is acceptable for writing bytes and when none is asserted, the data cycle will be treated as a NOP. DEVSEL# is asserted using medium speed target response timing. For valid accesses TRDY# is asserted one PCLK following DEVSEL# assertion.
- **The** AIC-7890A/91 **as Master:** not generated.

Memory Read Multiple (MRDMC) CBE[3:0]#=1100: is a command used to read data from a target mapped in the system Memory Address space with its MSPACEEN active in the Configuration COMMAND register. MRDMC is cache line referenced and when used indicates that multiple cache lines are expected to be required for the transaction, but do not have to be used.

- **The** AIC-7890A/91 **as Target:** defaults to MRDC.
- **The** AIC-7890A/91 **as Master:** supports MRDMC for transfers from system memory. It will be issued whenever the starting address is on the selected cache line boundary, no byte offset condition exists, remaining count is greater than/or equal to the cache line size. Cache line streaming is supported.

Dual Address Cycle (DAC) CBE[3:0]#=1101: is a command used to transfer 32-bit data anywhere in a 32-bit address space segment of a 64-bit address space. In the 32-bit bus, the 64-bit address is indicated on AD[31:00] with two address phases of one PCLK each. The low 32 bits are transferred in the first PCLK and the high 32 bits in the second PCLK with the data on the following PCLKs. The CBE[3:0]# value supplied in the second address PCLK period identifies the type of data command the same as when only a single address cycle occurs. In the 64-bit bus, the 64-bit address is indicated on AD[63:00] during the address phase. The CBE[7:4]# value identifies the type of data command.

- **The** AIC-7890A/91 **as Target:** will respond to DAC if PCI Address matches the MBAR[63:12].
- **The** AIC-7890A/91 **as Master:** supports DAC for transfers to and from system memory. It will be issued in the first address phase whenever DACEN is active in the Configuration DEVCONFIG register and HADDR[7:4] register contents are not zero. In the second address phase, the AIC-7890A/91 will issue a MRDC, MRDLC, MRDMC, MWRC or MWRIC command followed by Data phases of the transaction. Transfers across 4-GByte boundaries are not allowed.

Memory Read Line (MRDLC) CBE[3:0]#=1110: is a command used to read data from a target mapped in the system memory address space with MSPACEEN active in the Configuration Command register. MRDLC is cache line referenced and when used indicates that a single cache line is expected to be required for the transaction, but does not have to be used.

- **The** AIC-7890A/91 **as Target:** defaults to MRDC.
- **The** AIC-7890A/91 **as Master:** supports MRDLC for transfers from system memory. It will be issued whenever the starting address is on the selected cache line boundary, no byte offset condition exists, remaining count is greater than/or equal to the cache line size, and CACHETHEN is active. Control of data transfer size to only cache line size may be obtained when the CACHSIZE, LAT_TIME registers and the GNT# assertion time have appropriate values, except for the last transfer which may be less. Also see MRDCEN. Cache line streaming is supported.

Memory Write and Invalidate (MWRIC) CBE[3:0]#=1111: is a command used to write data to a target mapped in the system Memory Address space with MSPACEEN active in the Configuration Command register. MWRIC is cache line size referenced and when used to improve system memory performance indicates that complete cache lines are to be transferred in the transaction.

- **The** AIC-7890A/91 **as Target:** defaults to MWRC.
- **The** AIC-7890A/91 **as Master:** supports MWRIC for transfers to and from system memory. It will be issued whenever the starting address is on the selected cache line boundary, no byte offset condition exists, remaining count is greater than/or equal to the cache line size and DFTHRSH is active. When CACHETHEN is active, control of data transfers to only cache line size when the CACHESIZE, LAT_TIME registers and GNT# assertion time have appropriate values. When FIFOFLUSH is active, a MWRC command will be used instead of MWRIC. Should the Target signal Disconnect in the middle of a MWRIC cache line command, the AIC-7890A/91 will terminate the MWRIC command and release the bus. The AIC-7890A/91 will then request the bus to complete the cache line using MWRC. Cache line streaming is supported.

Scatter/Gather Operation with / without Preload

A Scatter/Gather element in a Scatter/Gather list contains the memory address and size of a data segment in the system memory. The Scatter/Gather list is made up with one or more Scatter/Gather elements for a single command. In order to perform a DMA data transfer between the AIC-7890A/91 and the system memory, the Data Channel Host Address register (HADDR[7:0]) and the Data Channel Host Count register (HCNT[2:0]) need to be initialized with a Scatter/Gather element which is typically pre-fetched from the system memory and stored in the S/G RAM in the Command Channel module prior to the data transfer.

The Scatter/Gather operation without preload feature simply requires one to load the HADDR[3:0] (HADDR[7:4] are only required for the DMA transfers above 4 GBytes of host memory space) and HCNT[2:0] registers with the next Scatter/Gather element, and then set HDMAEN bit to 1 in DFCNTRL register to start the DMA assuming that there is no other Data Channel DMA in progress already. Then, the HDONE bit in DFSTATUS register can be polled to determine if the DMA is complete before the next Scatter/Gather element can be loaded. The HDONE bit is set whenever the HCNT[2:0] reaches zero. Note that before the next element can be loaded, HDMAEN bit should be cleared first.

Whereas the Scatter/Gather operation with preload feature, the procedure is similar as above. The Data Channel DMA engine can store up to three Scatter/Gather elements at a time. For the subsequent elements after the first one, when the HADDR[7:0] and HCNT[2:0] registers are loaded, PRELOADEN bit in the DFCNTRL register must be set to 1 to validate the contents in the HADDR[7:0] and HCNT[2:0] registers. Whenever the DMA for the current element is complete, the DMA for the next preloaded element is automatically started by the Data Channel DMA engine, then the DMA engine is ready to accept the next element if there is one. When the Scatter/Gather elements are exhausted for the current command, the HDONE bit in DFSTATUS register can be polled to determine if the last DMA is complete. The HDONE bit stays inactive (=0) as long as HCNT is not zero. After the first three elements are loaded, the PRELOAD_AVAIL bit should be polled and cleared if it was set before the next element can be loaded. When the last element of the Scatter/Gather list is complete, HDMAEN and HDONE bits should be cleared. A typical sequence of operations is as follows assuming the Data Channel DMA engine is not already enabled,

1. Load HADDR[3:0] (HADDR[7:4] only if is necessary) and HCNT[2:0] registers for the first element.
2. If there is at least one more element available on the S/G list, set LAST_SEG bit to 0 in the SG_CACHEPTR register.
3. Set HDMAEN and PRELOADEN bits of DFCNTRL register to 1.
4. If there is at least one more element available on the S/G list, continue to next step; otherwise, go to step 10.
5. Read PRELOAD_AVAIL bit of DFSTATUS register.
6. If PRELOAD_AVAIL = 0, go back to step 4; otherwise, continue to next step.
7. Load HADDR[3:0] (HADDR[7:4] only if is necessary) and HCNT[2:0] registers for the next element.
8. If there is no more element available on the S/G list, set LAST_SEG bit to 1 in the SG_CACHEPTR register.
9. Set PRELOADEN bit of DFCNTRL register to 1, and go back to step 4.

10 Read LAST_SEG_DONE bit of SG_CACHEPTR register.

11 If LAST_SEG_DONE = 0, go back to step 10; otherwise, continue to next step.

12 DMA is complete. Clear HDMAEN bit.

Queue Offset Registers for SCB Delivery and Done SCB Queue Management

An efficient SCB delivery and Done queue management schemes have been developed by using four registers: the Host New SCB Queue Offset register (HNSCB_QOFF), the Sequencer New SCB Queue Offset register (SNSCB_QOFF), the Sequencer Done SCB Queue Offset register (SDSCB_QOFF) and the Queue Offset Control and Status register (QOFF_CTLSTA).

The HNSCB_QOFF register and the SNSCB_QOFF register are used as a SCB delivery mechanism between the host and the Sequencer. The HNSCB_QOFF register is incremented by the system host to indicate the number of new SCB(s) have already been prepared in the system memory. The SNSCB_QOFF register is typically read by the Sequencer. A read operation of this register automatically increments the register value by 1. Therefore, after each SCB is brought into the AIC-7890A/91, a read operation is executed by the Sequencer to this register to increment the value. When there is a difference between two registers (HNSCB_QOFF and SNSCB_QOFF), the SCB_AVAIL bit in QOFF_CTLSTA register is set to 1 which indicates that there is at least one SCB available for the Sequencer to bring into the SCB array. Since, only the host system can read from or write to the HNSCB_QOFF register, the Sequencer is not required to be paused by the system host during the whole operation.

The SDSCB_QOFF register is used as part of the Done SCB Queue management for the Sequencer. This register is typically read by the Sequencer only. A read operation of this register automatically increments the register value by 1. This register is used to indicate how many Done SCBs have been sent to the host. The maximum value of this register is set by the SCB_QSIZE bits in the QOFF_CTLSTA register. When the corresponding bits in the SDSCB_QOFF register is zero in relation to the selected SCB_QSIZE[2:0] (see table for QOFF_CTLSTA register definition), SDSCB_ROLLOVER bit in the QOFF_CTLSTA register is set, and this is the indication for the Sequencer to re-initialize the base address of the Done SCB queue.

PCI Big Endian Support

The AIC-7890A/91 supports both little and big endian format for data transfers. This section only discusses the big endian mode of operation since the little endian data format is standard in PCI operations.

Big endian mode is supported for either DMA, target or both types of data transfers. Big endian data format refers to the fact that data in byte lane 3 is actually the least significant byte (LSB) in the 32-bit system and byte lane 7 in the 64-bit system while data in byte lane 0 is the most significant byte (MSB) for a 32-bit system.

DMA Big endian operation. This mode is entered by setting the DMABIGENDIAN bit. During DMA big endian operation, the first byte from a dword aligned SCSI access is steered to byte lane 3 of the PCI bus and succeeding ones are steered to byte lanes 2, 1, and 0. This implies that the AIC-7890A/91 will perform the following internally:

- Data is byte-swapped. Swapping is done with consideration of PCI data width. For 32-bit data width, DMA byte from AIC-7890A/91 byte lane 0 is steered to PCI AD byte lane 3 (AD[31:24]). For 64-bit data width, DMA data byte lane 0 is steered to PCI AD byte lane 7 (AD[63:56]).

- CBE# (byte enables) are swapped by bit during the DMA PCI data phase. For 32-bit data width, the internal CBE#[0] of AIC-7890A/91 is steered to CBE#[3] during the data phase. For 64-bit data width, the internal CBE#[0] of AIC-7890A/91 is steered to CBE#[7]. The AD and CBE# bus are not swapped during the command phases.
- All DMA accesses are big endian (including fetching SCB from system memory). In order to facilitate no or minimal changes in firmware, SCBs have to be built in the big endian format (including the address pointers).

Target Big endian operation. This mode is entered by setting the TARBIGENDIAN bit. This mode is provided as an option for big endian machines to talk to the AIC-7890A/91 (as a target) without having to worry about big endian translation. Internal data swapping is performed just as in the DMA big endian mode.

Setting for Big endian operation. The AIC-7890A/91 powers up in the little endian mode. In order for a big endian machine to set the AIC-7890A/91 for a big endian mode, two sets of two mirrored bits (total of four) are provided. These mirrored bits are in DEVSTATUS0 and DEVSTATUS1 configuration registers. In order to set for big endian mode, TARBIGENDIAN and/or DMABIGENDIAN must be set. The least confusing way would be to perform a configuration dword write (with bits 14 and 22 equal to one for TARGET big endian or with bits 15 and 23 equal to one for DMA big endian). It is preferred that the user performs a configuration dword read from configuration register 40h and maintains the setting of the other bits. A detailed code sequence is as illustrated in the following mnemonics:

```
; dword READ cycle
cfg read 40h      ; data on physical bus is 32'h 00_00_0x_80 [31:0]
                  ; since AIC-7890A/91 is still in little endian mode
                  ; the data returned depends on the configuration of
                  ; the AIC-7890A/91 chip (hence the "x" value" for bits [11:8]
                  ; byte enables all active
; dword WRITE cycle to enable both DMA & Target big endian modes
cfg write 40h, 32'h00c0cx80    ; data on physical bus MUST be 32'h 00_c0_cx_80
                    ; since AIC-7890A/91 is still in little endian mode

; Now AIC-7890A/91 is in big endian mode
; dword READ config reg 40h again
cfg read 40h      ; data on physical bus is 32'h 80_cx_c0_00 [31:0]
; byte WRITE config reg 04h byte 3 (MSB) to enable AIC-7890A/91
cfg write 04h, 8'h07    ; data on physical bus is 32'h xx_xx_xx_07
                        ; byte enables on physical bus are 4'b 1110
```

PCI Power Management

Table 3-1 and Table 3-2 are the PCI Power State Transition tables.

Table 3-1. Effects of D0 to D3hot Transition

Register/Pad Signal	Register Address	Affected Bits	Event	Value
PCI Command0 Register	N04h - byte 0	00	Masked	0
		01	Masked	0
		02	Masked	0
IRQA# AIC-7890A/91 Output			Masked	1[1]

[1] Requires pullup

Table 3-2. Effects of D3hot to D0 Transition

Register/Pad Signal	Register Address	Affected Bits	Event	Value
PCI Command0 Register	N04h - byte 0	all	Reset	Reset condition
PCI Command1 Register	N04h - byte 1	all	Reset	Reset condition
PCI Status0 Register	N04h - byte 2	all	Reset	Reset condition
PCI Status1 Register	N04h - byte 3	all	Reset	Reset condition
Cachesize Register	N0Ch - byte 0	all	Reset	Reset condition
LatTime Register	N0Ch - byte 1	all	Reset	Reset condition
HdrType Register	N0Ch - byte 2	all	Reset	Reset condition
BaseAdr0 Register	N10h	all	Reset	Reset condition
BaseAdr1 Register	N14h	all	Reset	Reset condition
ExROMCtl Register	N30h	all	Reset	Reset condition
IntLinSel Register	N3Ch - byte 0	all	Reset	Reset condition
IntPinSel Register	N3Ch - byte 1	all	Reset	Reset condition
MinGnt Register	N3Ch - byte 2	all	Reset	Reset condition
MaxLat Register	N3Ch - byte 3	all	Reset	Reset condition
DevConfig Register	N40h - byte 0	all	Reset	Reset condition
DevStatus Register	N40h - byte 1	all	Reset	Reset condition
PCIErrGen Register	N40h - byte 3	all	Reset	Reset condition
HCNTL	M/DS - 87	bit 0	Set	1

Notes:

- Transition from D0 to D3hot is immediate. PCI Command register bits 0, 1, and 2 are masked internally. IRQA# output is also masked.
- Upon transition from D3hot to D0, a selective reset is asserted for 15 PCI clocks. This resets the PCI configuration registers, with the exception of the System Device ID, System Vendor ID, Subsystem Device ID, Subsystem Vendor ID, CardBus CIS pointer, and Test Control. The CHIPRST bit (bit 0) in the Host Control register is reset. PCI command register bits 0, 1, and 2 are unmasked internally. IRQA# is also unmasked.

Error Reporting and Interrupt Handling

Interrupts fall into four basic classes: normal operation, driver intervention, error, and diagnostic. Interrupt status is given in INTSTAT. The sequencer does not have to be paused to read INTSTAT. The CMDCMPLT bit is set by the sequencer to indicate that a command has been completed. The sequencer will still be running and executing any other commands that have been loaded. Sequencer interrupts are interrupts that require the driver to intervene in the normal operation in order to provide a lengthy or difficult calculation. Sequencer interrupts are caused by the sequencer setting the SEQINT bit in INTSTAT along with the INTCODE. Setting the SEQINT bit will cause the sequencer to self-pause. The sequencer may be restarted by clearing the SEQINT bit and writing a zero to the PAUSE bit in HCNTRL. The sequencer code will be structured to continue after the driver is finished handling the particular situation. A SCSI interrupt is caused by some catastrophic event such as a SCSI Reset, SCSI Parity Error, Unexpected Bus Free, or Selection Timeout. This interrupt is generated by hardware according to any SCSI event that is enabled in the SIMODE0 or SIMODE1. The sequencer is also paused by this interrupt. The BRKADRINT interrupt is used with special diagnostic code for the purpose of device debug, or for the detection of a hardware failure. The sequencer is paused by this interrupt.

SCSI Interrupts

SCSI interrupts occur when the appropriate bit in SIMODE0 or SIMODE1 is set and the corresponding condition comes true. This will set the system interrupt pin if INTEN (bit 1, HCNTRL) is set and also the SCSIINT bit in INTSTAT. If the sequencer is executing a SCSI command, these conditions are error conditions and will pause the sequencer. If the driver is executing the SCSI command, this is the normal way to respond to a SCSI interrupt. See SCSI interface section for more details.

Command Complete Interrupts

A Command Complete interrupt happens when the sequencer writes to the INTSTAT register with that bit set. It signifies that a command is finished and the completed pointer has been returned.

Breakpoint Interrupts

The sequencer has a diagnostic feature which allows a driver to stop the sequencer at a predetermined address. The address is loaded in BRKADDR0 and BRKADDR1 with BRKDIS (bit 7, BRKADDR1) cleared. When the program counter of the sequencer equals the value loaded in BRKADDR then the sequencer will be paused. BRKADRINT (bit 3, INTSTAT) will be set at this time. If BRKADRINTEN (bit 3, SEQCTL) is set, the IRQA# pin will also be driven active. BRKADRINT and the interrupt may be cleared by setting CLRBRKADRINT (bit 3, CLRINT).

Software Interrupt

The interrupt line IRQA# may be set by the software driver or Sequencer by setting SWINT (bit 4, HCNTRL). IRQA# will remain active until SWINT is cleared. INTEN will override SWINT, and must be set in order to see the IRQA#. Table 3-3 is a software interrupt summary.

Interrupt Summary

Table 3-3. Interrupt Summary

Description	Enable Conditions	Pause	INSTAT bit	ERROR bit
Sequencer Parity Error	FAILDIS=0, PERRORDIS=0 and parity error detected during opcode read	Yes	BRKADRINT	SQPARERR
CIOBUS Parity Error	FAILDIS=0, PERRORDIS=0 and CIOPARERR detected	Yes	BRKADRINT	CIOPARERR
Memory Parity Error	FAILDIS=0, MPARCKEN = 1 and MPARERR detected	Yes	BRKADRINT	MPARERR
Data Parity Error	FAILDIS=0, DPARCKEN = 1 and DPARERR detected	Yes	BRKADRINT	DPARERR
Opcode Error	FAILDIS=0 and ILLOPCODE detected	Yes	BRKADRINT	ILLOPCODE
PCI Status Error Detected	FAILDIS=0 and PCI status error detected	Yes	NONE	PCIERRSTAT
Sequencer Break Address Accessed	BRKDIS=0 and BRKADRINTEN=1 and BRKADDR compares with sequencer address	Yes	BRKADRINT	NONE
SCSI Event	Set in SIMODE0 and SIMODE1	Yes	SCSIINT	NONE
Sequencer Event	Always enabled	Yes	SEQINT	NONE
Command Complete	Always enabled	No	CMDCMPLT	NONE
Software	Always enabled	No	NONE	NONE

SCSI Interface

Manual Mode Data Transfer

In Manual PIO mode, the SCSI block is used essentially as a bus buffer having no control functions. The host transfers data directly to and from the SCSI bus via the SCSI data latch registers SCSIDATL and SCSIDATH, and processes the SCSI control signals via the SCSI signal registers SCSISIGI and SCSISIGO. This mode only supports asynchronous transfers and is usually used during the Message and Status phases. Care should be taken to ensure that data is stable while ACK or REQ is asserted.

Automatic Mode Data Transfer

Automatic PIO data transfers are enabled by setting SPIOEN (bit 3, SXFRCTL0). In Automatic PIO mode, the sequencer transfers data directly to and from the SCSI bus via the SCSI data latch registers SCSIDATL and SCSIDATH, while the hardware performs SCSI REQ/ACK handshake automatically. Transfer complete are signaled by an interrupt or by polling the status bit SPIORDY. This mode only supports asynchronous transfers and is usually used during the Message and Status phases. SCSI data may be read directly using SCSIBUSL and SCSIBUSH. The following Initiator and Target discussions assume an 8-bit transfer.

In Initiator mode, Command, Data Out or Message Out phase, SPIORDY (bit 1, SSTAT0) will be set if REQ is asserted. The sequencer or host system may write data to SCSIDATL. The

write to SCSIDATL clears SPIORDY, presents data to the SCSI bus, and causes ACK to be asserted. ACK will remain asserted until the target releases REQ, at which time the logic will release ACK completing the data transfer.

When the chip is in initiator mode and the bus is in Data In Message In, or Status phase and REQ is active, SPIORDY (bit 1, SSTAT0) will be set indicating that valid data has been latched in the SCSIDATL register. When SCSIDATL is read, ACK is driven active on the SCSI bus and SPIORDY is cleared. PIO logic will release the ACK, completing the transfer, when the REQ signal is sensed false.

When the chip is in target mode it is controlling the SCSI data phase, software must set the desired phase in the SCSISIGO register before enabling automatic PIO transfers.

In Target mode, when SCSI I/O indicates an out transfer (initiator to host) setting SPIOEN (bit 3, SXFRCTL0) WILL CAUSE the PIO logic to immediately assert REQ. SPIORDY (bit 1, SSTAT0) will be set when the initiator responds to the REQ by driving Data and ACK, software may read SCSIDATL. If this data is the last byte in the current phase then the software *must* clear SPIOEN before reading the SCSIDATL register. Reading SCSIDATL will clear the SPIORDY bit and cause the PIO logic to release REQ. If SPIOEN is still set the logic will initiate a second transfer by asserting REQ as soon as the initiator completed the current transfer by releasing ACK.

When, in target mode, the SCSI I/O signal indicates a transfer In (target to host), setting SPIOEN will immediately set the SPIORDY status bit. Software may write data the SCSIDATL register. The data write clears the SPIORDY bit and causes the PIO logic to initiate the transfer handshake by asserting REQ. SPIORDY will be set for the next byte when the initiator completed the current transfer by releasing ACK.

Automatic PIO mode may be used with 16-bit SCSI data transfers, if asynchronous timing is used. In this case, SCSIDATH should be written to or read from first, since the SCSI handshake signals will be triggered with an access to SCSIDATL.

Normal (DMA) Mode Data Transfer

In Normal (DMA) mode, the hardware performs the SCSI transfers and bus control automatically. Data is transferred automatically between the SCSI bus and the data FIFO. This transfer can be monitored via interrupts or by polling status bits. Wide, DMA transfers which are of the odd length and/or odd boundary type are handled automatically. Normal mode supports asynchronous transfers for Command and Data phase, and synchronous transfers which may be Wide and which are used during Data phase only. A DMA data transfer is enabled by setting up the SCSI and host sections with regard to direction, pointers and count values, then setting the appropriate enable bits in DFCNTRL. The data transfer rate for the Data phase is set up in the SCSIRATE register. This register chooses asynchronous or synchronous transfers, and may be set up beforehand. It has no effect on the Command phase.

Differential/Single Ended Support

External transceivers are required for HVD. However, it is important to note that HVD operation is totally different from any existing Adaptec products. If external HVD transceivers are present on the PC board then the EXTXCRV# pin must be tied to ground; otherwise, EXTXCVR# can be ignored. EXTXCRV# has an internal pull-up that can prevent the pin from floating.

The voltage on the SCSI bus DIFFSENS line indicates the type of interface connected to the chip. This signal is now used as an analog D.C. input to a three output comparator. The comparator thresholds are set as follows:

Input V	Output
<= 0.6	SE (single ended)
0.7 to 1.9	LVD (low voltage differential)
>= 2.2	HVD (high voltage differential)

SCSI Interrupts

The SCSI interrupt logic provides for the masking, generation, and clearing of all interrupts. This logic includes the interrupt mask (SIMODE), interrupt clear(CLRSINT) and interrupt status (SSTAT) registers. A SCSI interrupt is caused by some significant event occurring such as Selection/Reselection Successful, SCSI Reset, Transfer Done, Unexpected Bus Free, or Selection Timeout. SCSIINT is generated only when an interrupt condition occurs and the bit associated with the condition is set in the mask register SIMODE0 or SIMODE1. When an interrupt is generated, the status registers SSTAT0 and SSTAT1 will contain the cause of the interrupt. SCSIINT is cleared by writing to the associated bit in the appropriate clear register CLRSINT0 or CLRSINT1, or by the condition that caused the interrupt going away. Upon receiving an interrupt, the host may want to examine all bits in the status registers since the occurrence of another interrupt causing event before the host services the original interrupt will cause another bit to be set in the status register but will not cause another SCSIINT.

There are two new interrupts that operate differently from the interrupts described above, the new interrupts are SCAMSELD and IOERR. The SCAMSELD interrupt occurs if a SCAM select completion is detected by the semi-automatic SCAM logic and software may begin information transfers. See the SCAM Operations section for a more complete description of this interrupt. The IOERR interrupt will occur if the DIFFSENS input changes after initial power-on-reset, this will cause AIC-7890A/91 to change the operating mode of the SCSI drivers.

Table 3-4. SCSI Interrupts

Interrupt	Mask	Clear	Interrupt Function
SELDO SSTAT0 - 6	ENSELDO SIMODE0 - 6	CLRSELDO CLRSINT0 - 6 or Bus Free	Occurs when a Selection Out or Reselection out is completed and the target device has asserted BSY.
SELDI SSTAT0 - 5	ENSELDI SIMODE0 - 5	CLRSELDI CLRSINT0 - 5 or Bus Free	Occurs when a valid Selection In or Reselection In is completed and the target device has asserted BSY.
SELINGO SSTAT0 - 4	ENSELINGO SIMODE0 - 4	CLRSELINGOCLR SINT0 - 4 or SELDO	Occurs when the chip has won arbitration and begins a (re)selection out phase. If SELDO comes true this interrupt is cleared. This interrupt is used if the software is Select Timeout counter.
IOERR SSTAT0 - 3	ENIOERR SIMODE0 - 3	CLRIOERR CLRSINT0 - 3 or SCSIRST	This interrupt is asserted if SCSI I/O logic senses an electrical change on the SCSI bus and disables or changes the SCSI driver controls. SCSI I/O logic changes the SCSI I/O mode if the outputs of the DIFFSENS comparator change from their initial values and are stable for at least 100 msec. If diffsense compare outputs are unstable for 100 msec all the SCSI outputs are disabled. The logic re-enables the cells in the new mode once diffsense is stable for 100 msec. This occurs if a device is removed or installed on the bus, termination is changed, or the cable is damaged.
SDONE SSTAT0 - 2	ENSDONE SIMODE0 - 2	Disable SCSI Xfers or STCNT <> 0	Occurs when the STCOUNT = 0, and SCSI data transfers are enabled. In target mode this event is used to stop SCSI data transfers at transfer completion. Also in target mode SCSI transfer must be disabled before this interrupt status bit is cleared or undesired ACKs will be generated.
SPIORDY SSTAT0 - 1	ENSPIORDY SIMODE0 - 1	CLRSPIORDY SIMODE0 - 1	Interrupt occurs when SCSI automatic mode data transfer are enabled and the software may transfer to/from the SCSIDAT register. During read mode (data from SCSI) it occurs when data is available to be read, during write mode it occurs when data in the SCSDAT has been transferred and the software may write to SCSDAT again.
DMADONE SSTAT0 - 0	ENDMADONE SIMODE0 - 0	SDONE bit clear or HDONE bit clear	This interrupt occurs when both SDONE and HDONE are true indicating that the current transfer is completed and no data remains in the chips internal FIFOs.
SELTIMO SSTAT1 - 7	ENSELTIMO SIMODE1 - 7	CLRSELTIMO CLRSINT1 - 7	Occurs if the Select time-out counter is enabled and the period expires. The logic will have performed a "soft" select abort as defined in the SCSI specification. SCSI reset is NOT asserted.
ATNTARG SSTAT1 - 6	ENATNTARG SIMODE1 - 6	CLRATNTARG CLRSINT1 - 6 or ATN false	Occurs in target mode only, is asserted if the chip is logically connected to the bus and the initiator asserts the SCSI ATN signal.

Table 3-4. SCSI Interrupts (Continued)

Interrupt	Mask	Clear	Interrupt Function
SCSIRST SSTAT1 - 5	ENSCSIRST SIMODE1 - 5	CLRSCSIRST CLRSINT1 - 5	This interrupt occurs if the SCSI RST input is asserted, the chip does not need to be logically connect to the SCSI bus. The SCSI reset input must be continuously valid for at least 2 micro seconds before this status bit and interrupt are asserted. The interrupt will NOT occur if software caused the reset by setting the SCSRSTO bit in the SCSISEQ register. This interrupt should not be masked off.
PHASEMIS SSTAT1 - 4	ENPHASEMIS SIMODE1 - 4	Write SCSISIGO to get phase match or REQINIT status cleared	Occurs if at the leading edge of REQ in if current SCSI bus phase does not match the upper three bits in the SCSISIGO register (SCSI phase mismatch condition). The interrupt is further qualified by the REQINIT status bit which must be set to enable the interrupt. The interrupt will only occur in Initiator mode.
BUSFREE SSTAT1 - 3	ENBUSFREE SIMODE1 - 3	CLRBUSFREE CLRSINT - 3	This interrupt will occur if SEL and BSY are both continuously false for more than 400 nsec.Remains true until cleared by CLRSBUSFREE.
SCSIPERR SSTAT1 - 2	ENSCSIPERR SIMODE1 - 2	CLRSCSIPERR CLRSINT1 - 2	Occurs if SCSI data parity is incorrect at the leading edge of REQ in Initiator mode or ACK in target mode. See SCSIPERR bit explanation in the SSTAT1 register for a more complete description.
PHASECHG SSTAT1 - 1	ENPHASECHG SIMODE1 - 1	CLRPHASECHG CLRSINT1 - 1	Interrupt occurs if the current SCSI bus phase does not match the upper three bits of the SCSISIGO register. there are no other qualifiers for this interrupt.
REQINIT SSTAT1 - 0	ENREQINIT SIMODE1 - 0	CLRREQINIT CLRSINT1 - 0	This interrupt occurs only in initiator mode. During asynchronous transfers interrupt is set by the leading edge of REQ and cleared by the following ACK. during synchronous transfers the interrupt is asserted if the SCSI offset is greater than 0, offset = 0 clears the interrupt. In general this interrupt means there are one or more unanswered REQs.
SCAMSELD SCAMCTL - 6	ENSCAMSELD SIMODE0 - 7	CLRSCAMSELD SCAMCTL - 6	This interrupt will occur only if semi-automatic SCAM support is enabled by setting SCAMCTL bits 0 and 1 to a non-zero value. The interrupt is asserted when the logic has detected a valid SCAM selection, the protocol has been initiated, and the software may begin SCAM information transfers. If SCAM level 1 is enabled then the SCSI module itself will have initiated the SCAM operation, if SCAM level 2 then any SCAM device on the bus may have initiated the SCAM.

SCSI Reset

The SCSI bus may be reset by setting SCSIRSTO (bit 0, SCSISEQ), waiting a Reset Hold Time (25 usec. minimum) and then clearing SCSIRSTO. SCSIRSTI (bit 5, SSTAT1) will be set only when the reset originates from the SCSI bus, if the reset originated from SCSIRSTO only, then SCSIRSTI will not be set.

SCAM Support

Two SCAM support methods are provided in the SCSI module, the direct software method and the semi-automatic method.

Direct software SCAM support is totally software controlled and is limited to SCAM level 1 only. This method is enabled by setting the SCAMEN bit in SXFRCTL0. Software may then drive or read the SCSI bus control bits through the SCSISIG register and the SCSI data bus through the SCSIBUS register. A timer is provided in bit 7, CLKOUT, of the TARGIDIN (previously called SELTIME), this signal is a 102.4 microsecond period square-wave.

Semi-automatic support for SCAM levels 1 and 2 are provided through the SCAMCTL and SCAMSTAT registers. The feature provides automatic arbitration and SCAM selection, soft I.D.s for initiators and SCAM select detection. See the SCAMCTL section for the operation of individual bits in these registers. In general software sets SCAMCTL as follows: the desired SCAM level is in the lower two bits. DLFTID is set if there is no defined ID, and ALTSTIM is set if the alternate select timeouts are to be used. When the software wishes to initiate the SCAM protocol it would set the ENSCAMSELO bit. The value set for select timeout determines SCAM select response time. Software then waits for the SCAMSELD bit to come true or the SCAMSELD interrupt to occur. Software may then begin SCAM information transfers.

SCSI Performance Monitor Register Set

The performance register set is special function register group used by host software to measure the efficiency of the I/O system. These registers are in the alternate mode register address space. The alternate mode can be entered by setting bit 7 of SFUNCT register to 1. In SCSI module these registers are used to measure the SCSI Bus Free / Not Free ratio (SCSI bus utilization). The PFREG_ENABLE signal enables register counters and should be negated before attempting the read the registers.

The bus utilization registers consists of two counters of 32 bits each. One counter increments when the bus is free; the other increments when the bus is not free. The SCSI bus is sampled and one of the counters incremented every 100 nsec. The registers are cleared by master reset only.

Writing to the Scatter/Gather SRAM via Command Channel DMA Operation

Scatter/Gather elements can be DMAed from Host Memory into S/G RAM in the Command Channel. CCHADDR[7:0], and CCHCNT must be first initialized by the Sequencer with system memory address and byte count to be transferred before DMA write transfers between host memory and this SRAM can take place. The DMA channel can then be enabled by writing a 9h value to register CCSGCTL (CCSGRESET= 1, and CCSGEN =1). For details regarding bit information, refer to CCSGCTL register description.

The procedure is as follows:

- The number of bytes to transfer is loaded into CCHCNT.
- The starting address in host memory is loaded into CCHADDR[7:0].
- The DMA transfer can then be started by writing 9h to CCSGCTL (CCSGEN=1 and CCSGRESET=1)
- Data from host memory are transferred via DMA to the Scatter/Gather SRAM. When bit 7 (CCSGDONE) in CCSGCTL is set, the transfer is complete.

Note: S/G RAM can only be written through the DMA operation as described above, and can only be read through the register port, CCSGRAM (E9h) from the Sequencer or the PCI Host.

Writing to the SCB Array via Command Channel DMA Operation

SCBs can be DMAed from Host Memory into internally or externally SCB array through the Command Channel SCB SRAM. The DMA operation can be complete with two steps. The procedure is as follows:

- The starting address in host memory is loaded into CCHADDR[7:0].
- The number of bytes to transfer is loaded into CCHCNT.
- The DMA transfer is started by writing Dh to CCSCBCTL (CCSCBRESET=1, CCSCBDIR=1, and CCSCBEN=1)
- Data from host memory is DMAed to the Command Channel SCB SRAM.
- To transfer from the command channel SCB SRAM to the SCB Array, the page address for the SCB is loaded into CCSCBPTR and the number of bytes to transfer is loaded into CCSCBCNT.
- If the SCB Array is external to the chip, the base address of the SCBs allowing relocation of 256 SCBs (16 KBytes) in one of two 16-KByte pages is loaded into SCBBADDR.
- The transfer is started by writing 15h to CCSCBCTL (CCSCBRESET=1, CCSCBDIR=1, and CCARREN=1).
- Data from SCB SRAM is transferred to the SCB array.

The DMA operation can be complete with one step. The procedure is as follows:

- The starting address in host memory is loaded into CCHADDR[7:0].
- The number of bytes to transfer is loaded into CCHCNT.
- CCSCBCNT, CCSCBPTR, and SCBADDR are loaded with their respective values.
- The transfer is started by writing 1Dh to CCSCBCTL (CCSCBRESET=1, CCSCBDIR=1, CCSCBEN=1, and CCARREN=1).
- Data from host memory is DMAed to the SCB SRAM, then to the SCB array.

Reading from the SCB Array via Command Channel DMA Operation

SCBs can be DMAed from internal or external SCB array into Host Memory through the Command Channel SCB SRAM. The DMA operation can be complete with two steps. The procedure is as follows:

- To transfer from SCB Array to the Command Channel SCB SRAM, the page address for the SCB is loaded into CCSCBPTR and the number of bytes to transfer is loaded into CCSCBCNT.
- If the SCB Array is external to the chip, the base address of the SCBs allowing relocation of 256 SCBs (16 KBytes) in one of two 16-KByte pages is loaded into SCBBADDR.
- The transfer is started by writing 11h to CCSCBCTL (CCSCBRESET=1, and CCARREN=1).
- To transfer from the Command Channel SCB SRAM to host memory, the starting address in host memory is loaded into CCHADDR[7:0].
- The number of bytes to transfer is loaded into CCHCNT.
- The DMA transfer is started by writing 09h to CCSCBCTL (CCSCBRESET=1, and CCSCBEN=1)
- Data from Command Channel SCB RAM is transferred to the host memory.

The DMA operation can be complete with one step. The procedure is as follows:

- The starting address in host memory is loaded into CCHADDR[7:0].
- The number of bytes to transfer is loaded into CCHCNT. CCSCBCNT is automatically loaded with CCHCNT value as long as CARREN is not set.
- CCSCBPTR, and SCBADDR are loaded with their respective values.
- The transfer is started by writing 19h to CCSCBCTL (CCSCBRESET=1, CCSCBEN=1, and CCARREN=1).

FLEXPort Interface

The AIC-7890A/91 has an external FLEXPort interface, which optionally may be used to extend its internal capabilities and control external functionality. In addition, the AIC-7890A/91 may share these external resources with other AIC-7890A/91 chips or with devices that are compatible with the AIC-7890A/91's FLEXPort protocol. When the FLEXPort is shared with other devices, an external Arbitration unit is required.

The external SRAM may be either an 8-bit or 9-bit device. When an 8-bit device is used, the EXTSCBPEN bit must be inactive to prevent false parity errors from being reported. A 9-bit device is used when SRAM parity operation is desired. Notice that in this case, the EXTSCBPEN bit must be active to allow checking of SRAM parity. SRAM parity will always be passed through on writes even if not used. The maximum SRAM size for direct addressability is 16 KBytes. The size of the SRAM present will be determined by the controlling driver software. SRAM paging may be performed by use of the BRDCTL register function and external board logic.

External BIOS ROM or Flash EEPROM of up to 128 KBytes is supported. To access memory this size, the 16 memory address bits of the FLEXPort are supplemented by multiplexing the 17th address bit onto the parity bit, since the ROM does not implement parity storage.

When the host writes to Flash memory, it performs a write-only cycle with extended timing for a 150 ns access device. MRW will be driven low due to CBE[3:0]# decoded as a PCI Write command with EXROMEN active, then RAMCS# will be asserted (low pulse, with the data stored on the rising edge), after which PCI TRDY# will be asserted by AIC-7890A/91 to end the cycle.

When the host reads from the external ROM, MRW will be driven high due to CBE[3:0]# decoded as a PCI Read command with EXROMEN active, then ROMCS# will be asserted with the read data stored internally on each rising edge. The AIC-7890A/91 assembles groups of four bytes into 32-bit dwords or groups of 8 bytes into 64-bit qwords, depending on the size of the PCI read, after which the AIC-7890A/91 asserts PCI TRDY# to end the cycle.

When the host or sequencer accesses SEEPROM or board logic devices, the timing of MD[7:0] and MDP are controlled by the states of the bits in SEECTL and BRDCTL registers while SEEMS is active and EXTARBACK# is asserted.

The external FLEXPort consists of the following signal lines:

Table 3-5. FLEXPort Interface

16	Address Out (MA[15:0])
8	Bidirectional Data (8-bit data) (MD[7:0])
1	Bidirectional Memory Data Parity (MDP/MA16)
1	Arbitration Request Output (EXTARBREQ#)
1	Arbitration Acknowledge Input (EXTARBACK#)
1	RAM Chip Select Output (RAMCS#)
1	ROM Chip Select Output (ROMCS#)
1	Read/Write Output (MRW)
1	Serial EEPROM/Board Logic Select Output (SEECS)
1	External SRAM Present Input/Buffered PCLK Output (RAMPS#)
1	Board Control Write Enable (BRDWE)
1	Board Control Read Enable (BRDOE#)

The FLEXPort has several modes of operation, as described below.

FLEXPort Not Used

When the FLEXPort is not used (no external devices), grounding the EXTARBACK# input is recommended.

FLEXPort Stand-alone Operation

The AIC-7890A/91 may be used in a stand-alone FLEXPort mode by grounding EXTARBACK#. Stand-alone mode indicates that the AIC-7890A/91 will be the only active user of the external resources (SRAM/ROM/EEPROM/SEEPROM/board logic devices). This mode may be verified by reading the state of MPORTMODE bit in the Configuration register. For stand-alone type operation, no external arbiter is required.

FLEXPort Shared Operation

The AIC-7890A/91 may be used in a shared FLEXPort mode by adding an external FLEXPort arbiter. An EXTARBREQ# and EXTARBACK# pair from each device is connected to

the arbiter. The arbiter uses the same clock signal as connected to the AIC-7890A/91's CLKIN pin to sample the EXTARBREQ# signals and control the EXTARBACK# signals in order to facilitate orderly use of the resources. (For a description of the protocol, see *FLEXPort External Arbitration* on page 3-23).

SEEPROM/Board Control Logic Operation

The external FLEXPort may be used to control custom logic. To enable board control, the SEEMS bit in the SEECTL (1E) register must be set. Setting the SEEMS bit will assert EXTARBREQ#. When the EXTARBACK# is asserted (indicated by SEERDY, bit 7 SEECTL register), the board control operations may start. Actual board control is now passed to the SEECTL and BRDCTL registers. These registers are defined in Chapter 4. The external bus is owned as long as the SEEMS bit remains active. Care must be taken not to lock out any other devices (shared operation) for extended periods of time.

Board control to external memory data port signal correlation is shown in Table 3-6.

Table 3-6. BRDCTL Signal Correlation

BRDCTL Register	Register Bit Name	Pin Name	Function
7	BRDDAT7	MD7	I/O
6	BRDDAT6	MD6	I/O
5	BRDDAT5	MD5	I/O
4	BRDDAT4	MD4	I/O
3	BRDDAT3	MD3	I/O
2	BRDDAT2	MDP	I/O
1	BRDRW	*	O
0	BRDSTB	*	O

* BRDWE = !BRDRW & BRDSTB;
BRDOE# = !BRDRW;

The BRDRW signal determines if data is written or read on the MD[7:3] and MDP pins. BRDRW, when high, indicates that the value read from the BRDCTL register is from the external MD[7:3] and MDP lines. BRDRW, when low, indicates that the value written to BRDDAT[7:2] will be driven on the MD[7:3] and MDP pins and may be written into external logic by use of BRDSTB.

It should be noted that MD[2:0] are connected to the SEECTL register when the SEEMS bit is set. The correlation is shown in Table 3-7.

Table 3-7. SEECTL Signal Correlation

SEECTL Register	Register Bit Name	MD Pin Name	Function
2	SEECK	MD2	O
1	SEEDO	MD1	O
0	SEEDI	MDO	I

The following register bits control timing and status of the FLEXPort functions.

Table 3-8. SEECTL Support Functions

SEECTL Register	Register Bit Name	Pin Name	Function
7	EXTARBACK	EXTARBACK#	[1]
6	EXTARBREQ	EXTARBREQ#	[1]
5	SEEMS	none	[2]
4	SEERDY	none	[3]

[1] Read access of arbitration control pins.
[2] SEEPROM/Board Control logic mode selection.
[3] Internal timing function for software usage and mode activation arbitration completed.

FLEXPort External Arbitration

Arbitration for the FLEXPort is accomplished by external logic. The exact functionality of the external arbiter is largely dependent upon the needs of the application, but the following FLEXPort bus arbitration protocol must be adhered to (see the arbitration diagram in Figure 3-3 on page 3-24). The protocol is characterized by the ability for a device to park itself on the bus if no other requests are outstanding. This feature ensures that the external signals are not left in a floating state, and reduces bus access time overhead in some cases. Another important feature is that successive bus grants will always be separated by one cycle, thus eliminating potential bus contention. The maximum number of EXTARBREQ#/EXTARBACK# pair channels is a function of the arbiter design and bus loading. A maximum of 100pf per signal is allowed.

The arbitration protocol is fully interlocked and synchronous (40 MHz clock). This implies that any arbiter design must use the same clock source as the AIC-7890A/91 CLKIN pin. To minimize the effect of skew, only the positive edge of the clock should be used. Typically a device requesting the bus asserts (drives low) its EXTARBREQ# line. In response, the arbiter asserts (drives low) its corresponding EXTARBACK# line. The arbiter asserts one and only one EXTARBACK# signal at any time. The AIC-7890A/91 may park itself on the bus (EXTREQLCK in DSCOMMAND register), by keeping its EXTARBREQ# active (even if no external cycles are run). The arbiter cannot grant the bus to any other devices, until a granted requester de-asserts its EXTARBREQ# line. If another device requests the bus, the present owner of the bus is signalled to remove itself from the bus. This signaling is done by the arbiter by de-asserting the EXTARBACK# signal to the current owner. The current owner relinquishes the bus immediately if not busy, or else immediately following the cycle(s) in progress, by de-asserting its EXTARBREQ# signal. The actual arbiter design may rely on customer requirements (round-robin, fixed priority, etc.) as long as the FLEXPort bus arbitration protocol is maintained.

SCB Array

The internal SCB array consists of a 128x72 SRAM, allowing storage of 16 SCBs (1024 bytes) with parity. It may be accessed by either the host or Sequencer one byte at a time, or by the Command Channel up to one qword at a time during DMA transfers. If external RAM (16Kx8 or 16Kx9) is present, then up to 256 SCBs (16 KBytes) may be stored in the external SRAM.

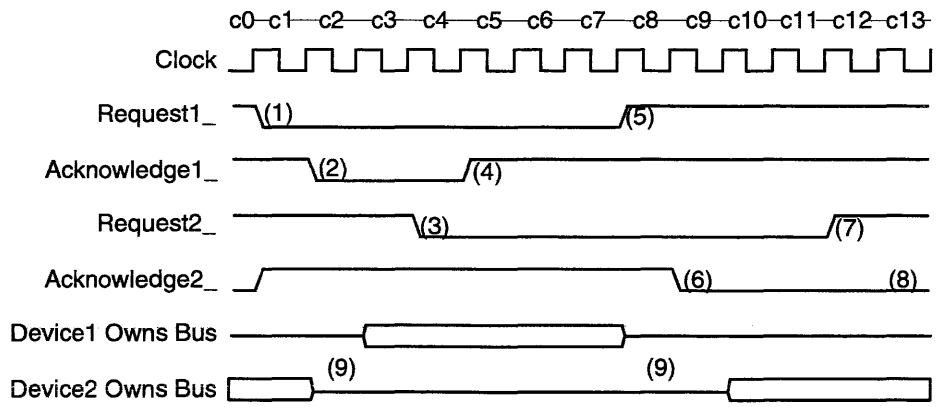
The host can write to the SCB array after the sequencer is paused. The SCB array in normal operation is written to by the command channel, via DMA from host memory. The

SCB array is divided into sections (or pages) which are addressed by the values in SCBPTR and SCBCNT for sequencer access. For DMA access, the individual pages are addressed by the value in CCSCBPTR. Only one 32-byte or 64-byte area of the array can be accessed at any one time. The selected area is mapped to a 64-byte address range (MA0 - MDF, DSA0 - DSDF).

The Auto-Increment feature allows locations to be loaded with minimal CPU overhead. The starting address is loaded in SCBCNT with SCBAUTO enabled. Each write to or read from an SCB array address increments the address to the next location. This feature can be used with sequencer or host CPU block move instructions to quickly load an SCB into the SCB Array. SCBAUTO must be cleared to allow random access to the SCB Array.

Arbitration Protocol

Figure 3-3 shows the arbitration protocol.



All timing on the positive edge of the clock.

(1) Device1 requests bus by asserting Request1_.

(2) Arbiter grants bus to Device1 by asserting Acknowledge1_ (no other requests are active).

(3) Device2 requests bus by asserting Request2_.

(4) Arbiter recognizes Request2_, a new bus request, and removes Acknowledge1_.

(5) Device1 recognizes Acknowledge1_ has been de-asserted, completes its current access, and de-asserts Request1_.

(6) Arbiter recognizes Request1_ has been de-asserted and asserts Acknowledge2_.

(7) Device2 completes its access and de-asserts Request2_.

(8) Arbiter has no active requests and continues to assert Acknowledge2_ to park Device2 on the bus.

(9) Bus exchange cycles, when neither device is driving the bus.

Figure 3-3. Arbitration Protocol

Sequencer

Loading

The sequencer is ready for loading after being reset or paused. The sequencer is loaded by first setting the LOADRAM bit in SEQCTL. The starting sequencer address should then be loaded in SEQADDR, with the low order address written first. The sequencer map should then be loaded sequentially into SEQRAM. The bytes are loaded into the RAM starting with the least significant byte at the address in SEQADDR. Subsequent bytes will load in the same double-word until 4 bytes are loaded, and then SEQADDR is incremented. Parity should be disabled when loaded.

Pause

The sequencer may be paused anytime without adverse effect by setting PAUSE in HCNTRL The sequencer logic will set PAUSEACK in HCNTRL when the hardware is in this state. This state is used by the driver to gain access to any of the internal registers or RAM. When the driver is finished, the PAUSE bit is cleared and the sequencer will continue with its program. When PAUSE is cleared, the sequencer will always execute at least one instruction, even if some other event is active to pause the sequencer. When changing the address of the sequencer to start execution at a different location, SEQADDR0 should be written first, followed by SEQADDR1.

Breakpoint

The sequencer has a diagnostic feature which allows a driver to stop the sequencer at a predetermined address. The address is loaded in BRKADDR0 and BRKADDR1 with BRKDIS (bit 7, BRKADDR1) cleared. When the program counter of the sequencer equals the value loaded in BRKADDR then the sequencer will be paused, and BRKADRINT (bit 3, INTSTAT) will be set. If BRKADRINTEN (bit 3, SEQCTL) is set, the IRQA# pin will also be driven active. BRKADRINT and the interrupt may be cleared by setting CLRBRKADRINT (bit 3, CLRINT). A driver may do any of the following:

- The driver may start execution from the current address and break on the next occurrence by clearing PAUSE.
- The driver may change the break address and clear PAUSE. This will start execution from the current address and break on the new one.
- The driver may single-step the sequencer.
- The driver may change the break address and the program counter, and clear PAUSE. The sequencer will start at a new address and break on a new address.

Single Step

The sequencer may be single-stepped after PAUSE (bit 2, HCNTRL) is set or a breakpoint has been reached. This is done by setting STEP in SEQCTL. The software driver should then clear PAUSE. The sequencer will execute one cycle and set PAUSE again. For consecutive single steps, PAUSE should be cleared consecutive times. To continue executing from the current location, clear STEP and then clear PAUSE.

Reset

The sequencer may be reset by writing to SEQRESET in SEQCTL. Setting this bit will cause the sequencer to start executing at address zero.

Restart

The sequencer may be restarted at any location by first setting PAUSE (bit 2, HCNTRL) and then loading SEQADDR0 and SEQADDR1 with the starting address. When the sequencer is unpaused by clearing PAUSE, the sequencer will start executing at the address that was loaded.

Indirect Jump

The sequencer may jump indirect to any location within the same 256 instruction page by writing the new address to SEQADDR0. The new address is moved from some general RAM location. A bank switch may be performed by setting SEQADDR1.

Hardware Failure Detect

The device has hardware failure detection mechanisms. Sequencer RAM parity errors and data parity errors will be detected and causes a BRKADRINT interrupt which pauses the sequencer and drives the IRQA# pin when enabled. The cause of the interrupt may be read from the ERROR register. If this condition occurs, BRKADRINT bit in INTSTAT register may be cleared by setting CLRPARERR or CHIPRST (bit 0, HCNTRL). This feature may be disabled by setting FAILDIS (bit 5, SEQCTL).

4

Register Description

Register Summary

The AIC-7890A and AIC-7891 register sets are identical, except for the DEVCONFIG (N-40h) register.

PCI Configuration Registers

DEVICE_ID (001Fh)		VENDOR_ID (9005h)	
R/W*N-02h		RN-00h	
15 DEVICE_ID15 = 0	07 DEVICE_ID07 = 0	15 VENDOR_ID15 = 1	07 VENDOR_ID07 = 0
14 DEVICE_ID14 = 0	06 DEVICE_ID06 = 0	14 VENDOR_ID14 = 0	06 VENDOR_ID06 = 0
13 DEVICE_ID13 = 0	05 DEVICE_ID05 = 0	13 VENDOR_ID13 = 0	05 VENDOR_ID05 = 0
12 DEVICE_ID12 = 0	04 DEVICE_ID04 = 1	12 VENDOR_ID12 = 1	04 VENDOR_ID04 = 0
11 DEVICE_ID11 = 0	03 DEVICE_ID03 = 1	11 VENDOR_ID11 = 0	03 VENDOR_ID03 = 0
10 DEVICE_ID10 = 0	02 DEVICE_ID02 = 1	10 VENDOR_ID10 = 0	02 VENDOR_ID02 = 1
09 DEVICE_ID09 = 0	01 DEVICE_ID01 = 1	09 VENDOR_ID09 = 0	01 VENDOR_ID01 = 0
08 DEVICE_ID08 = 0	00 DEVICE_ID00 = 1	08 VENDOR_ID08 = 0	00 VENDOR_ID00 = 1

STATUS		COMMAND	
RN-06h		R/WN-04h	
15 DPE	07 TFBFBC=1	15 RSVD	07 WAITCTLEN=0
14 SSE	06 UDF=0	14 RSVD	06 PERRESPEN
13 RMA	05 66MHZ=0	13 RSVD	05 VSNOOPEN=0
12 RTA	04 CAP_LIST=1	12 RSVD	04 MWRICEN
11 STA	03 RSVD	11 RSVD	03 SPCYCEN = 0
10 DST1=0	02 RSVD	10 RSVD	02 MASTEREN
09 DST0=1	01 RSVD	09 MFBFEN=0	01 MSPACEEN
08 DPR	00 RSVD	08 SERRESPEN	00 ISPACEEN

BASECLASS	SUBCLASS	PROGINFC	DEVREV_ID

RN-0Bh	RN-0Ah	RN-09h	RN-08h
07 BCLASS7=0	07 SCLASS7=0	07 PINFC7=0	07 DEVREV_ID7
06 BCLASS6=0	06 SCLASS6=0	06 PINFC6=0	06 DEVREV_ID6
05 BCLASS5=0	05 SCLASS5=0	05 PINFC5=0	05 DEVREV_ID5
04 BCLASS4=0	04 SCLASS4=0	04 PINFC4=0	04 DEVREV_ID4
03 BCLASS3=0	03 SCLASS3=0	03 PINFC3=0	03 DEVREV_ID3
02 BCLASS2=0	02 SCLASS2=0	02 PINFC2=0	02 DEVREV_ID2
01 BCLASS1=0	01 SCLASS1=0	01 PINFC1=0	01 DEVREV_ID1
00 BCLASS0=1	00 SCLASS0=0	00 PINFC0=0	00 DEVREV_ID0

BIST	HDRTYPE	LAT_TIME	CACHESIZE
RN-0Fh	RN-0Eh	R/WN-0Dh	R/WN-0Ch
07 BIST_CAPABLE = 1	07 MFDEV=0	07 LAT_TIME7	07 CDWDSIZE7
06 START_BIST	06 HTYPE6=0	06 LAT_TIME6	06 CDWDSIZE6
05 RSVD	05 HTYPE5=0	05 LAT_TIME5	05 CDWDSIZE5
04 RSVD	04 HTYPE4=0	04 LAT_TIME4	04 CDWDSIZE4
03 BIST_CODE3	03 HTYPE3=0	03 LAT_TIME3	03 CDWDSIZE3
02 BIST_CODE2	02 HTYPE2=0	02 LAT_TIME2	02 CDWDSIZE2
01 BIST_CODE1	01 HTYPE1=0	01 LAT_TIME1=0	01 CDWDSIZE1=0
00 BIST_CODE0	00 HTYPE0=0	00 LAT_TIME0=0	00 CDWDSIZE0=0

BASEADR0			
R/WN-10h			
31 IBMADR31	23 IBMADR23	15 IBMADR15	07 IBMADR07=0
30 IBMADR30	22 IBMADR22	14 IBMADR14	06 IBMADR06=0
29 IBMADR29	21 IBMADR21	13 IBMADR13	05 IBMADR05=0
28 IBMADR28	20 IBMADR20	12 IBMADR12	04 IBMADR04=0
27 IBMADR27	19 IBMADR19	11 IBMADR11	03 IBMADR03=0
26 IBMADR26	18 IBMADR18	10 IBMADR10	02 IBMADR02=0
25 IBMADR25	17 IBMADR17	09 IBMADR09	01 RSVD
24 IBMADR24	16 IBMADR16	08 IBMADR08	00 ISPACEIND=1

BASEADR1			
R/WN-14h			
31 MBMADR31	23 MBMADR23	15 MBMADR15	07 MBMADR07=0
30 MBMADR30	22 MBMADR22	14 MBMADR14	06 MBMADR06=0
29 MBMADR29	21 MBMADR21	13 MBMADR13	05 MBMADR05=0
28 MBMADR28	20 MBMADR20	12 MBMADR12	04 MBMADR04=0
27 MBMADR27	19 MBMADR19	11 MBMADR11=0	03 PREFETCH =0
26 MBMADR26	18 MBMADR18	10 MBMADR10=0	02 MSPACTYP1=1
25 MBMADR25	17 MBMADR17	09 MBMADR09=0	01 MSPACTYP0=0
24 MBMADR24	16 MBMADR16	08 MBMADR08=0	00 MSPACEIND=0

BASEADR1			
R/WN-18h			
63 MBMADR63	55 MBMADR55	47 MBMADR47	39 MBMADR39
62 MBMADR62	54 MBMADR54	46 MBMADR46	38 MBMADR38
61 MBMADR61	53 MBMADR53	45 MBMADR45	37 MBMADR37
60 MBMADR60	52 MBMADR52	44 MBMADR44	36 MBMADR36
59 MBMADR59	51 MBMADR51	43 MBMADR43	35 MBMADR35
58 MBMADR58	50 MBMADR50	42 MBMADR42	34 MBMADR34
57 MBMADR57	49 MBMADR49	41 MBMADR41	33 MBMADR33
56 MBMADR56	48 MBMADR48	40 MBMADR40	32 MBMADR32

SUBSYSTEM_ID (000Fh default)		SUBVENDOR_ID (9005h default)	
R/W*N-2Eh		R/W*N-2Ch	
15 SUBSYSTEM_ID15	07 SUBSYSTEM_ID07	15 SUBVENDOR_ID15	07 SUBVENDOR_ID07
14 SUBSYSTEM_ID14	06 SUBSYSTEM_ID06	14 SUBVENDOR_ID14	06 SUBVENDOR_ID06
13 SUBSYSTEM_ID13	05 SUBSYSTEM_ID05	13 SUBVENDOR_ID13	05 SUBVENDOR_ID05
12 SUBSYSTEM_ID12	04 SUBSYSTEM_ID04	12 SUBVENDOR_ID12	04 SUBVENDOR_ID04
11 SUBSYSTEM_ID11	03 SUBSYSTEM_ID03	11 SUBVENDOR_ID11	03 SUBVENDOR_ID03
10 SUBSYSTEM_ID10	02 SUBSYSTEM_ID02	10 SUBVENDOR_ID10	02 SUBVENDOR_ID02
09 SUBSYSTEM_ID09	01 SUBSYSTEM_ID01	09 SUBVENDOR_ID09	01 SUBVENDOR_ID01
08 SUBSYSTEM_ID08	00 SUBSYSTEM_ID00	08 SUBVENDOR_ID08	00 SUBVENDOR_ID00

EXROMBADR			
R/WN-30h			
31 EXROMBADR31	23 EXROMBADR23	15 EXROMBADR15=0	07 RSVD
30 EXROMBADR30	22 EXROMBADR22	14 EXROMBADR14=0	06 RSVD
29 EXROMBADR29	21 EXROMBADR21	13 EXROMBADR13=0	05 RSVD
28 EXROMBADR28	20 EXROMBADR20	12 EXROMBADR12=0	04 RSVD
27 EXROMBADR27	19 EXROMBADR19	11 EXROMBADR11=0	03 RSVD
26 EXROMBADR26	18 EXROMBADR18	10 RSVD	02 RSVD
25 EXROMBADR25	17 EXROMBADR17	09 RVSD	01 RSVD
24 EXROMBADR24	16 EXROMBADR16=0	08 RSVD	00 EXROMEN

RESERVED	CAP_PTR
R (All Zeroes) N3B-N35	R N34h
	07 CAP_PTR07 = 1 06 CAP_PTR06 = 1 05 CAP_PTR05 = 0 04 CAP_PTR04 = 1 03 CAP_PTR03 = 1 02 CAP_PTR02 = 1 01 CAP_PTR01 = 0 00 CAP_PTR00 = 0

MAXLAT	MINGNT	INTPINSEL	INTLINSEL
RN-3Fh	RN-3Eh	RN-3Dh	R/WN-3Ch
07 MAXLAT7=0	07 MINGNT7=0	07 INTPS7=0	07 INTLS7
06 MAXLAT6=0	06 MINGNT6=0	06 INTPS6=0	06 INTLS6
05 MAXLAT5=0	05 MINGNT5=1	05 INTPS5=0	05 INTLS5
04 MAXLAT4=1	04 MINGNT4=0	04 INTPS4=0	04 INTLS4
03 MAXLAT3=1	03 MINGNT3=0	03 INTPS3=0	03 INTLS3
02 MAXLAT2=0	02 MINGNT2=1	02 INTPS2=0	02 INTLS2
01 MAXLAT1=0	01 MINGNT1=1	01 INTPS1=0	01 INTLS1
00 MAXLAT0=1	00 MINGNT0=1	00 INTPS0=1	00 INTLS0

PCIERRORGEN	DEVSTATUS1	DEVSTATUS0	DEVCONFIG
R/WN-43h	R/WN-42h	R/WN-41h	R/WN-40h
07 PCIERRGENDIS	07 DMABIGENDIAN	07 DMABIGENDIAN	07 PCI64BIT
06 DIS_SCHMITT	06 TARBIGENDIAN	06 TARBIGENDIAN	06 MRDCEN
05 RSVD	05 RSVD	05 RSVD	05 RSVD
04 MADRSPARERR	04 RSVD	04 RSVD	04 EXTSCBPEN
03 MWDATPARERR	03 RSVD	03 TESTMODE (RO)	03 RSVD
02 TRDATAPARERR	02 RSVD	02 MPORTMODE (RO)	02 DACEN
01 MTDATAPARERR	01 RSVD	01 RSVD	01 STPWLEVEL
00 TADRSPARERR	00 RSVD	00 VOLSENSE (RO)	00 RSVD

RESERVED	
R	N-DBh-44h
07 RSVD	
06 RSVD	
05 RSVD	
04 RSVD	
03 RSVD	
02 RSVD	
01 RSVD	
00 RSVD	

PM_CAPABILITY		NEXT_ITEM_PTR	CAPABILITY_ID
R/W	N-DEh	R N-DDh	R N-DCh
15 PME_SUPPORT4 = 0	07 RSVD	07 NEXT_ITEM_PTR07 = 0	07 CAP_ID07 = 0
14 PME_SUPPORT3 = 0	06 RSVD	06 NEXT_ITEM_PTR06 = 0	06 CAP_ID06 = 0
13 PME_SUPPORT2 = 0	05 DSI = 0	05 NEXT_ITEM_PTR05 = 0	05 CAP_ID05 = 0
12 PME_SUPPORT1 = 0	04 AUX_POWER = 0	04 NEXT_ITEM_PTR04 = 0	04 CAP_ID04 = 0
11 PME_SUPPORT0 = 0	03 PME_CLOCK = 0	03 NEXT_ITEM_PTR03 = 0	03 CAP_ID03 = 0
10 D2_SUPPORT = 0	02 PM_VERSION2 = 0	02 NEXT_ITEM_PTR02 = 0	02 CAP_ID02 = 0
09 D1_SUPPORT = 0	01 PM_VERSION1 = 0	01 NEXT_ITEM_PTR01 = 0	01 CAP_ID01 = 0
08 RSVD	00 PM_VERSION0 = 1	00 NEXT_ITEM_PTR00 = 0	00 CAP_ID00 = 1

PM_DATA		PMCSR_BSE		PM_CSR	
R	N-E3h	R	N-E2h	R/W	N-E0h
07 PM_DATA07 = 0		07 BPCC_EN = 0		15 PME_STATUS = 0	07 RSVD
06 PM_DATA06 = 0		06 B2_B3# = 0		14 DATA_SCALE1 = 0	06 RSVD
05 PM_DATA05 = 0		05 RSVD		13 DATA_SCALE0 = 0	05 RSVD
04 PM_DATA04 = 0		04 RSVD		12 DATA_SELECT3 = 0	04 RSVD
03 PM_DATA03 = 0		03 RSVD		11 DATA_SELECT2 = 0	03 RSVD
02 PM_DATA02 = 0		02 RSVD		10 DATA_SELECT1 = 0	02 RSVD
01 PM_DATA01 = 0		01 RSVD		09 DATA_SELECT0 = 0	01 POWER_STATE1
00 PM_DATA00 = 0		00 RSVD		08 PME_EN = 0	00 POWER_STATE0

IDENREG+
R/W N-FFh
07 RSVD
06 RSVD
05 RSVD
04 RSVD
03 RSVD
02 RSVD
01 RSVD
00 IDWEN

(RO) - Read Only

*These registers are not writeable in revision 0 chips (DEVREV_ID = 09h)

+The IDENREG register was added after revision 0 of the chip (DEVREV_ID = 00h). In revision 0 chips, register location FFh in the PCI configuration space is reserved.

Device Registers in the Functional Mode (ALT_MODE = 0)

Device Registers are divided into two 256-byte pages, and can be selected with the ALT_MODE bit (bit-7) of SFUNCT (9Fh) register. When ALT_MODE = 0, the Functional mode is selected. When ALT_MODE = 1, the Alternate mode is selected.

Prefix and Suffix Definitions:

M - Address offset from AIC-7890A/91 assigned PCI memory space or memory mapped I/O space base address.

DS - AIC-7890A/91 Internal Device Space Physical Address.

SCSISIGI	SCSISIGO	SXFRCTL1	SXFRCTL0	SCSISEQ
RM/DS 03h	WM/DS 03h	R/WM/DS 02h	R/WM/DS 01h	R/WM/DS 00h
7 CDI	7 CDO	7 BITBUCKET	7 DFON	7 TEMODEO
6 IOI	6 IOO	6 RSVD	6 DFPEXP	6 ENSELO
5 MSGI	5 MSGO	5 ENSPCHK	5 RSVD	5 ENSELI
4 ATNI	4 IATNO	4 STIMESEL1	4 CLRSTCNT	4 ENRSELI
3 SELI	3 SELO	3 STIMESEL0	3 SPIOEN	3 ENAUTOATNO
2 BSYI	2 BSYO	2 ENSTIMER	2 SCAMEN	2 ENAUTOATNI
1 REQI	1 TREQO	1 ACTNEGEN	1 CLRCHN	1 ENAUTOATNP
0 ACKI	0 ACKO	0 STPWEN	0 RSVD	0 SCSIRSTO

SCSIDATH	SCSIDATL	SCSIOFFSET	SCSIRATE
R/WM/DS 07h	R/WM/DS 06h	R/WM/DS 05h	R/WM/DS 04h
7 DB15	7 DB07	7 RSVD	7 WIDEXFER
6 DB14	6 DB06	6 SCSIOFFSET6	6 XFERRATE6
5 DB13	5 DB05	5 SCSIOFFSET5	5 XFERRATE5
4 DB12	4 DB04	4 SCSIOFFSET4	4 XFERRATE4
3 DB11	3 DB03	3 SCSIOFFSET3	3 XFERRATE3
2 DB10	2 DB02	2 SCSIOFFSET2	2 XFERRATE2
1 DB09	1 DB01	1 SCSIOFFSET1	1 XFERRATE1
0 DB08	0 DB00	0 SCSIOFFSET0	0 XFERRATE0

SSTAT0	CLRSINT0	STCNT2	STCNT1	STCNT0
RM/DS 0Bh	WM/DS 0Bh	R/WM/DS 0Ah	R/WM/DS 09h	R/WM/DS 08h
7 TARGET	7 RSVD	7 STCNT23	7 STCNT15	7 STCNT07
6 SELDO	6 CLRSELDO	6 STCNT22	6 STCNT14	6 STCNT06
5 SELDI	5 CLRSELDI	5 STCNT21	5 STCNT13	5 STCNT05
4 SELINGO	4 CLRSELINGO	4 STCNT20	4 STCNT12	4 STCNT04
3 IOERR	3 CLRIOERR	3 STCNT19	3 STCNT11	3 STCNT03
2 SDONE	2 RSVD	2 STCNT18	2 STCNT10	2 STCNT02
1 SPIORDY	1 CLRSPIORDY	1 STCNT17	1 STCNT09	1 STCNT01
0 DMADONE	0 RSVD	0 STCNT16	0 STCNT08	0 STCNT00

SCSIID	SSTAT3	SSTAT2	SSTAT1	CLRSINT1
R/WM/DS 0Fh	RM/DS 0Eh	RM/DS 0Dh	RM/DS 0Ch	WM/DS 0Ch
7 TID3	7 RSVD	7 OVERRUN	7 SELTO	7 CLRSELTIMO
6 TID2	6 OFFCNT6	6 SHVALID	6 ATNTARG	6 CLRATNO
5 TID1	5 OFFCNT5	5 WIDE_RES	5 SCSIRSTI	5 CLRSCSIRSTI
4 TID0	4 OFFCNT4	4 EXP_ACTIVE	4 PHASEMIS	4 RSVD
3 OID3	3 OFFCNT3	3 RSVD	3 BUSFREE	3 CLRBUSFREE
2 OID2	2 OFFCNT2	2 RSVD	2 SCSIPERR	2 CLRSCSIPERR
1 OID1	1 OFFCNT1	1 RSVD	1 PHASECHG	1 CLRPHASECHG
0 OID0	0 OFFCNT0	0 RSVD	0 REQINIT	0 CLRREQINIT

SCSIBUSH	SCSIBUSL	SIMODE1	SIMODE0
R/WM/DS 13h	R/WM/DS 12h	R/WM/DS 11h	R/WM/DS 10h
7 SDB15	7 SDB07	7 ENSELTIMO	7 ENSCAMSELD
6 SDB14	6 SDB06	6 ENATNTARG	6 ENSELDO
5 SDB13	5 SDB05	5 ENSCSIRST	5 ENSELDI
4 SDB12	4 SDB04	4 ENPHASEMIS	4 ENSELINGO
3 SDB11	3 SDB03	3 ENBUSFREE	3 ENIOERR
2 SDB10	2 SDB02	2 ENSCSIPERR	2 ENSDONE
1 SDB09	1 SDB01	1 ENPHASECHG	1 ENSPIORDY
0 SDB08	0 SDB00	0 ENREQINIT	0 ENDMADONE

SHADDR3	SHADDR2	SHADDR1	SHADDR0
R/WM/DS 17h	R/WM/DS 16h	R/WM/DS 15h	R/WM/DS 14h
7 SHADDR31	7 SHADDR23	7 SHADDR15	7 SHADDR07
6 SHADDR30	6 SHADDR22	6 SHADDR14	6 SHADDR06
5 SHADDR29	5 SHADDR21	5 SHADDR13	5 SHADDR05
4 SHADDR28	4 SHADDR20	4 SHADDR12	4 SHADDR04
3 SHADDR27	3 SHADDR19	3 SHADDR11	3 SHADDR03
2 SHADDR26	2 SHADDR18	2 SHADDR10	2 SHADDR02
1 SHADDR25	1 SHADDR17	1 SHADDR09	1 SHADDR01
0 SHADDR24	0 SHADDR16	0 SHADDR08	0 SHADDR00

SHADDR7	SHADDR6	SHADDR5	SHADDR4
R/W M/DS 17h	R/WM/DS 16h	R/WM/DS 15h	R/WM/DS 14h
7 SHADDR63	7 SHADDR55	7 SHADDR47	7 SHADDR39
6 SHADDR62	6 SHADDR54	6 SHADDR46	6 SHADDR38
5 SHADDR61	5 SHADDR53	5 SHADDR45	5 SHADDR37
4 SHADDR60	4 SHADDR52	4 SHADDR44	4 SHADDR36
3 SHADDR59	3 SHADDR51	3 SHADDR43	3 SHADDR35
2 SHADDR58	2 SHADDR50	2 SHADDR42	2 SHADDR34
1 SHADDR57	1 SHADDR49	1 SHADDR41	1 SHADDR33
0 SHADDR56	0 SHADDR48	0 SHADDR40	0 SHADDR32

TARGIDL	SCAMSTAT	SCAMCTL	SELID	TARGIDIN
R/W M/DS 1Bh	R M/DS 1Ah	W M/DS 1Ah	RM/DS 19h	R M/DS 18h
7 TARGIDEN07	7	7 ENSCAMSELO	7 SELID3	7 CLKOUT
6 TARGIDEN06	SCAMSELOSTAT	6 CLRSCAMSELD	6 SELID2	6 RSVD
5 TARGIDEN05	6 SCAMSELD	5 ALTSTIM	5 SELID1	5 RSVD
4 TARGIDEN04	5 ALTSTIM	4 DFLTID	4 SELID0	4 RSVD
3 TARGIDEN03	4 DFLTID	3 Not used	3 ONEBIT	3 TARGID3
2 TARGIDEN02	3 RSVD	2 Not used	2 RSVD	2 TARGID2
1 TARGIDEN01	2 RSVD	1 SCAMLVL1	1 RSVD	1 TARGID1
0 TARGIDEN00	1 SCAMLVL1	0 SCAMLVL0	0 RSVD	0 TARGID0
	0 SCAMLVL0			

SBLKCTL	SEECTL	BRDCTL	TARGIDH
R/W M/DS 1Fh	R/WM/DS 1Eh	R/WM/DS 1Dh	R/W M/DS 1Ch
7 DIAGLEDEN	7 EXTARBACK (RO)	7 BRDDAT7	7 TARGIDEN15
6 DIAGLEDON	6 EXTARBREQ (RO)	6 BRDDAT6	6 TARGIDEN14
5 AUTOFLUSHDIS	5 SEEMS	5 BRDDAT5	5 TARGIDEN13
4 RSVD	4 SEERDY (RO)	4 BRDDAT4	4 TARGIDEN12
3 ENAB40	3 SEECS	3 BRDDAT3	3 TARGIDEN11
2 ENAB20	2 SEECK	2 BRDDAT2	2 TARGIDEN10
1 SELWIDE	1 SEEDO	1 BRDRW	1 TARGIDEN09
0 XCVR	0 SEEDI (RO)	0 BRDSTB	0 TARGIDEN08

SCRATCH RAM
R/W M/DS-5Fh~20h
7 SCRATCH_DAT7
6 SCRATCH_DAT6
5 SCRATCH_DAT5
4 SCRATCH_DAT4
3 SCRATCH_DAT3
2 SCRATCH_DAT2
1 SCRATCH_DAT1
0 SCRATCH_DAT0

SEQADDR1	SEQADDR0	SEQRAM	SEQCTL
R/W M/DS-63h	R/W M/DS-62h	R/W M/S-61h	R/W M/DS-60h
15 RSVD	7 SEQADDR07	7 SEQRAM07	7 PERRORDIS
14 RSVD	6 SEQADDR06	6 SEQRAM06	6 PAUSEDIS
13 RSVD	5 SEQADDR05	5 SEQRAM05	5 FAILDIS
12 RSVD	4 SEQADDR04	4 SEQRAM04	4 FASTMODE
11 RSVD	3 SEQADDR03	3 SEQRAM03	3 BRKADRINTEN
10 RSVD	2 SEQADDR02	2 SEQRAM02	2 STEP
9 SEQADDR09	1 SEQADDR01	1 SEQRAM01	1 SEQRESET
8 SEQADDR08	0 SEQADDR00	0 SEQRAM00	0 LOADRAM

BRKADDR0	DINDEX	SINDEX	ACCUM
R/W M67h, DS-67h	R/W M66h, DS-66h	R/W M65h, DS-65h	R/W M64h, DS-64h
7 BRKADDR07	7 DINDEX07	7 SINDEX07	7 ACCUM07
6 BRKADDR06	6 DINDEX06	6 SINDEX06	6 ACCUM06
5 BRKADDR05	5 DINDEX05	5 SINDEX05	5 ACCUM05
4 BRKADDR04	4 DINDEX04	4 SINDEX04	4 ACCUM04
3 BRKADDR03	3 DINDEX03	3 SINDEX03	3 ACCUM03
2 BRKADDR02	2 DINDEX02	2 SINDEX02	2 ACCUM02
1 BRKADDR01	1 DINDEX01	1 SINDEX01	1 ACCUM01
0 BRKADDR00	0 DINDEX00	0 SINDEX00	0 ACCUM00

FLAGS	NONE0	ALLZEROS	ALLONES	BRKADDR1
R M6Bh, DS-6Bh	W M6Ah, DS-6Ah	R M6Ah, DS-6Ah	R M69h, DS-69h	R/W M68h, DS-68h
7 RSVD	7 RSVD	7 =0	7 =1	7 BRKDIS
6 RSVD	6 RSVD	6 =0	6 =1	6 RSVD
5 RSVD	5 RSVD	5 =0	5 =1	5 RSVD
4 RSVD	4 RSVD	4 =0	4 =1	4 RSVD
3 RSVD	3 RSVD	3 =0	3 =1	3 RSVD
2 RSVD	2 RSVD	2 =0	2 =1	2 RSVD
1 ZERO	1 RSVD	1 =0	1 =1	1 BRKADDR09
0 CARRY	0 RSVD	0 =0	0 =1	0 BRKADDR08

STACK	FUNCTIONONE	FUNCTIONONE	DINDIR	SINDIR
R M6Fh, DS-6Fh	R M6Eh, DS-6Eh	W M6Eh, DS-6Eh	W DS-6Dh	RDS-6Ch
7 STACK7	7 FUNONEDAT7	7 NOT USED	CONTENTS POINTED TO BY DINDEX	CONTENTS POINTED TO BY SINDEX
6 STACK6	6 FUNONEDAT6	6 FUNCTION2		
5 STACK5	5 FUNONEDAT5	5 FUNCTION1		
4 STACK4	4 FUNONEDAT4	4 FUNCTION0		
3 STACK3	3 FUNONEDAT3	3 NOT USED		
2 STACK2	2 FUNONEDAT2	2 NOT USED		
1 STACK1	1 FUNONEDAT1	1 NOT USED		
0 STACK0	0 FUNONEDAT0	0 NOT USED		

SCRATCH RAM
R/W M/DS-7Fh~70h
7 SCRATCH_DAT7
6 SCRATCH_DAT6
5 SCRATCH_DAT5
4 SCRATCH_DAT4
3 SCRATCH_DAT3
2 SCRATCH_DAT2
1 SCRATCH_DAT1
0 SCRATCH_DAT0

RESERVED	RESERVED	RESERVED	RESERVED
RM-83h	RM-82h	RM-81h	RM-80h
7 RSVD	7 RSVD	7 RSVD	7 RSVD
6 RSVD	6 RSVD	6 RSVD	6 RSVD
5 RSVD	5 RSVD	5 RSVD	5 RSVD
4 RSVD	4 RSVD	4 RSVD	4 RSVD
3 RSVD	3 RSVD	3 RSVD	3 RSVD
2 RSVD	2 RSVD	2 RSVD	2 RSVD
1 RSVD	1 RSVD	1 RSVD	1 RSVD
0 RSVD	0 RSVD	0 RSVD	0 RSVD

HCNTRL	HS_MAILBOX	DSCOMMAND1	DSCOMMAND0
R/WM-87h	R/WM/DS-86h	R/WM/DS-85h	R/WM/DS-84h
7 RSVD	7 HOST_MAILBOX3	7 RSVD	7 CACHETHEN
6 POWRDN	6 HOST_MAILBOX2	6 RSVD	6 DPARCKEN
5 RSVD	5 HOST_MAILBOX1	5 RSVD	5 MPARCKEN
4 SWINT	4 HOST_MAILBOX0	4 RSVD	4 EXTREQLCK
3 HCNTRL3	3 SEQ_MAILBOX3	3 RSVD	3 INTSCBRAMSEL
2 PAUSE[ACK]	2 SEQ_MAILBOX2	2 RSVD	2 RAMPSM
1 INTEN	1 SEQ_MAILBOX1	1 HADDRLDSEL1	1 SCBSIZE32
0 CHIPRST[ACK]	0 SEQ_MAILBOX0	0 HADDRLDSEL0	0 CIOPARCKEN

HADDR3	HADDR2	HADDR1	HADDR0
R/WM/DS-8Bh	R/WM/DS-8Ah	R/WM/DS-89h	R/WM/DS-88h
7 HADDR31	7 HADDR23	7 HADDR15	7 HADDR07
6 HADDR30	6 HADDR22	6 HADDR14	6 HADDR06
5 HADDR29	5 HADDR21	5 HADDR13	5 HADDR05
4 HADDR28	4 HADDR20	4 HADDR12	4 HADDR04
3 HADDR27	3 HADDR19	3 HADDR11	3 HADDR03
2 HADDR26	2 HADDR18	2 HADDR10	2 HADDR02
1 HADDR25	1 HADDR17	1 HADDR09	1 HADDR01
0 HADDR24	0 HADDR16	0 HADDR08	0 HADDR00

HADDR7	HADDR6	HADDR5	HADDR4
R/WM/DS-8Bh	R/WM/DS-8Ah	R/WM/DS-89h	R/WM/DS-88h
7 HADDR63	7 HADDR55	7 HADDR47	7 HADDR39
6 HADDR62	6 HADDR54	6 HADDR46	6 HADDR38
5 HADDR61	5 HADDR53	5 HADDR45	5 HADDR37
4 HADDR60	4 HADDR52	4 HADDR44	4 HADDR36
3 HADDR59	3 HADDR51	3 HADDR43	3 HADDR35
2 HADDR58	2 HADDR50	2 HADDR42	2 HADDR34
1 HADDR57	1 HADDR49	1 HADDR41	1 HADDR33
0 HADDR56	0 HADDR48	0 HADDR40	0 HADDR32

RSVD	HCNT2	HCNT1	HCNT0
RM/DS-8Fh	R/WM/DS-8Eh	R/WM/DS-8Dh	R/WM/DS-8Ch
7 RSVD	7 HCNT23	7 HCNT15	7 HCNT07
6 RSVD	6 HCNT22	6 HCNT14	6 HCNT06
5 RSVD	5 HCNT21	5 HCNT13	5 HCNT05
4 RSVD	4 HCNT20	4 HCNT12	4 HCNT04
3 RSVD	3 HCNT19	3 HCNT11	3 HCNT03
2 RSVD	2 HCNT18	2 HCNT10	2 HCNT02
1 RSVD	1 HCNT17	1 HCNT09	1 HCNT01
0 RSVD	0 HCNT16	0 HCNT08	0 HCNT00

DFCNTRL	ERROR	CLRINT	INTSTAT	SCBPTR
R/WM/DS-93h	RM-92h	W M-92h	R/WM/DS-91h	R/WM/DS 90h
7 PRELOADEN 6 RSVD 5 SCSIEN[ACK] 4 RSVD 3 HDMAEN[ACK] 2 DIRECTION[ACK] 1 FIFOFLUSH[ACK] 0 RSVD	7 CIOPARERR 6 PCIERRSTAT 5 MPARERR 4 DPARERR 3 SQPARERR 2 ILLOPCODE 1 RSVD 0 RSVD	7 RSVD 6 RSVD 5 RSVD 4 CLRPARERR 3 CLRBRKADRINT 2 CLRSCSIINT 1 CLRCMDINT 0 CLRSEQINT	7 INTCODE3 6 INTCODE2 5 INTCODE1 4 INTCODE0 3 BRKADRINT 2 SCSIINT 1 CMDCMPLT 0 SEQINT	7 SCBVAL7 6 SCBVAL6 5 SCBVAL5 4 SCBVAL4 3 SCBVAL3 2 SCBVAL2 1 SCBVAL1 0 SCBVAL0

DFRADDR	RSVD	DFWADDR	DFSTATUS
R/WM/DS 97h	RM/DS 96h	R/WM/DS 95h	RM/DS-94h
7 RSVD	7 RSVD	7 RSVD	7 PRELOAD_AVAIL
6 DFRADDR06	6 RSVD	6 DFWADDR06	6 RSVD
5 DFRADDR05	5 RSVD	5 DFWADDR05	5 RSVD
4 DFRADDR04	4 RSVD	4 DFWADDR04	4 MREQPEND
3 DFRADDR03	3 RSVD	3 DFWADDR03	3 HDONE
2 DFRADDR02	2 RSVD	2 DFWADDR02	2 DFTHRSH
1 DFRADDR01	1 RSVD	1 DFWADDR01	1 FIFOFULL
0 DFRADDR00	0 RSVD	0 DFWADDR00	0 FIFOEMP

RSVD	SCBCNT	DFDAT	RSVD
RM/DS 9Bh	R/WM/DS 9Ah	R/WM/DS 99h	RM/DS 98h
7 RSVD	7 SCBAUTO	7 DFDAT7	7 RSVD
6 RSVD	6 RSVD	6 DFDAT6	6 RSVD
5 RSVD	5 SCBCNT5	5 DFDAT5	5 RSVD
4 RSVD	4 SCBCNT4	4 DFDAT4	4 RSVD
3 RSVD	3 SCBCNT3	3 DFDAT3	3 RSVD
2 RSVD	2 SCBCNT2	2 DFDAT2	2 RSVD
1 RSVD	1 SCBCNT1	1 DFDAT1	1 RSVD
0 RSVD	0 SCBCNT0	0 DFDAT0	0 RSVD

SFUNCT	RSVD	RSVD	RSVD
R/WM/DS-9Fh	RM/DS-9Eh	RM/DS 9Dh	RM/DS 9Ch
7 ALT_MODE	7 RSVD	7 RSVD	7 RSVD
6 GROUP3	6 RSVD	6 RSVD	6 RSVD
5 GROUP2	5 RSVD	5 RSVD	5 RSVD
4 GROUP1	4 RSVD	4 RSVD	4 RSVD
3 GROUP0	3 RSVD	3 RSVD	3 RSVD
2 TEST2	2 RSVD	2 RSVD	2 RSVD
1 TEST1	1 RSVD	1 RSVD	1 RSVD
0 TEST0	0 RSVD	0 RSVD	0 RSVD

SCB RAM
R/WM/DS-DFh~A0h
7 SCBRAM7
6 SCBRAM6
5 SCBRAM5
4 SCBRAM4
3 SCBRAM3
2 SCBRAM2
1 SCBRAM1
0 SCBRAM0

CCHADDR3	CCHADDR2	CCHADDR1	CCHADDR0
R/WM/DS-E3h	R/WM/DS-E2h	R/WM/DS-E1h	R/WM/DS-E0h
7 CCHADDR31	7 CCHADDR23	7 CCHADDR15	7 CCHADDR07
6 CCHADDR30	6 CCHADDR22	6 CCHADDR14	6 CCHADDR06
5 CCHADDR29	5 CCHADDR21	5 CCHADDR13	5 CCHADDR05
4 CCHADDR28	4 CCHADDR20	4 CCHADDR12	4 CCHADDR04
3 CCHADDR27	3 CCHADDR19	3 CCHADDR1	3 CCHADDR03
2 CCHADDR26	2 CCHADDR18	2 CCHADDR10	2 CCHADDR02
1 CCHADDR25	1 CCHADDR17	1 CCHADDR09	1 CCHADDR01
0 CCHADDR24	0 CCHADDR16	0 CCHADDR08	0 CCHADDR00

CCHADDR7	CCHADDR6	CCHADDR5	CCHADDR4
R/WM/DS-E7h	R/WM/DS-E6h	R/WM/DS-E5h	R/WM/DS-E4h
7 CCHADDR63	7 CCHADDR55	7 CCHADDR47	7 CCHADDR39
6 CCHADDR62	6 CCHADDR54	6 CCHADDR46	6 CCHADDR38
5 CCHADDR61	5 CCHADDR53	5 CCHADDR45	5 CCHADDR37
4 CCHADDR60	4 CCHADDR52	4 CCHADDR44	4 CCHADDR36
3 CCHADDR59	3 CCHADDR51	3 CCHADDR43	3 CCHADDR35
2 CCHADDR58	2 CCHADDR50	2 CCHADDR42	2 CCHADDR34
1 CCHADDR57	1 CCHADDR49	1 CCHADDR41	1 CCHADDR33
0 CCHADDR56	0 CCHADDR48	0 CCHADDR40	0 CCHADDR32

CCSGCTL	CCSGADR	CCSGRAM	CCHCNT
R/WM/DS EBh	R/WM/DS EAh	RM/DS E9h	R/WM/DS-E8h
7 CCSGDONE	7 CCSGADR7	7 CCSGRAM7	7 CCHCNT7
6 RSVD	6 CCSGADR6	6 CCSGRAM6	6 CCHCNT6
5 RSVD	5 CCSGADR5	5 CCSGRAM5	5 CCHCNT5
4 RSVD	4 CCSGADR4	4 CCSGRAM4	4 CCHCNT4
3 CCSGEN[ACK]	3 CCSGADR3	3 CCSGRAM3	3 CCHCNT3
2 RSVD	2 CCSGADR2	2 CCSGRAM2	2 CCHCNT2
1 FLAG	1 CCSGADR1	1 CCSGRAM1	1 CCHCNT1
0 CCSGRESET	0 CCSGADR0	0 CCSGRAM0	0 CCHCNT0

CCSCBCNT	CCSCBCTL	CCSCBADR	CCSCBRAM
R/WM/DS EFh	R/WM/DS EEh	R/WM/DS EDh	R/WM/DS ECh
7 CCSCBCNT7	7 CCSCBDONE	7 CCSCBADR7	7 CCSCBRAM7
6 CCSCBCNT6	6 ARRDONE	6 CCSCBADR6	6 CCSCBRAM6
5 CCSCBCNT5	5 RSVD	5 CCSCBADR5	5 CCSCBRAM5
4 CCSCBCNT4	4 CCARREN[ACK]	4 CCSCBADR4	4 CCSCBRAM4
3 CCSCBCNT3	3 CCSCBEN[ACK]	3 CCSCBADR3	3 CCSCBRAM3
2 CCSCBCNT2	2 CCSCBDIR[ACK]	2 CCSCBADR2	2 CCSCBRAM2
1 CCSCBCNT1	1 RSVD	1 CCSCBADR1	1 CCSCBRAM1
0 CCSCBCNT0	0 CCSCBRESET	0 CCSCBADR0	0 CCSCBRAM0

RSVD	RSVD	CCSCBPTR	SCBBADDR
R/WM/DS F3h	R/WM/DS F2h	R/WM/DS F1h	R/WM/DS F0h
7 RSVD	7 RSVD	7 CCSCBPTR7	7 RSVD
6 RSVD	6 RSVD	6 CCSCBPTR6	6 RSVD
5 RSVD	5 RSVD	5 CCSCBPTR5	5 RSVD
4 RSVD	4 RSVD	4 CCSCBPTR4	4 RSVD
3 RSVD	3 RSVD	3 CCSCBPTR3	3 RSVD
2 RSVD	2 RSVD	2 CCSCBPTR2	2 RSVD
1 RSVD	1 RSVD	1 CCSCBPTR1	1 RSVD
0 RSVD	0 RSVD	0 CCSCBPTR0	0 SCBBADDR0

RSVD	SNSCB_QOFF	RSVD	HNSCB_QOFF
RM/DS-F7h	R/WM/DS-F6h	RM/DS-F5h	R/WM/DS-F4h
7 RSVD	7 SNSCB_QOFF07	7 RSVD	7 HNSCB_QOFF07
6 RSVD	6 SNSCB_QOFF06	6 RSVD	6 HNSCB_QOFF06
5 RSVD	5 SNSCB_QOFF05	5 RSVD	5 HNSCB_QOFF05
4 RSVD	4 SNSCB_QOFF04	4 RSVD	4 HNSCB_QOFF04
3 RSVD	3 SNSCB_QOFF03	3 RSVD	3 HNSCB_QOFF03
2 RSVD	2 SNSCB_QOFF02	2 RSVD	2 HNSCB_QOFF02
1 RSVD	1 SNSCB_QOFF01	1 RSVD	1 HNSCB_QOFF01
0 RSVD	0 SNSCB_QOFF00	0 RSVD	0 HNSCB_QOFF00

DFF_THRSH	QOFF_CTLSTA	RSVD	SDSCB_QOFF
R/WM/DS-FBh	R/WM/DS-FAh	RM/DS-F9h	R/WM/DS-F8h
7 RSVD	7 RSVD	7 RSVD	7 SDSCB_QOFF07
6 WR_DFTHRSH2	6 SCB_AVAIL	6 RSVD	6 SDSCB_QOFF06
5 WR_DFTHRSH1	5 SNSCB_ROLLOVER	5 RSVD	5 SDSCB_QOFF05
4 WR_DFTHRSH0	4 SDSCB_ROLLOVER	4 RSVD	4 SDSCB_QOFF04
3 RSVD	3 RSVD	3 RSVD	3 SDSCB_QOFF03
2 RD_DFTHRSH2	2 SCB_QSIZE2	2 RSVD	2 SDSCB_QOFF02
1 RD_DFTHRSH1	1 SCB_QSIZE1	1 RSVD	1 SDSCB_QOFF01
0 RD_DFTHRSH0	0 SCB_QSIZE0	0 RSVD	0 SDSCB_QOFF00

CSDATH/CDDATH (RSVD)	CSDATL/CDDATL	RSVD	SG_CACHEPTR
RM/DS-FFh	RM/DS-FEh	RM/DS-FDh	RM/DS-FCh
7 RSVD	7 CSDAT07/CDDAT07	7 RSVD	7 SG_CACHEPTR7
6 RSVD	6 CSDAT06/C DDAT06	6 RSVD	6 SG_CACHEPTR6
5 RSVD	5 CSDAT05/CDDAT05	5 RSVD	5 SG_CACHEPTR5
4 RSVD	4 CSDAT04/CDDAT04	4 RSVD	4 SG_CACHEPTR4
3 RSVD	3 CSDAT03/CDDAT03	3 RSVD	3 SG_CACHEPTR3
2 RSVD	2 CSDAT02/CDDAT02	2 RSVD	2 SG_CACHEPTR2
1 RSVD	1 CSDAT01/CDDAT01	1 RSVD	1 SG_CACHEPTR1
0 RSVD	0 CSDAT00/CDDAT00	0 RSVD	0 SG_CACHEPTR0

Device Registers in the Alternate Mode (ALT_MODE = 1)

Device Registers are divided into two 256-byte pages, and can be selected with ALT_MODE bit (bit-7) of SFUNCT (9Fh) register. When ALT_MODE = 0, the Functional mode is selected. When ALT_MODE = 1, the Alternate mode is selected.

Prefix and Suffix Definitions:

M - Address offset from AIC-7890A/91 assigned PCI memory space or memory mapped I/O space base address.

DS - AIC-7890A/91 Internal Device Space Physical Address.

BUSFREE3	BUSFREE2	BUSFREE1	BUSFREE0
RM/DS -03h	R M/DS - 02h	RM/DS -01h	RM/DS -00h
7 BFREE31	7 BFREE23	7 BFREE15	7 BFREE07
6 BFREE30	6 BFREE22	6 BFREE14	6 BFREE06
5 BFREE29	5 BFREE21	5 BFREE13	5 BFREE05
4 BFREE28	4 BFREE20	4 BFREE12	4 BFREE04
3 BFREE27	3 BFREE19	3 BFREE11	3 BFREE03
2 BFREE26	2 BFREE18	2 BFREE10	2 BFREE02
1 BFREE25	1 BFREE17	1 BFREE09	1 BFREE01
0 BFREE24	0 BFREE16	0 BFREE08	0 BFREE00

BUSBSY3	BUSBSY2	BUSBSY1	BUSBSY0
RM/DS -07h	R M/DS - 06h	RM/DS - 05h	RM/DS -04h
7 BBSY31	7 BBSY23	7 BBSY15	7 BBSY07
6 BBSY30	6 BBSY22	6 BBSY14	6 BBSY06
5 BBSY29	5 BBSY21	5 BBSY13	5 BBSY05
4 BBSY28	4 BBSY20	4 BBSY12	4 BBSY04
3 BBSY27	3 BBSY19	3 BBSY11	3 BBSY03
2 BBSY26	2 BBSY18	2 BBSY10	2 BBSY02
1 BBSY25	1 BBSY17	1 BBSY09	1 BBSY01
0 BBSY24	0 BBSY16	0 BBSY08	0 BBSY00

SXFRCTL2	SCSITEST	FRQSYNCTL1	FRQSYNCTL0
R/W M/DS -13h	R M/DS -12h	RM/DS - 11h	RM/DS -10h
7 RSVD	7 DISABEXT66	7 FRQSYN_SELPLL	7 EXT_CLK_PRSNT
6 RSVD	6 SELEXT80	6 FRQSYN_VCOD	6 FRQSYN_EN
5 RSVD	5 RSVD	5 FRQSYN_BCNT5	5 FRQSYN_FCNT5
4 AUTORSTDIS	4 BOOSTDISAB	4 FRQSYN_BCNT4	4 FRQSYN_FCNT4
3 CMDDMAEN	3 CNTRTEST	3 FRQSYN_BCNT3	3 FRQSYN_FCNT3
2 ASU2	2 DATALOOPEN	2 FRQSYN_BCNT2	2 FRQSYN_FCNT2
1 ASU1	1 RSVD	1 FRQSYN_BCNT1	1 FRQSYN_FCNT1
0 ASU0	0 RSVD	0 FRQSYN_BCNT0	0 FRQSYN_FCNT0

SFUNCT	SEQDBCTL	IOPDNCTL
R/W M/DS-9Fh	R/W M/DS-60h	R/W M/DS-14h
7 ALT_MODE	7 RSVD	7 RSVD
6 GROUP3	6 RSVD	6 RSVD
5 GROUP2	5 RSVD	5 RSVD
4 GROUP1	4 RSVD	4 PDN_LBGDMTL
3 GROUP0	3 RSVD	3 PDN_VTBIAS
2 TEST2	2 RSVD	2 PDN_IDIST
1 TEST1	1 RAMBIST_FAIL	1 PDN_BIAS1
0 TEST0	0 RAMBIST_EN	0 PDN_DIFFSENSE

PF_REQGNTCYCCNT3	PF_REQGNTCYCCNT2	PF_REQGNTCYCCNT1	PF_REQGNTCYCCNT0
R M/DS -A3h	R M/DS -A2h	R M/DS -A1h	R M/DS -A0h
7 PF_REQGNTCYCCNT31	7 PF_REQGNTCYCCNT23	7 PF_REQGNTCYCCNT15	7 PF_REQGNTCYCCNT07
6 PF_REQGNTCYCCNT30	6 PF_REQGNTCYCCNT22	6 PF_REQGNTCYCCNT14	6 PF_REQGNTCYCCNT06
5 PF_REQGNTCYCCNT29	5 PF_REQGNTCYCCNT21	5 PF_REQGNTCYCCNT13	5 PF_REQGNTCYCCNT05
4 PF_REQGNTCYCCNT28	4 PF_REQGNTCYCCNT20	4 PF_REQGNTCYCCNT12	4 PF_REQGNTCYCCNT04
3 PF_REQGNTCYCCNT27	3 PF_REQGNTCYCCNT19	3 PF_REQGNTCYCCNT11	3 PF_REQGNTCYCCNT03
2 PF_REQGNTCYCCNT26	2 PF_REQGNTCYCCNT18	2 PF_REQGNTCYCCNT10	2 PF_REQGNTCYCCNT02
1 PF_REQGNTCYCCNT25	1 PF_REQGNTCYCCNT17	1 PF_REQGNTCYCCNT09	1 PF_REQGNTCYCCNT01
0 PF_REQGNTCYCCNT24	0 PF_REQGNTCYCCNT16	0 PF_REQGNTCYCCNT08	0 PF_REQGNTCYCCNT00

PFRD_BURSTCNT3	PFRD_BURSTCNT2	PFRD_BURSTCNT1	PFRD_BURSTCNT0
RM/DS -A7h	R M/DS -A6h	RM/DS -A5h	RM/DS -A4h
7 PFRD_BURSTCNT31	7 PFRD_BURSTCNT23	7 PFRD_BURSTCNT15	7 PFRD_BURSTCNT07
6 PFRD_BURSTCNT30	6 PFRD_BURSTCNT22	6 PFRD_BURSTCNT14	6 PFRD_BURSTCNT06
5 PFRD_BURSTCNT29	5 PFRD_BURSTCNT21	5 PFRD_BURSTCNT13	5 PFRD_BURSTCNT05
4 PFRD_BURSTCNT28	4 PFRD_BURSTCNT20	4 PFRD_BURSTCNT12	4 PFRD_BURSTCNT04
3 PFRD_BURSTCNT27	3 PFRD_BURSTCNT19	3 PFRD_BURSTCNT11	3 PFRD_BURSTCNT03
2 PFRD_BURSTCNT26	2 PFRD_BURSTCNT18	2 PFRD_BURSTCNT10	2 PFRD_BURSTCNT02
1 PFRD_BURSTCNT25	1 PFRD_BURSTCNT17	1 PFRD_BURSTCNT09	1 PFRD_BURSTCNT01
0 PFRD_BURSTCNT24	0 PFRD_BURSTCNT16	0 PFRD_BURSTCNT08	0 PFRD_BURSTCNT00

PFRD_DWXFRCNT3	PFRD_DWXFRCNT2	PFRD_DWXFRCNT1	PFRD_DWXFRCNT0
RM/DS -ABh	RM/DS -AAh	RM/DS -A9h	RM/DS -A8h
7 PFRD_DWXFRCNT31	7 PFRD_DWXFRCNT23	7 PFRD_DWXFRCNT15	7 PFRD_DWXFRCNT07
6 PFRD_DWXFRCNT30	6 PFRD_DWXFRCNT22	6 PFRD_DWXFRCNT14	6 PFRD_DWXFRCNT06
5 PFRD_DWXFRCNT29	5 PFRD_DWXFRCNT21	5 PFRD_DWXFRCNT13	5 PFRD_DWXFRCNT05
4 PFRD_DWXFRCNT28	4 PFRD_DWXFRCNT20	4 PFRD_DWXFRCNT12	4 PFRD_DWXFRCNT04
3 PFRD_DWXFRCNT27	3 PFRD_DWXFRCNT19	3 PFRD_DWXFRCNT11	3 PFRD_DWXFRCNT03
2 PFRD_DWXFRCNT26	2 PFRD_DWXFRCNT18	2 PFRD_DWXFRCNT10	2 PFRD_DWXFRCNT02
1 PFRD_DWXFRCNT25	1 PFRD_DWXFRCNT17	1 PFRD_DWXFRCNT09	1 PFRD_DWXFRCNT01
0 PFRD_DWXFRCNT24	0 PFRD_DWXFRCNT16	0 PFRD_DWXFRCNT08	0 PFRD_DWXFRCNT00

PFRD_PREQCNT3	PFRD_PREQCNT2	PFRD_PREQCNT1	PFRD_PREQCNT0
RM/DS -AFh	RM/DS -AEh	RM/DS -ADh	RM/DS -ACh
7 PFRD_PREQCNT31	7 PFRD_PREQCNT23	7 PFRD_PREQCNT15	7 PFRD_PREQCNT07
6 PFRD_PREQCNT30	6 PFRD_PREQCNT22	6 PFRD_PREQCNT14	6 PFRD_PREQCNT06
5 PFRD_PREQCNT29	5 PFRD_PREQCNT21	5 PFRD_PREQCNT13	5 PFRD_PREQCNT05
4 PFRD_PREQCNT28	4 PFRD_PREQCNT20	4 PFRD_PREQCNT12	4 PFRD_PREQCNT04
3 PFRD_PREQCNT27	3 PFRD_PREQCNT19	3 PFRD_PREQCNT11	3 PFRD_PREQCNT03
2 PFRD_PREQCNT26	2 PFRD_PREQCNT18	2 PFRD_PREQCNT10	2 PFRD_PREQCNT02
1 PFRD_PREQCNT25	1 PFRD_PREQCNT17	1 PFRD_PREQCNT09	1 PFRD_PREQCNT01
0 PFRD_PREQCNT24	0 PFRD_PREQCNT16	0 PFRD_PREQCNT08	0 PFRD_PREQCNT00

RSVD	RSVD	PFRD_MAXBURSTLEN1	PFRD_MAXBURSTLEN0
R M/DS -B3h	R M/DS -B2h	R M/DS -B1h	R M/DS -B0h
7 RSVD	7 RSVD	7 PFRD_MAXBURSTLEN15	7 PFRD_MAXBURSTLEN07
6 RSVD	6 RSVD	6 PFRD_MAXBURSTLEN14	6 PFRD_MAXBURSTLEN06
5 RSVD	5 RSVD	5 PFRD_MAXBURSTLEN13	5 PFRD_MAXBURSTLEN05
4 RSVD	4 RSVD	4 PFRD_MAXBURSTLEN12	4 PFRD_MAXBURSTLEN04
3 RSVD	3 RSVD	3 PFRD_MAXBURSTLEN11	3 PFRD_MAXBURSTLEN03
2 RSVD	2 RSVD	2 PFRD_MAXBURSTLEN10	2 PFRD_MAXBURSTLEN02
1 RSVD	1 RSVD	1 PFRD_MAXBURSTLEN09	1 PFRD_MAXBURSTLEN01
0 RSVD	0 RSVD	0 PFRD_MAXBURSTLEN08	0 PFRD_MAXBURSTLEN00

PFWR_BURSTCNT3	PFWR_BURSTCNT2	PFWR_BURSTCNT1	PFWR_BURSTCNT0
RM/DS -B7h	RM/DS -B6h	RM/DS -B5h	RM/DS -B4h
7 PFWR_BURSTCNT31	7 PFWR_BURSTCNT23	7 PFWR_BURSTCNT15	7 PFWR_BURSTCNT07
6 PFWR_BURSTCNT30	6 PFWR_BURSTCNT22	6 PFWR_BURSTCNT14	6 PFWR_BURSTCNT06
5 PFWR_BURSTCNT29	5 PFWR_BURSTCNT21	5 PFWR_BURSTCNT13	5 PFWR_BURSTCNT05
4 PFWR_BURSTCNT28	4 PFWR_BURSTCNT20	4 PFWR_BURSTCNT12	4 PFWR_BURSTCNT04
3 PFWR_BURSTCNT27	3 PFWR_BURSTCNT19	3 PFWR_BURSTCNT11	3 PFWR_BURSTCNT03
2 PFWR_BURSTCNT26	2 PFWR_BURSTCNT18	2 PFWR_BURSTCNT10	2 PFWR_BURSTCNT02
1 PFWR_BURSTCNT25	1 PFWR_BURSTCNT17	1 PFWR_BURSTCNT09	1 PFWR_BURSTCNT01
0 PFWR_BURSTCNT24	0 PFWR_BURSTCNT16	0 PFWR_BURSTCNT08	0 PFWR_BURSTCNT00

PFWR_DWXFRCNT3	PFWR_DWXFRCNT2	PFWR_DWXFRCNT1	PFWR_DWXFRCNT0
RM/DS -BBh	RM/DS -BAh	RM/DS -B9h	RM/DS -B8h
7 PFWR_DWXFRCNT31	7 PFWR_DWXFRCNT23	7 PFWR_DWXFRCNT15	7 PFWR_DWXFRCNT07
6 PFWR_DWXFRCNT30	6 PFWR_DWXFRCNT22	6 PFWR_DWXFRCNT14	6 PFWR_DWXFRCNT06
5 PFWR_DWXFRCNT29	5 PFWR_DWXFRCNT21	5 PFWR_DWXFRCNT13	5 PFWR_DWXFRCNT05
4 PFWR_DWXFRCNT28	4 PFWR_DWXFRCNT20	4 PFWR_DWXFRCNT12	4 PFWR_DWXFRCNT04
3 PFWR_DWXFRCNT27	3 PFWR_DWXFRCNT19	3 PFWR_DWXFRCNT11	3 PFWR_DWXFRCNT03
2 PFWR_DWXFRCNT26	2 PFWR_DWXFRCNT18	2 PFWR_DWXFRCNT10	2 PFWR_DWXFRCNT02
1 PFWR_DWXFRCNT25	1 PFWR_DWXFRCNT17	1 PFWR_DWXFRCNT09	1 PFWR_DWXFRCNT01
0 PFWR_DWXFRCNT24	0 PFWR_DWXFRCNT16	0 PFWR_DWXFRCNT08	0 PFWR_DWXFRCNT00

PFWR_PREQCNT3	PFWR_PREQCNT2	PFWR_PREQCNT1	PFWR_PREQCNT0
RM/DS -BFh	RM/DS -BEh	RM/DS -BDh	RM/DS -BCh
7 PFWR_PREQCNT31	7 PFWR_PREQCNT23	7 PFWR_PREQCNT15	7 PFWR_PREQCNT07
6 PFWR_PREQCNT30	6 PFWR_PREQCNT22	6 PFWR_PREQCNT14	6 PFWR_PREQCNT06
5 PFWR_PREQCNT29	5 PFWR_PREQCNT21	5 PFWR_PREQCNT13	5 PFWR_PREQCNT05
4 PFWR_PREQCNT28	4 PFWR_PREQCNT20	4 PFWR_PREQCNT12	4 PFWR_PREQCNT04
3 PFWR_PREQCNT27	3 PFWR_PREQCNT19	3 PFWR_PREQCNT11	3 PFWR_PREQCNT03
2 PFWR_PREQCNT26	2 PFWR_PREQCNT18	2 PFWR_PREQCNT10	2 PFWR_PREQCNT02
1 PFWR_PREQCNT25	1 PFWR_PREQCNT17	1 PFWR_PREQCNT09	1 PFWR_PREQCNT01
0 PFWR_PREQCNT24	0 PFWR_PREQCNT16	0 PFWR_PREQCNT08	0 PFWR_PREQCNT00

PF_CNTRL	RSVD	PFWR_MAXBURSTLEN1	PFWR_MAXBURSTLEN0
R/W M/DS -DFh	R M/DS- C2h to DEh	R M/DS-C1h	R M/DS -C0h
7 RSVD	RSVD	7 PFWR_MAXBURSTLEN15	7 PFWR_MAXBURSTLEN07
6 RSVD	RSVD	6 PFWR_MAXBURSTLEN14	6 PFWR_MAXBURSTLEN06
5 RSVD	RSVD	5 PFWR_MAXBURSTLEN13	5 PFWR_MAXBURSTLEN05
4 RSVD	RSVD	4 PFWR_MAXBURSTLEN12	4 PFWR_MAXBURSTLEN04
3 RSVD	RSVD	3 PFWR_MAXBURSTLEN11	3 PFWR_MAXBURSTLEN03
2 RSVD	RSVD	2 PFWR_MAXBURSTLEN10	2 PFWR_MAXBURSTLEN02
1 RSVD	RSVD	1 PFWR_MAXBURSTLEN09	1 PFWR_MAXBURSTLEN01
0 PFREG_ENABLE	RSVD	0 PFWR_MAXBURSTLEN08	0 PFWR_MAXBURSTLEN00

DFDBCTL	DFBKPTR1	DFBKPTR0	DFPTRS
R/WM/DS E3h	R/WM/DS E2h	R/WM/DS E1h	R/WM/DS E0h
7 RSVD	7 RSVD	7 RSVD	7 RSVD
6 RSVD	6 DFBKPTR09	6 RSVD	6 RSVD
5 RSVD	5 DFBKPTR08	5 RSVD	5 DFRPTR02
4 DFF_CIO_WR_RDY	4 DFBKPTR07	4 RSVD	4 DFRPTR01
3 DFF_CIO_RD_RDY	3 DFBKPTR06	3 RSVD	3 DFRPTR00
2 DFF_DIR_ERR	2 DFBKPTR05	2 DFBKPTR02	2 DFWPTR02
1 DFF_RAMBIST_FAIL	1 DFBKPTR04	1 DFBKPTR01	1 DFWPTR01
0 DFF_RAMBIST_EN	0 DFBKPTR03	0 DFBKPTR00	0 DFWPTR00

DFBCNT1	DFBCNT0	DFSCNT1	DFSCNT0
RM/DS E7h	RM/DS E6h	RM/DS E5h	RM/DS E4h
7 RSVD	7 DFBCNT07	7 RSVD	7 DFSCNT07
6 RSVD	6 DFBCNT06	6 RSVD	6 DFSCNT06
5 RSVD	5 DFBCNT05	5 RSVD	5 DFSCNT04
4 RSVD	4 DFBCNT04	4 RSVD	4 DFSCNT04
3 RSVD	3 DFBCNT03	3 RSVD	3 DFSCNT03
2 RSVD	2 DFBCNT02	2 RSVD	2 DFSCNT02
1 DFBCNT09	1 DFBCNT01	1 DFSCNT09	1 DFSCNT01
0 DFBCNT08	0 DFBCNT00	0 DFSCNT08	0 DFSCNT00

CCSCBADR_BK
R/WM/DS EDh
7 CCSCBADR_BK7
6 CCSCBADR_BK6
5 CCSCBADR_BK5
4 CCSCBADR_BK4
3 CCSCBADR_BK3
2 CCSCBADR_BK2
1 CCSCBADR_BK1
0 CCSCBADR_BK0

Register Definitions

The following conventions are used throughout this section

set - Indicates that the bit was loaded with a 1

cleared - Indicates that the bit was loaded with a 0

(0) - Indicates that the bit is cleared when the PCIRST# pin is active

(1) - Indicates that the bit is set when the PCIRST# pin is active

(x) - Indicates that the bit is in an unknown state after the reset condition

R - The register is read-only.

W - The register is write-only.

R/W - The register is readable and writable.

(r) - Bit(s) is read-only.

(w) - Bit(s) is write-only.

(r/w) -Bit(s) is readable or writable.

RSVD - Reserved bit(s) in registers. Always returns zero when read. No other values (other than zero) should be written to this bit(s).

Not used - Undefined bit(s) in registers when written.

PCI Configuration Registers

Vendor Identification (VENDOR_ID)

Type:R
Address:N-00h

The PCI vendor identification registers contain product information for use by the host in initialization and configuration of the system. The vendor ID contains two bytes of a compressed bit representation (9005h) of the vendor ID. In revision 0 chips, VENDOR_ID[15:0] can be changed by strapping both TESTMODE# and PDPUDIS# pins to high, allowing SUBVENDOR_ID[15:0] to be copied to VENDOR_ID[15:0] after IDDAT values are shifted in. In other revisions of the chip, this feature is not provided. VENDOR_ID may be read at any time in Configuration space.

VENDOR_ID R			
15	VENDOR_ID15	07	VENDOR_ID07
14	VENDOR_ID14	06	VENDOR_ID06
13	VENDOR_ID13	05	VENDOR_ID05
12	VENDOR_ID12	04	VENDOR_ID04
11	VENDOR_ID11	03	VENDOR_ID03
10	VENDOR_ID10	02	VENDOR_ID02
09	VENDOR_ID09	01	VENDOR_ID01
08	VENDOR_ID08	00	VENDOR_ID00

Bit			Name	Definition
15	(1)	(r)	VENDOR_ID15	Always reads 1, 2nd vendor ID character
14	(0)	(r)	VENDOR_ID14	Always reads 0, 2nd vendor ID character
13	(0)	(r)	VENDOR_ID13	Always reads 0, 2nd vendor ID character LSB.
12	(1)	(r)	VENDOR_ID12	Always reads 1, 3rd vendor ID character
11	(0)	(r)	VENDOR_ID11	Always reads 0, 3rd vendor ID character
10	(0)	(r)	VENDOR_ID10	Always reads 0, 3rd vendor ID character
09	(0)	(r)	VENDOR_ID09	Always reads 0, 3rd vendor ID character.
08	(0)	(r)	VENDOR_ID08	Always reads 0, 3rd vendor ID character LSB.
07	(0)	(r)	VENDOR_ID07	Always reads 0, (fill bit).
06	(0)	(r)	VENDOR_ID06	Always reads 0, 1st vendor ID character MSB.
05	(0)	(r)	VENDOR_ID05	Always reads 0, 1st vendor ID character.
04	(0)	(r)	VENDOR_ID04	Always reads 0, 1st vendor ID character.
03	(0)	(r)	VENDOR_ID03	Always reads 0, 1st vendor ID character.
02	(1)	(r)	VENDOR_ID02	Always reads 1, 1st vendor ID character LSB.
01	(0)	(r)	VENDOR_ID01	Always reads 0, 2nd vendor ID character MSB.
00	(1)	(r)	VENDOR_ID00	Always reads 1, 2nd vendor ID character.

Device Identification (DEVICE_ID)

Type:R/W
Address:N-02h

The PCI device identification registers contain product information for use by the host in initialization and configuration of the system. The two device ID bytes contain an Adaptec product code. The product code for the AIC-7890A/91 is 001Fh. The last nibble (4 bits) can be changed by strapping both TESTMODE# and PDPUDIS# pins to high, allowing the lower nibble of SUBSYSTEM_ID[3:0] to be copied to DEVICE_ID[3:0]. DEVICE_ID may be read at any time in Configuration space. If the ID Write Enable (IDWEN) bit is set in the IDENREG register, the DEVICE_ID register is writeable and readable. If the IDWEN bit is cleared, the DEVICE_ID register is read-only. In revision 0 chips (DEVREV_ID = 00h), this register is read-only.

DEVICE_ID R/W			
15	DEVICE_ID15	07	DEVICE_ID07
14	DEVICE-ID14	06	DEVICE_ID06
13	DEVICE_ID13	05	DEVICE_ID05
12	DEVICE_ID12	04	DEVICE_ID04
11	DEVICE_ID11	03	DEVICE_ID03
10	DEVICE_ID10	02	DEVICE_ID02
09	DEVICE_ID09	01	DEVICE_ID01
08	DEVICE_ID08	00	DEVICE_ID00

Bit			Name	Definition
15	(0)	(r)	DEVICE_ID15	Normally reads 0, 4th device ID character MSB.
14	(0)	(r)	DEVICE_ID14	Normally reads 0, 4th device ID character.
13	(0)	(r)	DEVICE_ID13	Normally reads 0, 4th device ID character.
12	(0)	(r)	DEVICE_ID12	Normally reads 0, 4th device ID character LSB.
11	(0)	(r)	DEVICE-ID11	Normally reads 0, 3rd device ID character MSB.
10	(0)	(r)	DEVICE_ID10	Normally reads 0, 3rd device ID character.
09	(0)	(r)	DEVICE_ID09	Normally reads 0, 3rd device ID character.
08	(0)	(r)	DEVICE-ID08	Normally reads 0, 3rd device ID character LSB.
07	(0)	(r)	DEVICE_ID07	Normally reads 0, 2nd device ID character MSB.
06	(0)	(r)	DEVICE_ID06	Normally reads 0, 2nd device ID character.
05	(0)	(r)	DEVICE_ID05	Normally reads 0, 2nd device ID character.
04	(1)	(r)	DEVICE_ID04	Normally reads 1, 2nd device ID character LSB.
03	(1)	(r)	DEVICE_ID03	Normally reads 1, 1st device ID character MSB.
02	(1)	(r)	DEVICE_ID02	Normally reads 1, 1st device ID character.
01	(1)	(r)	DEVICE_ID01	Normally reads 1, 1st device ID character.
00	(1)	(r)	DEVICE_ID00	Normally reads 1, 1st device ID character LSB.

Command (COMMAND)

Type:R/W
Address: N-04h

The COMMAND register provides coarse control over a PCI device's ability to generate and respond to PCI transactions. When MSPACEEN and ISPACEEN bits are cleared in this register, the AIC-7890A/91 is logically disconnected from the PCI bus transactions except for Configuration Space transactions. The COMMAND register may be read or written at any time in Configuration Space.

COMMAND R/W			
15	RSVD	07	WAITCTLEN=0
14	RSVD	06	PERRESPEN
13	RSVD	05	VSNOOPEN=0
12	RSVD	04	MWRICEN
11	RSVD	03	SPCYCEN=0
10	RSVD	02	MASTEREN
09	MFBFEN=0	01	MSPACEEN
08	SERRESPEN	00	ISPACEEN

Bit			Name	Definition
15-10	(0)	(r)	RSVD	Always reads 0.
09	(0)	(r)	MFBFEN	**Master Fast Back-to-back Enable.** When active (=1), indicates a master can perform Fast Back-to-back transactions to different PCI targets. The AIC-7890A/91 does not support this feature and MFBFEN always reads as 0.
08	(0)	(r/w)	SERRESPEN	**System Error Response Enable.** When active (=1) and PERRESPEN is also active, SERR# is asserted when a PCI even parity error is detected by the AIC-7890A/91 as a PCI target during the address phase(s) of transactions. The AIC-7890A/91 only asserts SERR# for detected address parity errors as a target and does not assert SERR# as a master.
07	(0)	(r)	WAITCTLEN	**Wait Control Enable.** Always reads 0. (May only be set to one by those devices that do not meet the PCI output specification of 33-10.) The AIC-7890A/91 does not support WAITCLTEN.
06	(0)	(r/w)	PERRESPEN	**Parity Error Response Enable.** When active (=1), enables PERR# to be asserted when a PCI even parity error is detected during Data phases of transactions, except for Special Cycle Transaction Data phase. PERRESPEN must also be active for an address parity error to be reported on SERR#. The AIC-7890A/91 will assert PERR# when PERRESPEN is active and a data parity error is detected as a target for write accesses or as an master for read accesses. PERRESPEN must also be active to allow DPE or DPR active conditions to cause IRQA# (when enabled) to be asserted.

Bit			Name	Definition
05	(0)	(r)	VSNOOPEN	**VGA Snoop Enable.** Always reads 0. The AIC-7890A/91 does not support VSNOOPEN.
04	(0)	(r/w)	MWRICEN	**Memory Write and Invalidate Enable.** When active (=1), enables a PCI master to issue Memory Write and Invalidate commands to more optimally transfer data to system memory. When inactive, the Memory Write and Invalidate command will be replaced with a Memory Write command. The AIC-7890A/91 as a master will issue MWRIC commands for the data channel when MWRICEN is active, the data FIFO contains stored data or space to store data that is equal to or greater than the selected cache size (not zero), the address is on the cache line start location, and the HCNT value is also equal to or greater than the selected cache size. The AIC-7890A/91 as a master will issue MWRIC commands for the command channel when MWRICEN is active, the Command channel RAM contains stored data or space to store data that is equal to or greater than the selected cache size (not zero), the address is on the cache line start location, and the CCHCNT value is also equal to or greater than the selected cache size.
03	(0)	(r)	SPCYCEN	**Special Cycle Enable.** Always reads 0. When active (=1), allows a target to monitor special cycle transactions broadcast on the PCI bus. The AIC-7890A/91 does not support special cycles as a target or master.
02	(0)	(r/w)	MASTEREN	**Master Enable.** When active (=1), enables the AIC-7890A/91 to perform bus master transactions on the PCI bus. AIC-7890A/91 device registers must be configured correctly before the AIC-7890A/91 generates a request to become a bus master. When inactive, the AIC-7890A/91 bus master transactions are inhibited.
01	(0)	(r/w)	MSPACEEN	**Memory Space Enable.** When active (=1), enables the AIC-7890A/91 to respond to Device register transactions through mapped memory space (see BASEADR1 register) or external ROM transaction through mapped memory space (see EXROMBADR register). When MSPACEEN is inactive, the AIC-7890A/91 will not respond to device space accesses from memory mapped addresses.
00	(0)	(r/w)	ISPACEEN	**I/O Space Enable.** When active (=1), enables the AIC-7890A/91 to respond to device register transactions through mapped I/O space (see BASEADR0 register). When inactive, the AIC-7890A/91 will not respond to device space accesses from I/O mapped addresses.

Status (STATUS)

Type:R/W
Address:N-06h

The STATUS register is used to record status information for PCI bus related events. Read transactions of the STATUS register will access the currently stored status information. Write transactions to the STATUS register are not used to store data but to change selected active bits to be inactive (=0). To change a bit to be inactive, the data value written for that bit (=1) with all other bits not being changed inactive (=0). Whenever DPE, SSE, RMA, RTA, STA or DPR is active in STATUS, it will cause the PCIERRSTAT bit in the ERROR register to be set and an interrupt to be generated unless FAILDIS or POWRDN is active, or INTEN is inactive. The STATUS register is cleared when PCIRST# is asserted. The STATUS register may be read or written at any time in Configuration space.

STATUS R/W			
15	DPE	07	TFBTBC
14	SSE	06	UDF
13	RMA	05	66MHZ
12	RTA	04	CAP_LIST
11	STA	03	RSVD
10	DST1	02	RSVD
09	DST0	01	RSVD
08	DPR	00	RSVD

Bit			Name	Definition
15	(0)	(r/w)	DPE	**Detected Parity Error.** Set active (=1) when an even-parity error is detected by a target during an Address phase or a Write Data phase (except for Special Cycles) and by the transaction master during a Read Data phase. DPE is set inactive during and after assertion of PCIRST# or by a write to the STATUS register with bit 15 set (=1). When the AIC-7890A/91 sets its DPE bit active with PERRESPEN and INTEN active and FAILDIS inactive, it will cause an interrupt to be generated to the host to handle the exception condition. PERR# will also be asserted. Parity is monitored by the AIC-7890A/91 during PCI Write transactions (when the AIC-7890A/91 is a target) and PCI Read transactions (when the AIC-7890A/91 is a master.)
14	(0)	(r/w)	SSE	**Signal System Error.** Set active (=1) whenever an agent asserts SERR#. SSE is set inactive during and after assertion of PCIRST# or by a write to the STATUS register with bit 14 set (=1). The AIC-7890A/91 sets its SSE bit active only when PERRESPEN and SERRESPEN are active for detected address parity errors. When SSE is active and FAILDIS is inactive and INTEN is active, it will cause an interrupt to be generated to the host to handle the exception condition.

Bit			Name	Definition
13	(0)	(r/w)	RMA	**Received Master Abort.** Set active (=1) when an AIC-7890A/91 bus master generated transaction is terminated by the AIC-7890A/91 for no response from the intended target by the sixth (for SAC) or seventh (for DAC) PCLK after the AIC-7890A/91 asserted FRAME#. The AIC-7890A/91 will release the bus on the next PCLK and will not retry the transaction. Software/firmware intervention is required for the AIC-7890A/91 to continue further master transactions. RMA is set inactive during and after assertion of PCIRST# or by a write to the STATUS register with bit 13 set (=1). The AIC-7890A/91 will also set RMA active should the addressed target deassert DEVSEL# while the AIC-7890A/91 is asserting FRAME#, a PCI protocol violation. **Note:** If RMA is cleared with the aborted master transaction still waiting to complete, the AIC-7890A/91 will retry the transaction. To prevent this action, if desired, clear HDMAEN data channel, and CCSGEN and CCSBCEN of command channel before clearing RMA.The interrupt will remain active till cleared with CLRPARERR.
12	(0)	(r/w)	RTA	**Received Target Abort.** Set active (=1) when the target of an AIC-7890A/91 bus generated transaction is terminated by the target, with a target-abort indication. RTA is set inactive during and after assertion of PCIRST# or by a write to the STATUS register with bit 12 set (=1). When a target-abort indication is received, the AIC-7890A/91 will not retry the transaction, and software/firmware intervention is required for the AIC-7890A/91 to continue further master transactions. **Note:** If RTA is cleared with the AIC-7890A/91 still waiting to complete the aborted master transaction, the AIC-7890A/91 will retry the transaction. To prevent this action, if desired, clear HDMAEN before clearing RTA for data channel errors and/or clear bits CCSGEN or CCSCBEN for command channel errors.The interrupt will remain active till cleared with CLRPARERR.
11	(0)	(r/w)	STA	**Signal Target Abort.** Set active (=1) by the target of a PCI bus transaction unable to respond due to a fatal error condition. STA is cleared during and after assertion of PCIRST# or by a write to the STATUS register with bit 11 set (=1). The AIC-7890A/91 will indicate target-abort for:

Bit			Name	Definition
				■ Incorrect data width — must be 8 bits for Device space — must be 8 bits for ROM space write ■ Value stored in base address registers for BASEADR1 and EXROMBADR are the same and EXROMEN is active. ■ SEEMS is active and an access is made to external SCB RAM space address. ■ Accesses with POWRDN active except for Host only registers and Configuration registers. ■ Address parity error detected (SSE = 1)with correct address compare (SERR# asserted) for current access. ■ Accessing AIC-7890A/91's Device space registers while Sequencer is not paused. **Note**: No valid data (no CBE is asserted for a Data phase) is not an error condition.
10-09	(1)	(r)	DST[1:0]	**Device Select Timing[1:0].** Value indicates the longest response time of a PCI device for assertion of DEVSEL# for any bus transaction with valid values of 0h for *fast* (1 PCLK), 1h for *medium* (2 PCLKs), 2h for *slow* (3 PCLKs) with value 3h *reserved*. Respond time for the AIC-7890A/91 is *medium*. DST[1:0] are fixed value read only bits.
08	(0)	(r/w)	DPR	**Data Parity Reported.** When active (=1), indicates the master of a transaction, with its PERRESPEN bit active, has detected PERR# asserted or asserted PERR#. DPR is set inactive during and after assertion of PCIRST# or by a write to the STATUS register with bit 8 set (=1).
07	(1)	(r)	TFBTBC	**Target Fast Back-to-back Capable.** When active (=1), indicates that the target is capable of accepting Fast PCI Back-to-back transactions even when the transactions are not to the same target. The AIC-7890A/91 as a target supports Fast Back-to-back transactions. TFBTBC is a read only bit.
06	(0)	(r)	UDF	Always reads 0.
05	(0)	(r)	66MHZ	Always reads 0.
04	(1)	(r)	CAP_LIST	When set to 1, indicates that the AIC-7890A/91 is capable of Power Management functions.
03-00	(0)	(r)	RSVD	Always reads 0.

Device Revision ID (DEVREV_ID)

Type:R
Address:N-08h

The Device Revision ID identifies the revision level of a PCI device. DEVREV_ID may be read at any time in Configuration space.

DEVREV_ID R	
07	DEVREV_ID7
06	DEVREV_ID6
05	DEVREV_ID5
04	DEVREV_ID4
03	DEVREV_ID3
02	DEVREV_ID2
01	DEVREV_ID1
00	DEVREV_ID0

Bit			Name	Definition
07-00	(0)	(r)	DEVREV_ID[7:0]	Reflects the revision ID of the AIC-7890A/91. The first part will read as 0 and subsequent revisions to the part will reflect with an increment by 1.

Programming Interface (PROGINFC)

Type:R
Address:N-09h

The Programming Interface register value identifies the specific register-level programming interface the agent supports. The PROGINFC for the first version of the AIC-7890A/91 will be identified as 00h (not VGA compatible). PROGINFC may be read at any time in Configuration space.

PROGINFC R	
07	PINFC7
06	PINFC6
05	PINFC5
04	PINFC4
03	PINFC3
02	PINFC2
01	PINFC1
00	PINFC0

Bit			Name	Definition
07-00	(0)	(r)	PINFC[7:0]	Always reads 0.

Sub Class (SUBCLASS)

Type:R
Address:N-0Ah

The Sub Class register identifies the sub class of the AIC-7890A/91 is assigned to. The SUBCLASS for the first version of the AIC-7890A/91 will be identified as 00h (SCSI bus controller). SUBCLASS may be read at any time in Configuration space.

SUBCLASS R	
07	SCLASS7
06	SCLASS6
05	SCLASS5
04	SCLASS4
03	SCLASS3
02	SCLASS2
01	SCLASS1
00	SCLASS0

Bit			Name	Definition
07-00	(0)	(r)	SCLASS[7:0]	Always reads 0.

Base Class (BASECLASS)

Type:R
Address:N-0Bh

The Base Class register identifies the base class that the AIC-7890A/91 has been assigned to. The BASECLASS for the first version of the AIC-7890A/91 will be identified as 01h (mass storage controller). BASECLASS may be read at any time in Configuration space.

BASECLASS R	
07	BCLASS7
06	BCLASS6
05	BCLASS5
04	BCLASS4
03	BCLASS3
02	BCLASS2
01	BCLASS1
00	BCLASS0

Bit			Name	Definition
07-00	(01h)	(r)	BCLASS[7:0]	Always reads 01h to be identified as mass storage controller.

Cache Line Size (CACHESIZE)

Type:R/W
Address:N-0Ch

The Cache Line Size register specifies the system cache line size in units of 32-bit Double-WorD(DWD). The value stored in the register defines the minimum data transfer size and associated cache starting boundary (and multiples thereof) that may be performed with cache line referenced PCI MWRIC, MRDLC or MRDMC commands.

The AIC-7890A/91 initiated cache line transactions can last indefinitely as long as GNT# remains asserted, provided that data or space for data that is being transferred and its transfer byte count has not expired. However, if GNT# is deasserted after the cache line transfer is initiated, the AIC-7890A/91 further limits the duration of the cache line transfer to the number of clocks specified by the LAT_TIME register, plus completion of an in-process cache line transfer referenced command. When the stored value in the CASHESIZE register is 0h, the AIC-7890A/91 will issue MWRC or MRDC only instead of MWRIC, MRDLC or MRDMC for data transfer.

Note the effect of MRDCEN active state on command issued and stopping point. CACHESIZE register may be read or written at any time in Configuration space. CDWDSIZE are reset to 0h during assertion of PCIRST#.

CACHESIZE R/W	
07	CDWDSIZE7
06	CDWDSIZE6
05	CDWDSIZE5
04	CDWDSIZE4
03	CDWDSIZE3
02	CDWDSIZE2
01	CDWDSIZE1
00	CDWDSIZE0

Bit			Name	Definition
07-00	(0)	(r/w)	CDWDSIZE[7:0]	**Cache Double Word Size [7:0]**. Define the cache line size that the AIC-7890A/91 as a master supports. Note that CDWDSIZE[1:0] always reads 0.

Cachesize Value [7:0]	Action
03h-00h	Use of MWRIC, (MRDLC and MRDMC) are disabled and replaced with MWRC or MRDC respectively.
07h-04h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 4 DWDs (16 Bytes).
0Fh-08h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 8 DWDs (32 Bytes).

Bit	Name	Definition	
		1Fh-10 h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 16 DWDs (64 Bytes).
		2Fh-20h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 32 DWDs (128 Bytes).
		4Fh-40h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 64 DWDs (256 Bytes).
		8Fh-80h	MWRIC, MRDLC and MRDMC use is enabled with a cache line size of 128 DWDs (512 Bytes).

Latency Timer (LAT_TIME)

Type:R/W
Address:N-0Dh

The AIC-7890A/91's master latency timer is held initialized until the AIC-7890A/91 asserts **FRAME#**, then it is enabled to count **PCLKs**. Whenever **FRAME#** is deasserted, the **LAT_TIME** timer is re-initialized. When the AIC-7890A/91's latency timer expires with **FRAME#** still asserted, then the AIC-7890A/91 will initiate transaction termination as soon as its GNT# is deasserted (unless a Memory Write and Invalidate command was issued and is in a process which must be completed before termination) and the target asserts **TRDY#** on the final Data phase. **LAT_TIME** register may be read or written at any time in Configuration space. The **LAT_TIME** register is cleared to 0h during **PCIRST#** assertion.

LAT_TIME R/W	
07	LAT_TIME7
06	LAT_TIME6
05	LAT_TIME5
04	LAT_TIME4
03	LAT_TIME3
02	LAT_TIME2
01	LAT_TIME1
00	LAT_TIME0

Bit			Name	Definition
07-02	(0)	(r/w)	LAT_TIME[7:2]	Latency Timer [7:2] are read/write and their value determines the AIC-7890A/91's bus master latency timer period (in PCLK periods)
01-00	(0)	(r)	LAT_TIME[1:0]	Latency Timer [1:0] always read 0 (sets granularity at four PCLKs).

Header Type (HDRTYPE)

Type:R
Address:N-0Eh

The Header Type register specifies the PCI Configuration header type the device supports. **HDRTYPE** register may be read at any time in Configuration space. The AIC-7890A/91 supports PCI Configuration header type 00h.

HDRTYPE R	
07	MFDEV
06	HTYPE6
05	HTYPE5
04	HTYPE4
03	HTYPE3
02	HTYPE2
01	HTYPE1
00	HTYPE0

Bit			Name	Definition
07	(0)	(r)	MFDEV	**Multifunction Device Type.** Always reads 0.
06-00	(0)	(r)	HTYPE[6:0]	**Header Type.** Always reads 0.

Built-In-Self-Test (BIST)

Type:R/W
Address:N-0Fh

The BIST register is used to control the Built-In-Self-Test logic in the AIC-7890A/91. This BIST logic can be used to test the Sequencer, Data FIFO and internal SCB array SRAMs. The Built-In-Self-Test register may be read at any time in Configuration space except when the BIST logic is activated (START_BIST = 1). All PCI accesses will be retried until the BIST function is complete (START_BIST = 0).

BIST R/W	
07	BIST_CAPABLE
06	START_BIST
05	RSVD
04	RSVD
03	BIST_CODE3
02	BIST_CODE2
01	BIST_CODE1
00	BIST_CODE0

Bit			Name	Definition
07	(1)	(r)	BIST_CAPABLE	**BIST Capable** This status bit indicates whether AIC-7890A/91 supports BIST from the PCI configuration space access. When active (=1), the PCI access BIST is supported. This bit always reads 1.
06	(0)	(r/w)	START_BIST	**Start BIST.** This bit is used to invoke the BIST logic. When invoked (set to 1), the BIST process will be started and upon completion, this bit will be self-cleared. During the BIST process, all PCI access will be retried. When invoking BIST, it would be preferable to wait for an appropriate time before trying to read BIST status as all PCI cycles are retried.
05-04	(0)	(r)	RSVD	Always reads 0.
03-00	(0)	(r)	BIST_CODE[3:0]	**BIST Error Status Code [3:0].** This 4-bit status shows the BIST completion status code. 0000: Passed XXX1: Sequencer Rambist Failed XX1X: Data FIFO Rambist Failed X1XX: SCB Rambist Failed 1XXX: RSVD These status codes will only be cleared with PCIRST# hardware reset.

Base Address 0 (BASEADR0)

Type:R/W
Address:N-10h

Base Address register 0 enables the AIC-7890A/91 Device register space to be relocated (mapped) within system I/O address space to enable the system board device independent POST software to build a consistent I/O address map. **BASEADR0** may be read at any time in Configuration space. **BASEADR0** value is reset to 01h during **PCIRST#** assertion.

BASEADR0 R/W							
31	IBMADR31	23	IBMADR23	15	IBMADR15	07	IBMADR07
30	IBMADR30	22	IBMADR22	14	IBMADR14	06	IBMADR06
29	IBMADR29	21	IBMADR21	13	IBMADR13	05	IBMADR05
28	IBMADR28	20	IBMADR20	12	IBMADR12	04	IBMADR04
27	IBMADR27	19	IBMADR19	11	IBMADR11	03	IBMADR03
26	IBMADR26	18	IBMADR18	10	IBMADR10	02	IBMADR02
25	IBMADR25	17	IBMADR17	09	IBMADR09	01	RSVD
24	IBMADR24	16	IBMADR16	08	IBMADR08	00	ISPACEIND

Bit			Name	Definition
31-08	(0)	(r/w)	IBMADR[31:08]	**I/O Base Map Address [31:08].** Bits are read/write capable to provide the ability for device independent software on the system board to relocate the AIC-7890A/91 Device register space on 256 byte I/O command boundaries within the low 32-bit address segment of the 32/64-bit address space.
07-02	(0)	(r)	IBMADR[07:02]	**I/O Base Map Address [07:02].** Always reads 0.
01	(0)	(r)	RSVD	Always reads 0.
00	(1)	(r)	ISPACEIND	**I/O Space Indicator.** Always reads 1. **Note:** Bit [00] =1 indicates that BASEADR0 register is used for mapping into system I/O address space.

Base Address 1 (BASEADR1)

Type:R/W
Address:N-14h

Base Address register 1, enables the AIC-7890A/91 Device register space to be relocated (mapped) within system Memory Address space to enable the system board device independent POST software to build a consistent system memory address map. The AIC-7890A/91 Device register space, located in Memory Address space, improves throughput of the AIC-7890A/91 Device register transactions. **BASEADR1** may be read at any time in Configuration space. **BASEADR1** value is reset to 0h during **PCIRST#** assertion.

Note: Software when using **BASEADR1** with **MSPACEEN** active to access Device registers must ensure that instructions not allow data moves that bridge 32-bit boundaries to ensure that bytes are not transferred out of intended order. When **BASEADR1** and **EXROMBADR** registers contain the same value and **EXROMEN** is active, a Target-Abort response will result if a memory access is made to its device space registers.

BASEADR1 R/W							
31	MBMADR31	23	MBMADR23	15	MBMADR15	07	MBMADR07=0
30	MBMADR30	22	MBMADR22	14	MBMADR14	06	MBMADR06=0
29	MBMADR29	21	MBMADR21	13	MBMADR13	05	MBMADR05=0
28	MBMADR28	20	MBMADR20	12	MBMADR12	04	MBMADR04=0
27	MBMADR27	19	MBMADR19	11	MBMADR11=0	03	PREFETCH=0
26	MBMADR26	18	MBMADR18	10	MBMADR10=0	02	MSPACTYP1=1
25	MBMADR25	17	MBMADR17	09	MBMADR09=0	01	MSPACTYP0=0
24	MBMADR24	16	MBMADR16	08	MBMADR08=0	00	MSPACEIND=0

BASEADR1 R/W							
63	MBMADR63	55	MBMADR55	47	MBMADR47	39	MBMADR39
62	MBMADR62	54	MBMADR54	46	MBMADR46	38	MBMADR38
61	MBMADR61	53	MBMADR53	45	MBMADR45	37	MBMADR37
60	MBMADR60	52	MBMADR52	44	MBMADR44	36	MBMADR36
59	MBMADR59	51	MBMADR51	43	MBMADR43	35	MBMADR35
58	MBMADR58	50	MBMADR50	42	MBMADR42	34	MBMADR34
57	MBMADR57	49	MBMADR49	41	MBMADR41	33	MBMADR33
56	MBMADR56	48	MBMADR48	40	MBMADR40	32	MBMADR32

Bit			Name	Definition
63-12	(0)	(r/w)	MBMADR[63:12]	**Memory Base Map Address[63-12].** Bits are read/write capable to indicate a mapping increment capability of 4096 bytes of system memory space. The AIC-7890A/91 decodes only the lower 8-bit address of the selected 4096-byte range. In other words, the AIC-7890A/91's 256-byte memory command range rolls over within the selected 4096-byte space.
11-04	(0)	(r)	MBMADR[11:04]	**Memory Base Map Address[11-04].** Indicates address space requirement. Always reads 0.
03	(0)	(r)	PREFETCH	**Prefetchable.** Always reads 0. The AIC-7890A/91 does not support this feature.
02-01	(2h)	(r)	MSPACTYP[1:0]	**Memory Space Access Type [1:0].** AIC-7890A/91 as a target may be located anywhere in the 64-bit address space of a 64-bit capable system.
00	(0)	(r)	MSPACEIND	**Memory Space Indicator.** Always reads 0. **Note:** Bit [00] =0 indicates that BASEADR1 register is used for mapping into system Memory Address space.

Subsystem Vendor ID, Subsystem ID (SUBVENDOR_ID, SUBSYSTEM_ID)

Type:R/W
Address:N-2Ch

Subsystem Vendor ID and Subsystem ID registers are used to uniquely identify the add-in board or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their cards from one another even though the cards may have the same PCI controller installed on them. SUBVENDOR_ID and SUBSYSTEM_ID may be read at any time in configuration space. The SUBVENDOR_ID and SUBSYSTEM_ID default register value is read only, but may be changed immediately following PCIRST# assertion through IDDAT pin if desired. If IDDAT is unconnected or pulled high, the default values in the registers are not changed. The default value of SUBVENOR_ID is 9005h, and SUBSYSTEM_ID is 000Fh. In revision 0 chips, if both TESTMODE# and PDPUDIS# pins are tied high, then SUBVENDOR_ID[15:0] is copied to VENDOR_ID[15:0] and the lower nibble of SUBSYSTEM_ID[3:0] is copied to DEVICE_ID[3:0] after IDDAT values are shifted in. In later revisions of the chip, if both the TESTMODE# and PDPUDIS# pins are tied high, only the lower nibble of SUBSYS_ID[3:0] is copied to DEVICE_ID[3:0] after IDDAT values are shifted in. See *Clock and Miscellaneous Pins* on page 2-30 for more details.

If the ID Write Enable (IDWEN) bit is set in the IDENREG register, the SUBSYSTEM_ID and SUBVENDOR_ID registers are writeable and readable. If the IDWEN bit is cleared, the SUBSYSTEM_ID and SUBVENDOR_ID registers are read-only. In revision 0 chips (DEVREV_ID = 00h), these registers are read-only.

SUBSYSTEM_ID R/W			
31	SUBSYSTEM_ID15	23	SUBSYSTEM_ID07
30	SUBSYSTEM_ID14	22	SUBSYSTEM_ID06
29	SUBSYSTEM_ID13	21	SUBSYSTEM_ID05
28	SUBSYSTEM_ID12	20	SUBSYSTEM_ID04
27	SUBSYSTEM_ID11	19	SUBSYSTEM_ID03
26	SUBSYSTEM_ID10	18	SUBSYSTEM_ID02
25	SUBSYSTEM_ID09	17	SUBSYSTEM_ID01
24	SUBSYSTEM_ID08	16	SUBSYSTEM_ID00

SUBVENDOR_ID R/W			
15	SUBVENDOR_ID15	07	SUBVENDOR_ID07
14	SUBVENDOR_ID14	06	SUBVENDOR_ID06
13	SUBVENDOR_ID13	05	SUBVENDOR_ID05
12	SUBVENDOR_ID12	04	SUBVENDOR_ID04
11	SUBVENDOR_ID11	03	SUBVENDOR_ID03
10	SUBVENDOR_ID10	02	SUBVENDOR_ID02
09	SUBVENDOR_ID09	01	SUBVENDOR_ID01
08	SUBVENDOR_ID08	00	SUBVENDOR_ID00

Bit			Name	Definition
31-16	(000Fh)	(r)	SUBSYSTEM_ID	**Subsystem ID.** Please see *Clock and Miscellaneous Pins* on page 2-30 for more details.
15-0	(9005h)	(r)	SUBVENDOR_ID	**Subsystem Vendor ID.** Please see *Clock and Miscellaneous Pins* on page 2-30 for more details.

Expansion ROM Base Address (EXROMBADR)

Type:R/W
Address:N-30h

The Expansion ROM Base Address register is used to define the base address, maximum size and access enable control of a local external ROM device which may be used with a PCI device. The external ROM's data and address must pass through an additional interface Memory Port of the device and use its normal address/data path to the PCI bus so that no additional loading is presented to the PCI bus other than the device's loading without the external ROM. **EXROMBADR** may be read at any time in Configuration space. **EXROMBADR** value is reset to 0h during **PCIRST#** assertion. The AIC-7890A/91 supports an external ROM/FLASH EPROM of 128 KBytes and no slower than 150 nsec access on its FlexPort. When a memory access is made to the AIC-7890A/91 with both **BASEADR1** and **EXROMBADR** registers containing the same value and **EXROMEN** is active, it will result in a Target-Abort response.

EXROMBADR R/W							
31	EXROMBADR31	23	EXROMBADR23	15	EXROMBADR15	07	RSVD
30	EXROMBADR30	22	EXROMBADR22	14	EXROMBADR14	06	RSVD
29	EXROMBADR29	21	EXROMBADR21	13	EXROMBADR13	05	RSVD
28	EXROMBADR28	20	EXROMBADR20	12	EXROMBADR12	04	RSVD
27	EXROMBADR27	19	EXROMBADR19	11	EXROMBADR11	03	RSVD
26	EXROMBADR26	18	EXROMBADR18	10	RSVD	02	RSVD
25	EXROMBADR25	17	EXROMBADR17	09	RSVD	01	RSVD
24	EXROMBADR24	16	EXROMBADR16=0	08	RSVD	00	EXROMEN

Bit			Name	Definition
31-17	(0)	(r/w)	EXROMBADR[31:17]	**Expansion ROM Base Address[31:17].** Bits are read/write capable to indicate a mapping increment capability of 128 KBytes.
16-11	(0)	(r)	EXROMBADR[16:11]	**Expansion ROM Base Address[16:11].** Always reads 0 to set the maximum ROM size to 128 KBytes.
10-01	(0)	(r)	RSVD	Always reads 0.

Bit			Name	Definition
00	(0)	(r/w)	EXROMEN	**Expansion ROM Enable.** When active (=1) (and MSPACEEN in the Configuration Command register is active), enables the device to accept accesses to its expansion ROM. MSPACEEN in the COMMAND register should not be active when writing to set EXROMEN active. For reads, the AIC-7890A/91 will use latched AD[31:02] and internally generated address [1:0] to access four bytes from the AIC-7890A/91's external ROM/Flash EPROM for each PCI expansion ROM read access, with TRDY# deasserted until all bytes are assembled into 32 bits for the access regardless of the CBE[3:0]# value. The first byte read from the ROM/Flash EPROM will be stored in bits 7-0 and the fourth byte in bits 31-24. As the combined access exceeds the maximum PCI recommended data access period, all PCI burst attempts will be disconnected on each Data phase transfer of the transaction. For writes, the AIC-7890A/91 will use latched AD[31:02] and the single asserted CBE[3:0]# to generate the internal address [1:0] to write a byte to the external EEPROM with TRDY# deasserted until the access is completed. PCI burst attempts will be disconnected after the first Data phase transfer. Accesses with more than one CBE bit asserted will result in a Target-Abort response. **Note:** Accesses may also be extended due to arbitration when required. Unless both EXROMEN and MSPACEEN are active, access attempts to external ROM addresses will not return DEVSEL# and will be ignored.

Capability Pointer (CAP_PTR)

Type:R
Address:N-34h

The Capability pointer register specifies the location of the first item in the Power Management Registers. The first register is located at address DCh of the PCI configuration space.

CAP_PTR R	
07	CAP_PTR07
06	CAP_PTR06
05	CAP_PTR05
04	CAP_PTR04
03	CAP_PTR03
02	CAP_PTR02
01	CAP_PTR01
00	CAP_PTR00

Bit		Name	Definition
7-0 (DCh)	(r)	CAP_PTR[7:0]	**Capabilities Pointer Address[7:0].** Always reads DCh.

Interrupt Line Select (INTLINSEL)

Type:R/W
Address:N-3Ch

The Interrupt Line Select register provides the capability for the system to communicate to the device's software driver to identify the system interrupt line that has been connected to the devices interrupt pin when one has been included in the devices design. When no interrupt pin is provided in the device's design, this register is RSVD and read only with a value of 0h.

INTLINSEL R/W	
07	INTLS7
06	INTLS6
05	INTLS5
04	INTLS4
03	INTLS3
02	INTLS2
01	INTLS1
00	INTLS0

Bit			Name	Definition
7-0	(0)	(r/w)	INTLS[7:0]	**Interrupt Line Select [7:0].** Bits are read-write capable to provide device drivers and operating system to know which system Interrupt line number (0-15 for standard dual 8259) AIC-7890A/91 interrupt output IRQA# has been connected.

INTLS[7:0]	Assignment
0Fh-00h	Interrupt numbers (referenced to a standard dual 8259 configuration).
FEh-10h	RSVD.
FFh	No connection or unknown. NOTE: The AIC-7890A/91 driver does not operate with this setting.

Interrupt Pin Select (INTPINSEL)

Type:R
Address:N-3Dh

The Interrupt Pin Select register specifies the PCI interrupt pin the device (or device function) uses. A separate Configuration space is required for each function in a device and only one pin may be identified in each space. INTPINSEL register may be read at any time in Configuration space. The AIC-7890A/91 supports PCI Configuration header type 00h (only one function) with INTA#.

INTPINSEL R	
07	INTPS7
06	INTPS6
05	INTPS5
04	INTPS4
03	INTPS3
02	INTPS2
01	INTPS1
00	INTPS0

Bit			Name	Definition
07-00	(01h)	(r)	INTPS[7:0]	Always reads 1h.

Min_Gnt Status (MINGNT)

Type:R
Address:N-3Eh

The Minimum Grant register indicates the desired GNT# asserted burst period needed to complete transfer of a devices data buffer assuming that the intended target does not extend the transfer time by use of TRDY#. The value read from the register specifies a period of time in units of 0.25 microsecond. The AIC-7890A/91's MINGNT register value is 27h which is the minimum time to burst out its 512-byte buffer assuming SCSI is also transferring at 80MB/sec. *The* AIC-7890A/91 *is able to operate with any size GNT# period from one clock to constant park condition.* MINGNT register may be read at any time in Configuration space.

MINGNT R	
07	MINGNT7
06	MINGNT6
05	MINGNT5
04	MINGNT4
03	MINGNT3
02	MINGNT2
01	MINGNT1
00	MINGNT0

Bit			Name	Definition
07-00	(27h)	(r)	MINGNT[7:0]	Always reads 27h.

MINGNT = $\frac{512 \text{ bytes}}{(133 - 80) \text{ MB/sec}}$ = 9.7us / .25 us = 39 decimal (27h)

Max_Lat Status (MAXLAT)

Type:R
Address:N-3Fh

The Maximum Latency register indicates how often the device needs to gain access to the PCI bus. The value read from the register specifies a period of time in units of 0.25 microsecond. The AIC-7890A/91's MAXLAT register value is 19h which is the minimum time to fill/empty 512 bytes of data on Ultra 2 SCSI bus read/write before requesting for PCI bus (PREQ# asserted). *The* AIC-7890A/91 *can operate with any size LAT_TIME register value.* MAXLAT register may be read at any time in Configuration space.

MAXLAT R	
31	MAXLAT7
30	MAXLAT6
29	MAXLAT5
28	MAXLAT4
27	MAXLAT3
26	MAXLAT2
25	MAXLAT1
24	MAXLAT0

Bit			Name	Definition
07-00	(19h)	(r)	MAXLAT[7:0]	Always reads 19h.

MAXLAT = $\frac{512 \text{ bytes}}{80 \text{ MB/sec}}$ = 6.4 us/ .25us = 25 decimal (19h)

Device Configuration (DEVCONFIG)

Type:R/W
Address:N-40h

Device Configuration register provides the AIC-7890A/91 with mode selection control of features in the AIC-7890A/91. **DEVCONFIG** may be read/written at any time in Configuration space. However, changing values in this register must be done with care due to the functional changes they control.

DEVCONFIG R/W		
	AIC-7890A	**AIC-7891**
07	RSVD	PCI64BIT
06	MRDCEN	MRDCEN
05	RSVD	RSVD
04	EXTSCBPEN	EXTSCBPEN
03	RSVD	RSVD
02	DACEN	DACEN
01	STPWLEVEL	STPWLEVEL
00	RSVD	RSVD

Bit			Name	Definition
07	(0)	(r/w)	RSVD (AIC-7890A)	Always reads 0 for AIC-7890A. This bit must not be set to 1 for AIC-7890A.
07	(*)	(r/w)	PCI64BIT (AIC-7891)	**PCI 64-Bit.** When this bit is cleared (=0), the PCI interface of AIC-7891 is capable of 32-bit transfer only, but it doesn't inhibit the AIC7891 to use DAC to access 64-bit system memory as a bus master. When this bit is set (=1), the PCI interface of AIC-7891 is capable of 32/64-bit transfer, depending on the PCI bus width and the active PCI device. **Note:** For AIC-7891, the default value is depended on the REQ64# pin value during the time PCIRST# is asserted and then deasserted. If REQ64# is low (=0), PCI64BIT is set, and if REQ64# is high (=1), PCI64BIT is cleared.

Bit			Name	Definition
06	(1)	(r/w)	MRDCEN	**Memory Read Command Enable.** When active (=1), enables the PCI master command out generator to generate the MRDC command value for its defined conditions. Enables master burst transfers being made with MRDLC or MRDMC commands to release the bus after the current and next data transfers are completed when the LAT_TIME register has expired and GNT# is not asserted. When inactive(=0), causes the PCI master command out generator to convert all MRDC commands to MRDLC commands. Enables master burst transfers being made with MRDLC or MRDMC commands, when the LAT_TIME register has expired and GNT# is not asserted, to release the bus after completing the current cache line.
05	(0)	(r)	RSVD	Always reads 0.
04	(0)	(r/w)	EXTSCBPEN	**External SCB Parity Enable.** When active (=1) and RAMPSM is active, enables checking of odd-byte parity for SCB data read from an external 9-bit SRAM. Note that when a 8-bit SRAM is present, do not enable checking of external SCB parity.
03	(0)	(r)	RSVD	Always reads 0.
02	(0)	(r/w)	DACEN	**Dual Address Cycle Enable.** When active, enables the AIC-7890A/91 to issue Dual Address Cycle (DAC) master transactions of 32-bit range within a 32-bit page of a 64-bit range pointed to by the value stored in the HADDR[7:4] and CCHADDR[7:4] registers. When HADDR[7:4]/CCHADDR[7:4] stored value is zero, only Single Address Cycles (SAC) may be issued the same as when DACEN is not active.
01	(0)	(r/w)	STPWLEVEL	**SCSI Termination Power Level.** When inactive (=0), selects the high level for the active state of the STPWCTL output. When active, selects the low level for the active state of output STPWCTL. STPWLEVEL is cleared to the inactive state by PCIRST# assertion. Writing to the CHIPRST bit in the Device HCNTRL register has no effect on STPWLEVEL.
00	(0)	(r)	RSVD	Always reads 0.

Device Status 0 (DEVSTATUS0)

Type:R/W
Address:N-41h

Device Status 0 register provides read capability for selected internal conditions as well as Big-Endian modes support in the AIC-7890A/91. **DEVSTATUS0** may be read or written at any time in Configuration space.

DEVSTATUS0 R/W	
07	DMABIGENDIAN
06	TARBIGENDIAN
05	RSVD
04	RSVD
03	TESTMODE
02	MPORTMODE
01	RSVD
00	VOLSENSE

Bit			Name	Definition
07	(0)	(r/w)	DMABIGENDIAN	**DMA Big Endian Mode**. When this bit is set, DMA data transfers are performed using big endian format. This bit is mirrored to bit 7 of the DEVSTATUS1 register.
06	(0)	(r/w)	TARBIGENDIAN	**Target Big Endian Mode**. When this bit is set, target mode data transfers are performed using big endian format. This bit is mirrored to bit 6 of the DEVSTATUS1 register.
05-04	(0)	(r)	RSVD	Always reads 0.
03	(*)	(r)	TESTMODE	**TestMode pin.** Provides a status bit for the TESTMODE# pin. If TESTMODE# pin is low, then this bit is 1. If TESTMODE# pin is high, then this bit is 0. **Note:** (*) Always reflects the inverse state of TESTMODE# pin.
02	(*)	(r)	MPORTMODE	**Memory Port Mode**. Provides the capability to determine when the AIC-7890A/91's Memory Port is in Single-user (dedicated) mode (=1) or in Multiuser mode (=0). **Note:** (*) EXTARBACK# is sampled after PCIRST# is deasserted from the active state. If EXTARBACK# is low, MPORTMODE is 1, and if EXTARBACK# is high, MPORTMODE is 0.
01	(0)	(r)	RSVD	Always reads 0.

Bit			Name	Definition
00	(*)	(r)	VOLSENSE	**Voltage Sense.** Provides the capability to determine which PCI bus voltage level ((=0) for 3.3V and (=1) for 5V) that the AIC-7890A/91's PCI interface has been connected to. The state of VOLSENSE adjusts the operation of the AIC-7890A/91's PCI interface pin cells to account for the difference in voltage. **Note:** (*) The reset state is determined by the external voltage present.

Device Status 1 (DEVSTATUS1)

Type:R/W
Address:N-42h

Device Status 1 register contains the two mirrored bits 7 and 6 of the DEVSTATUS0 register for the Big-endian mode support, and selects the PCI bus size.

DEVSTATUS1 R/W	
07	DMABIGENDIAN
06	TARBIGENDIAN
05	RSVD
04	RSVD
03	RSVD
02	RSVD
01	RSVD
00	RSVD

Bit			Name	Definition
07	(0)	(r/w)	DMABIGENDIAN	**DMA Big Endian Mode**. This bit mirrors bit 7 of DEVSTATUS0 register for big-endian support.
06	(0)	(r/w)	TARBIGENDIAN	**Target Big Endian Mode**. This bit mirrors bit 6 of DEVSTATUS0 register for big-endian support.
05-00	(0)	(r)	RSVD	Always reads 0.

PCI Error Generation (PCIERRGEN)

Type:R/W
Address:N-43h

This register provides the capability to generate PCI errors for testing conditions with diagnostic support.

PCIERRGEN R/W	
07	PCIERRGENDIS
06	DIS_SCHMITT
05	RSVD
04	MADRSPARERR
03	MWDATPARERR
02	TRDATAPARERR
01	MTDATAPARERR
00	TADRSPARERR

Bit			Name	Definition
07	(1)	(r/w)	PCIERRGENDIS	**PCI Error Generation Disable.** When active (=1) prevents other active bits in this register from generating an error. When active, allows reading the active state of the other bits for test purpose.
06	(0)	(r/w)	DIS_SCHMITT	**Disable Precision Schmitt.** When set (=1), this bit allows the user to disable the SCSI I/O precision schmitt trigger circuitry. This bit should only be set for evaluation purposes.
05	(0)	(r)	RSVD	Always reads 0.
04	(0)	(r/w)	MADRSPARERR	**Master Address Parity Error.** When this bit is active (=1) and PCIERRGENDIS is not active, AIC-7890A/91 as a PCI bus master will cause a parity error on the next master address phase. Then, this bit will automatically reset.
03	(0)	(r/w)	MWDATPARERR	**Master Write Data Parity Error.** When this bit is active (=1) and PCIERRGENDIS is not active, AIC-7890A/91 as a PCI bus master will cause a parity error on the next master write data phase that transfers data. Then, this bit will automatically reset.
02	(0)	(r/w)	TRDATAPARERR	**Target Read Data Parity Error.** When this bit is active (=1) and PCIERRGENDIS is not active, AIC-7890A/91 as a PCI bus master will cause a parity error on the next target read data phase that transfers data. Then, this bit will automatically reset.

Bit			Name	Definition
01	(0)	(r/w)	MTDATAPARERR	**Master/Target Data Parity Error.** When this bit is active (=1) and PCIERRGENDIS is not active, AIC-7890A/91 as a PCI target will signal a parity error on the next master read data phase or target write data phase. Then, this bit will automatically reset.
00	(0)	(r/w)	TADRSPARERR	**Target Address Parity Error.** When this bit is active (=1) and PCIERRGENDIS is not active, AIC-7890A/91 as a PCI target will signal a parity error on the next target address phase. Then, this bit will automatically reset.

Capability Identifier (CAPABILITY_ID)

Type:R
Address:N-DCh

This Capability Identifier register (= 01h) identifies about its capability for Power Management function.

CAPABILITY_ID R	
07	CAP_ID07
06	CAP_ID06
05	CAP_ID05
04	CAP_ID04
03	CAP_ID03
02	CAP_ID02
01	CAP_ID01
00	CAP_ID00

Bit	Name	Definition
7-0(01h)(r)	CAP_ID	**Capability Identifier.** Always reads 01h.

Next Item Pointer (NEXT_ITEM_PTR)

Type:R

Address:N-DDh

This Next Item Pointer register indicates the offset Configuration Space location of the next item in the Power Management's capability list. Value of zero indicates that no more items are in the list.

NEXT_ITEM_PTR R	
07	NEXT_ITEM_PTR07
06	NEXT_ITEM_PTR06
05	NEXT_ITEM_PTR05
04	NEXT_ITEM_PTR04
03	NEXT_ITEM_PTR03
02	NEXT_ITEM_PTR02
01	NEXT_ITEM_PTR01
00	NEXT_ITEM_PTR00

Bit	Name	Definition
7-0(00h)(r)	NEXT_ITEM_PTR	**Next Item Pointer.** Always reads 00h.

Power Management Capabilities (PM_CAPABILITY)

Type:R
Address:N-DEh

This 16-bit Power Management Capabilities register provides information regarding the Power management capabilities.

PM_CAPABILITY R			
15	PME_SUPPORT4	07	RSVD
14	PME_SUPPORT3	06	RSVD
13	PME_SUPPORT20	05	DSI
12	PME_SUPPORT1	04	AUX_POWER
11	PME_SUPPORT0	03	PME_CLOCK
10	D2_SUPPORT	02	PM_VERSION2
09	D1_SUPPORT	01	PM_VERSION1
08	RSVD	00	PM_VERSION0

Bit			Name	Definition
15-11	(0)	(r)	PME_SUPPORT	**PME_SUPPORT.** This 5 bit field indicates the power states supported for asserting PME#. The AIC-7890A/91 cannot support (assert) PME#. Always reads 00h.
10	(0)	(r)	D2_SUPPORT	**D2_SUPPORT.** AIC-7890A/91 is not capable of D2 Power Management State. Always reads 0.
09	(0)	(r)	D1_SUPPORT	**D1_SUPPORT.** AIC-7890A/91 is not capable of D1 Power Management State. Always reads 0.
08	(0)	(r)	RSVD	Always reads 0.
07-06	(0)	(r)	RSVD	Always reads 0.
05	(0)	(r)	DSI	**Device Specific Initialization.** When set, a specific device driver is required to reinitialize AIC-7890A/91 after it leaves D3 (Power Down) state to D0 (active or normal) state.
04	(0)	(r)	AUX_POWER	**Auxiliary Power Source.** Not supported. Always reads 0.
03	(0)	(r)	PME_CLOCK	**PME Clock.** Not supported. Always reads 0.
02-00	(1)	(r)	PM_VERSION	**Power Management Version.** This field indicates that Power Management is implemented as revision 1.0 Always reads 1.

Power Management Control Status Register (PM_CSR)

Type:R/W
Address:N-E0h

This 16-bit Power Management Control/Status register allows the control of Power States.

PM_CSR R/W			
15	PME_STATUS	07	RSVD
14	DATA_SCALE1	06	RSVD
13	DATA_SCALE0	05	RSVD
12	DATA_SELECT3	04	RSVD
11	DATA_SELECT2	03	RSVD
10	DATA_SELECT1	02	RSVD
09	DATA_SELECT0	01	POWER_STATE1
08	PME_EN	00	POWER_STATE0

Bit			Name	Definition
15	(0)	(r)	PME_STATUS	**PME STATUS.** This status bit indicates that PME# was asserted regardless of PME_EN bit. AIC-7890A/91 does not support PME#. Always reads 0.
14-13	(0)	(r)	DATA_SCALE[1:0]	**Data Scaling Factor.** This field is used in conjunction with the PM_Data register. AIC-7890A/91 does not support PM_Data register. Always reads 0.
12-09	(0)	(r)	DATA_SELECT[3:0]	**Data Select.** This field is used to select the data reported in the PM_Data register. AIC-7890A/91 does not support PM_Data register. Always reads 0.
08	(0)	(r)	PME_EN	**PME Enable.** AIC-7890A/91 does not support PME#. Always reads 0.
07-02	(0)	(r)	RSVD	Always reads 0.
01-00	(0)	(r/w)	POWER_STATE	**Power Management States.** AIC-7890A/91 only supports 2 states 00 - D0 (normal operation) 00 - D1 (same as D0) 10 - D2 (same as D0) 11 - D3 (Power Down internal CLK40 Stopped)

PMCSR Bridge Support Extension (PMCSR_BSE)

Type:R
Address:N-E2h

The PMCSR_BSE register defines PCI bridge specific functionality for PCI-to-PCI bridges. The Bridge Support Extension is not supported and therefore PMCSR_BSE is assigned a value of zero.

PMCSR_BSE R	
07	PPCC_EN
06	B2_B3#
05	RSVD
04	RSVD
03	RSVD
02	RSVD
01	RSVD
00	RSVD

Bit			Name	Definition
7	(0)	(r)	BPCC_EN	**Bus Power/Clock Control Enable.** This bit ties controls of the PCI secondary Power/Clock source to the originating source for PCI-to-PCI bridge. This function is NOT supported. Always reads 0
6	(0)	(r)	B2_B3#	**B2/B3 Support for D3*hot*.** This bit is used to determine the PM state of the secondary PCI bus for D3*hot* in a PCI-to-PCI bridge implementation. This function is NOT supported. Always reads 0
07-00	(0)	(r)	RSVD	Reserved. Always reads 0

PM Data Register (PM_DATA)

Type:R
Address:N-E3h

The PM_DATA register is used to report operating states such as Power Consumption or Heat Dissipation. These features are currently not supported and the bits are therefore assigned a value of zero

PM_DATA R	
07	PM_DATA07
06	PM_DATA06
05	PM_DATA05
04	PM_DATA04
03	PM_DATA03
02	PM_DATA02
01	PM_DATA01
00	PM_DATA00

Bit			Name	Definition
7-0	(00h)	(r)	PM_DATA	**PM Data Register.** This feature is not supported. Always reads 0.

ID Enable Register (IDENREG)

Type:R/W
Address:N-FFh

The IDENREG register may be read/written at any time in Configuration space. The IDENREG vaule is reset to 0h only during PCIRST# assertion.

IDENREG R/W	
07	RSVD
06	RSVD
05	RSVD
04	RSVD
03	RSVD
02	RSVD
01	RSVD
00	IDWEN

Bit			Name	Definition
7-1	(0)	(r)	RSVD	Always reads 0.
0	(0)	(r/w)	IDWEN	**ID Write Enable**. When active (=1), allows write access to SUBVENDOR_ID, SUBSYSTEM_ID, and DEVICE_ID registers in Configuration space. When inactive (=0), configuration write accesses have no effect on the above registers.

Device Registers in the Functional Mode (ALT_MODE = 0)

SCSI Sequence Control (SCSISEQ)

Type:R/W
Address:M-00h, DS-00h

Each bit, when set, enables the specified hardware sequence. The register is readable to allow bit manipulation instructions without saving a register image in scratch RAM. All bits except SCSIRSTO can be cleared by SCSI bus reset.

SCSISEQ R/W	
7	TEMODEO
6	ENSELO
5	ENSELI
4	ENRSELI
3	ENAUTOATNO
2	ENAUTOATNI
1	ENAUTOATNP
0	SCSIRSTO

Bit			Name	Definition
7	(0)	(r/w)	TEMODEO	**Target Enable Mode Out**. This bit is used to select whether ENSELO will start a Selection Out (TEMODEO = 0) or a Reselection Out (TEMODEO = 1) SCSI bus sequence.
6	(0)	(r/w)	ENSELO	**Enable Selection Out**. When this bit is set, it will allow the SCSI logic to perform a Selection sequence (TEMODEO = 0) as an Initiator (ID = OID field of SCSIID register) and select a Target (ID = TID field of the SCSIID register), or to perform a Reselection sequence (TEMODEO = 1) as a Target (ID = OID field of SCSIID register) and reselect an Initiator (ID = TID field of the SCSIID Register). The SELINGO status (bit 4, SSTAT0) is one when the SCSI logic has entered the Selection/Reselection phase and is waiting for BSY back from the Target/Initiator. The sequencer must wait for SELDO status (bit 6, SSTAT0) to be one or SELTO (bit 7, SSTAT1) to be one if the hardware selection time-out is enabled (bit 2, SXFRCTL1 is set to one), or for the software selection time-out if the hardware time-out is not enabled. This control is cleared by the sequencer, or by a PCIRST# reset.

Bit			Name	Definition
5	(0)	(r/w)	ENSELI	**Enable Selection In.** When this bit is set to one, it will allow the SCSI logic to respond to a valid Selection sequence. When selected, the SELDI status (bit 5, SSTAT0) is set to one and TARGET status (bit 7, SSTAT0) is set to one. This control is only set to zero by the sequencer when no more selections are wanted. The AIC-7890A/91's Target ID is defined by the value in the OID field and the contents of the TARGETID register pair.
4	(0)	(r/w)	ENRSELI	**Enable Reselection In.** When this bit is set to one, it will allow the SCSI logic to respond to a valid Reselection sequence. When reselected the SELDI status (bit 5, SSTAT0) is one and TARGET status (bit 7, SSTAT0) is set to zero. This control is reset to zero by writing a zero to this bit.
3	(0)	(r/w)	ENAUTOATNO	**Enable Auto Attention Out.** When this bit is set to one, SCSI ATN will be asserted when a Selection sequence (ENSELO=1, TEMODEO=0) is executed. This is used when you are an Initiator and want to follow the Selection with a Message Out. SCSI ATN may be cleared by the sequencer by writing one to CLRATNO (bit 6, CLRSINT1), or by a Bus Free state on the SCSI bus. Writing a zero to this bit does not clear ATN.
2	(0)	(r/w)	ENAUTOATNI	**Enable Auto Attention In.** When this bit is set to one, SCSI ATN will be asserted when you are reselected by a Target (ENRSELI=1). This is used when you are an Initiator and want to follow the Reselection with a Message Out (refer to SCSI-3 Specification). SCSI ATN may be cleared by the sequencer by writing one to CLRATNO (bit 6, CLRSINT1), or by a Bus Free state on the SCSI bus. Writing a zero to this bit does not clear ATN.
1	(0)	(r/w)	ENAUTOATNP	**Enable Auto Attention Parity.** When this bit is set to one with ENSPCHK (bit 5, SXFRCTL1) and you are an Initiator, SCSI ATN will be asserted during information transfer in phases (Data In, Message In, Status In) if a parity error is detected on SCD[7:0] or SCD[15:8]. SCSI ATN may be cleared by the sequencer by writing one to CLRATNO (bit 6, CLRSINT1), or by a Bus Free state on the SCSI bus. Writing a zero to this bit does not clear ATN.
0	(0)	(r/w)	SCSIRSTO	**SCSI Reset Out.** When this bit is set to one, SCSI RESET# is asserted on the SCSI bus. It must be cleared by the sequencer with a write of 0 to this bit. This control is not gated with the Target/Initiator mode.

SCSI Transfer Control 0 (SXFRCTL0)

Type:R/W
Address:M-01h, DS-01h

This register together with **SXFRCTL1** are used to control the SCSI module data path.

SXFRCTL0 R/W	
7	DFON
6	DFPEXP
5	RSVD
4	CLRSTCNT
3	SPIOEN
2	SCAMEN
1	CLRCHN
0	RSVD

Bit			Name	Definition
7	(0)	(r/w)	DFON	**Digital Filtering On** When set, this bit enables digital filtering on the incoming REQ or ACK signal. Filter period is determined by current SCSI data transfer rate and state of DFPEXP bit below.
6	(0)	(r/w)	DFPEXP	**Digital Filtering Period Expanded.** When this bit is set to one, it increases the minimum filter period from 50.0 to 62.5 nsec if the SCSI transfer rate is set to less than or equal to 5 MBytes/sec. When the SCSI transfer rate is greater than 5 MBytes/sec, this bit has no effect on the filter period.
5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r/w)	CLRSTCNT	**Clear SCSI Transfer Count.** When set to one, the SCSI transfer counter (STCNT) is reset to 000000h. This bit is self-clearing and need not be toggled. This bit is always read back as zero. This does not affect the SHADDR
3	(0)	(r/w)	SPIOEN	**SCSI PIO Enable.** When set to one, automatic PIO SCSI data transfer is enabled. This bit must remain set for the entire PIO transfer. The individual PIO transfers are triggered by reading or writing to SCSIDATL register depending on data direction and Target/Initiator mode. Writing a zero to this bit will stop any further PIO transfers without corrupting any valid data in the SCSIDATL register. In **INITIATOR** mode, this bit may be left on even when in DMA mode since SCSIEN or SDMAEN override it. (This should not be done in **TARGET** mode as it might cause inadvertent REQ assertions)

Bit			Name	Definition
2	(0)	(r/w)	SCAMEN	**SCAM Enable**. When active (=1), enables the SCSI module to perform level 1 SCAM protocol with HIM driver assistance. SCAMEN enables direct SCSI bus control through the SCSISIG and SCSIDAT registers. SCAMEN bit set also enables CLKOUT period timer bit in the SELTIMER register. (see SELTIMER description).
1	(0)	(r/w)	CLRCHN	**Clear Data Channel.** When set to one the Synchronous REQ/ACK offset counter will be cleared. The transfer control logic will also be initialized to a reset state. The SCSI transfer counters (STCNT and SHADDR) will not be changed. This is used to initialize the data channel for a transfer. This bit is self-clearing.
0	(0)	(r)	RSVD	Always reads 0.

The following table defines the digital filter "blanking period" limits.

DFON	DFPEXP	Transfer Rate	Min. Filter Period	Max. Filter Period	
0	X	—	0 nsec	0 nsec	filter off
1	0	=< 5 MXfer/sec	50.0 nsec	62.5 nsec	slow
1	1	=< 5 MXfer/sec	62.6 nsec	75.0 nsec	slow w/ dfexp
1	X	=< 10 MXfer/sec > 5 MXfer/sec	12.5 nsec	25.0 nsec	fast
1	X	=< 20 MXfer/sec > 10 MXfer/sec	8.0 nsec	10.0 nsec	ultra
1	X	> 20 MXfer/sec	6.0 nsec	8.0 nsec	ultra-2

SCSI Transfer Control 1 (SXFRCTL1)

Type:R/W
Address:M-02h, DS-02h

This register, together with **SXFRCTL0**, is used to control the SCSI module data path.

	SXFRCTL1 R/W
7	BITBUCKET
6	RSVD
5	ENSPCHK
4	STIMESEL1
3	STIMESEL0
2	ENSTIMER
1	ACTNEGEN
0	STPWEN

Bit			Name	Definition
7	(0)	(r/w)	BITBUCKET	**SCSI Bit Bucket Mode.** When this bit is set to one, it enables the SCSI logic to read data from the SCSI bus and throw it away or supply 00h write data. No data is saved and no transfer stops occur because of Data FIFO full/empty conditions. This only applies while in Initiator mode.
6	(0)	(r)	RSVD	Always reads 0.
5	(0)	(r/w)	ENSPCHK	**Enable SCSI Parity Checking.** When set to one, parity checking is enabled on SCSI bus during Selection, Reselection, and Information Transfer cycles. If a parity error is detected, SCSIPERR (bit 2, SSTAT1) is set and if ENAUTOATNP (bit 1, SCSISEQ) is set, then ATN is driven active on the SCSI bus. When set to a zero, SCSIPERR is always read as a zero.
4-3	(0)	(r/w)	STIMESEL[1:0]	**Selection Timeout Delay Select.** The value written to this two bit field sets the Selection Timeout delay. An alternate set of times may be enabled by setting the ALTSTIM bit in the SCAMCTL register. The table at the end of this section defines the normal and alternate choices.
2	(0)	(r/w)	ENSTIMER	**Enable Selection Timeout.** When set to one, enables the selection timer. During Selection or Reselection Out, if the timer times out the SCSI module will begin a "soft" selection abort process as defined in the SCSI 3 specification. If BSY is not sensed true in time then the SELTO bit in SSTAT1will be set and the (re)selection ended. If ENSTIMER is false the (re)selection will continue until terminated by the sequencer.

Bit			Name	Definition
1	(0)	(r/w)	ACTNEGEN	**Active Negation Enable**. When set this bit enables active negation on all SCSI output drivers except RESET#, BSY#, and SEL#. This bit is overridden by hardware, disabling active negation, during SCAM operations and when the chip is not logically connected to the SCSI bus.
0	(0)	(r/w)	STPWEN	**SCSI Termination Power Enable.** When in the active state (=1) will cause output STPWCTL to be in the asserted state selected by STPWLEVEL bit in the Configuration DEVCONFIG register. STPWCTL output may be used to enable or disable the external SCSI bus termination power source. When output STPWEN is inactive the external termination power device is expected to be off or disabled. STPWEN may also be used for a general purpose control bit for external logic.

The following table lists the Select Abort Timer Setting options:

ALTSTIM	STIMESEL1	STIMESEL0	Timer Delay.
0	0	0	256 msec.
0	0	1	128 msec
0	1	0	64 msec
0	1	1	32 msec.
1	0	0	256 msec
1	0	1	4 msec.
1	1	0	2 msec.
1	1	1	1 msec.

SCSI Control Signal In (SCSISIGI)

Type:R
Address:M-03h, DS-03h

The **SCSISIGI** register reads the actual state of the signals on the SCSI bus pins.

	SCSISIGI R
7	CDI
6	IOI
5	MSGI
4	ATNI
3	SELI
2	BSYI
1	REQI
0	ACKI

Bit			Name	Definition
7	(x)	(r)	CDI	Reads the state of the CD signal on the SCSI bus.
6	(x)	(r)	IOI	Reads the state of the IO signal on the SCSI bus.
5	(x)	(r)	MSGI	Reads the state of the MSG signal on the SCSI bus.
4	(x)	(r)	ATNI	Reads the state of the ATN signal on the SCSI bus.
3	(x)	(r)	SELI	Reads the state of the SEL signal on the SCSI bus.
2	(x)	(r)	BSYI	Reads the state of the BSY signal on the SCSI bus.
1	(x)	(r)	REQI	Reads the state of the REQ signal on the SCSI bus.
0	(x)	(r)	ACKI	Reads the state of the ACK signal on the SCSI bus.

SCSI Control Signal Out (SCSISIGO)

Type:W
Address:M-03h, DS-03h

The SCSISIGO write register lets the sequencer set the state of the SCSI bus control signals. However, only those control signals appropriate to the current mode (Target, Initiator or SCAM) are enabled onto the SCSI bus. The most significant three bits (CDO, IOO, and MSGO) are used for SCSI bus phase comparison in Initiator mode. All SCSISIGO write register bits are cleared by PCIRST#, CHIPRST, SCSI bus reset, or SCSI bus free.

SCSISIGO W	
7	CDO
6	IOO
5	MSGO
4	ATNO
3	SELO
2	BSYO
1	REQO
0	ACKO

Bit		Name	Definition
7	(w)	CDO	**CD Out.** If in Target mode, sets CD on SCSI bus. If in Initiator mode, sets the state of CD expected on the next REQ pulse. If in SCAM mode, sets CD on the SCSI bus.
6	(w)	IOO	**I/O Out.** If in Target mode, sets I/O on SCSI bus. If in Initiator mode, sets the state of I/O expected on the next REQ pulse. If in SCAM mode, sets I/O on the SCSI bus.
5	(w)	MSGO	**MSG Out.** If in Target mode sets MSG on SCSI bus. If in Initiator mode, sets the state of MSG expected on the next REQ pulse. If in SCAM mode, sets MSG on the SCSI bus.
4	(w)	ATNO	**ATN Out.** In Target mode, this bit is not used. In Initiator mode, writing one to this bit sets ATN on the SCSI bus. Writing a zero to this bit has no effect. ATN may be cleared by writing one to CLRATNO (bit 6 in CLRSINT1).
3	(w)	SELO	**SEL Out.** When set to one, asserts SEL on the SCSI bus. Can be used to negate SEL. If in SCAM mode, sets SEL on the SCSI bus.
2	(w)	BSYO	**BSY Out.** When set to one, asserts BSY on the SCSI bus. May also be used to negate BSY. When BSYO is set to one and the DIAGLEDEN bit in the Device SBLKCTL register is not active, LED output is asserted to indicate the AIC-7890A/91 is connected to the SCSI bus. If in SCAM mode, sets BSY on the SCSI bus.
1	(w)	REQO	**REQ Out.** If in Target mode, sets REQ on the SCSI bus. It is not functional in Initiator mode. If in SCAM mode, sets REQ on the SCSI bus.
0	(w)	ACKO	**ACK Out.** If in Initiator mode, sets ACK on the SCSI bus. It is not functional in Target mode.

SCSI Rate (SCSIRATE)

Type:R/W
Address:M-04h, DS-04h

The contents of this register determine the synchronous SCSI data transfer rate, and also the WIDEXFER bit is here.

This register must be programmed before doing any DMA transfers. Every time the AIC-7890A/91 connects to a SCSI device (selects or reselects a device, or is selected or reselected by a device) this register will be programmed to a value appropriate for transferring data to or from that device. In initiator mode, this register should be programmed during the initial message phase of a connection, before ACKing the message byte.

SCSIRATE R/W	
7	WIDEXFER
6	XFERRATE6
5	XFERRATE5
4	XFERRATE4
3	XFERRATE3
2	XFERRATE2
1	XFERRATE1
0	XFERRATE0

Bit			Name	Definition
7	(0)	(r/w)	WIDEXFER	**WIDE SCSI TRANSFER Bit.** When the SELWIDE bit (SBLKCTL register bit 1) and this bit are both set, then 16 bit SCSI transfers are enabled.
6-0	(0)	(r/w)	XFERRATE[6:0]	**SCSI Data Transfer Rate [6:0].** The period and maximum rate of REQ or ACK pulses generated by the SCSI module during synchronous information transfers. A table below defines the actual rates and periods.

XFERRATE [6:0]	REQ/ACK Rate	REQ/ACK Period	REQ/ACK Width
001_0011	40 MHz	25.0 nsec (2T)	12.5 nsec
001_0100	26.67 MHz (or 33 MHz)	37.5 nsec (3T) (or 30 nsec (2T))	12.5 nsec (or 15 nsec)
001_0101	20 MHz	50.0 nsec.(4T)	25.0 nsec
001_0110	16 MHz	62.5 nsec (5t)	37.5 nsec
001_0111	13.33 MHz	75.0 nsec (6T)	37.5 nsec
001_1000	10 MHz	100 nsec.(8T)	50.0 nsec
001_1001	8.0 MHz	125 nsec (10T)	50.0 nsec
001_1010	6.7 MHz	150 nsec (12T)	50.0 nsec
001_1011	5.7 MHz	175 nsec (14T)	50.0 nsec
001_1100	5.0 MHz	200 nsec (16T)	100 nsec
000_1111	NONE: this value reserved for S/W	N/A	N/A
000_0000	NONE: this value reserved for S/W	N/A	N/A

For SCSI data transfers below 5.0 MHz, use asynchronous transfer mode (do this by setting the **SCSIOFFSET** register to 0).

The 001_0100 code for **XFERRATE** is special. The SPI-2 specification calls for a transfer speed of 33 MHz, but this cannot be provided with **SCSICLK** at 80 MHz. The AIC-7890A/91 has an alternate **SCSICLK** input where a 66 MHz input can be passed in to provide 33 MHz. When **XFERRATE** is set to 001_0100, if there is a signal present on the alternate **SCSICLK** input, and the **DISABEXT66** bit in the **SCLKCTL** register is not set, then **SCSICLK** is switched to the alternate frequency (presumably 66 MHz) and transfers are done at half that speed. If there is no signal present on the alternate **SCSICLK** input, or if **DISABEXT66** is set, then **SCSICLK** stays at its usual 80 MHz and outgoing data, and strobes from AIC-7890A/91 will go at a third of that (26.67 MHz). Although this is not ideal, it is legal to go slower than the negotiated speed. The AIC-7890A/91 can accept incoming data and strobes at the full 33 MHz when operating this way.

Note: In the table, some **XFERRATE** settings are reserved as codes that may never be used for an actual transfer rate on this or any future chip. Software reserves these codes for its own use to represent that it hasn't yet negotiated a transfer speed with a particular SCSI device.

Loading the reserved codes, or any code not specified in the table above, will select a transfer rate of 5 MHz (or asynchronous, based on the setting of **SCSIOFFSET**).

SCSI Maximum Offset (SCSIOFFSET)

Type:R/W
Address:M-05h, DS-05h

The contents of this register determine the maximum synchronous REQ/ACK offset.

An offset value of 0 in the SCSIOFFSET register disables synchronous data transfers. Any offset value greater than 0 enables synchronous transfers.

SCSIOFFSET R/W	
7	RSVD
6	SCSIOFFSET6
5	SCSIOFFSET5
4	SCSIOFFSET4
3	SCSIOFFSET3
2	SCSIOFFSET2
1	SCSIOFFSET1
0	SCSIOFFSET0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6-0	(0)	(r/w)	SCSIOFFSET [6:0]	**SCSI Offset [6:0]** The maximum SCSI offset value. Software determines this value during synchronous negotiations, AIC-7890A/91 can support a maximum offset of 127 transfers. When set to 0, SCSI data transfers will be in asynchronous mode.

SCSI Latched Data (SCSIDATH, SCSIDATL)

Type:R/W
Address:M06/M-07h, DS-06/07h also writable at 12h/13h

This is a read/write latch used to transfer data on the SCSI bus during Automatic or Manual SCSI PIO transfer. These registers are used in both 8-bit and 16-bit data transfer modes. In 8-bit mode, data is written to or read from SCSIDATL only. The SCSI ACK (as Initiator) or REQ (as Target) is driven active when the write or read occurs if automatic SCSI PIO transfer is enabled. In 16-bit mode, SCSIDATH should be written or read before SCSIDATL. The initial read value after a chip reset is unknown. Valid SCSI bus read data is loaded into this register pair by the leading edge of the input data strobe (REQ or ACK). Direct unlatched access to the SCSI data bus is available via the SCSIBUSL(H) pair at address 12/13h. Data written to the SCSIBUS register pair is actually written to the SCSIDATAL(H) writable registers.

SCSIDATH R/W		SCSIDATL R/W	
7	DB15	7	DB07
6	DB14	6	DB06
5	DB13	5	DB05
4	DB12	4	DB04
3	DB11	3	DB03
2	DB10	2	DB02
1	DB09	1	DB01
0	DB08	0	DB00

SCSI Transfer Count (STCNT[2:0])

Type:R/W
Address:M-0Ah~08h, DS-0Ah~08h

These registers contain the DMA or Automatic PIO byte transfer count on the SCSI interface. STCNT0 is the least significant byte, STCNT1 is the mid byte, and STCNT2 is the most significant byte. If Initiator mode is enabled, it is loaded with the number of ACKs to send out on the SCSI bus. If Target mode is enabled, it is loaded with the number of REQs to send out on the SCSI bus. In Automatic PIO mode, STCNT is used as a counter only and need not be initialized to transfer data with Automatic PIO handshakes.

The counter counts down by one when a SCSI byte is transferred. When sending data to the bus, a byte is considered transferred when the appropriate handshake signal is received (REQ#/ACK#). When receiving data from the bus, a byte is considered transferred when it has been written to the data FIFO. Two counters are maintained for this purpose. The sense of DIRECTION (bit 2, DFCNTRL) which is latched by the last positive edge of SCSIEN determines which one is used.

SDONE (bit 2, SSTAT0) is set when the transfer count is zero.

STCNT2 R/W		STCNT1 R/W		STCNT0 R/W	
7	STCNT23	7	STCNT15	7	STCNT07
6	STCNT22	6	STCNT14	6	STCNT06
5	STCNT21	5	STCNT13	5	STCNT05
4	STCNT20	4	STCNT12	4	STCNT04
3	STCNT19	3	STCNT11	3	STCNT03
2	STCNT18	2	STCNT10	2	STCNT02
1	STCNT17	1	STCNT09	1	STCNT01
0	STCNT16	0	STCNT08	0	STCNT00

Clear SCSI Interrupt 0 (CLRSINT0)

Type:W
Address:M-0Bh, DS-0Bh

Writing a one to a bit in this register clears the associated SCSI interrupt bit in **SSTAT0**. Each bit is self-clearing and writing a zero to any bit in this register will have no effect.

	CLRSINT0 W
7	Not used
6	CLRSELDO
5	CLRSELDI
4	CLRSELINGO
3	CLRIOERR
2	RSVD
1	CLRSPIORDY
0	RSVD

Bit		Name	Definition
7	(w)	Not used	Undefined.
6	(w)	CLRSELDO	Clears the SELDO interrupt and status when is set to 1. No effect when zero is written. This bit is self-clearing.
5	(w)	CLRSELDI	Clears the SELDI interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
4	(w)	CLRSELINGO	Clears the SELINGO interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
3	(w)	CLRIOERR	Clears the IOERR bit in SSTAT0, which gets set when there's an operating mode (DIFFSENSE) change on the SCSI bus.
2	(w)	Not used	Undefined.
1	(w)	CLRSPIORDY	Clears SPIORDY interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
0	(w)	Not used	Undefined.

SCSI Status 0 (SSTAT0)

Type:R
Address:M-0Bh, DS-0Bh

This register contains the status of SCSI interrupt bits. Any status bit may be read at any time whether or not it has been enabled in **SIMODE0**. If an interrupt bit is enabled and set to one, the **SCSIINT** interrupt line will be driven to the active state except **TARGET** bit, which is a status bit only.

SSTAT0 R	
7	TARGET
6	SELDO
5	SELDI
4	SELINGO
3	IOERR
2	SDONE
1	SPIORDY
0	DMADONE

Bit			Name	Definition
7	(0)	(r)	TARGET	**Target.** When set this bit indicates that the SCSI module is in Target mode. The Target mode bit is set following successful completion of a Select detection or Reselection Out. The bit is cleared by bus free.
6	(0)	(r)	SELDO	**Select Out.** This bit is a one when you have successfully done a Select Out or Reselect Out sequence. TARGET will decide whether it was Select (TARGET=0) or Reselect (TARGET=1). It is cleared by a Bus Free condition or by setting CLRSELDO (bit 6,CLRSINT0). Interrupts may be enabled by setting ENSELDO (bit 6, SIMODE0) to one.
5	(0)	(r)	SELDI	**Select In.** This bit is a one when you have been selected or reselected. If TARGET is active, you have been selected, and if inactive, you have been reselected. It is cleared by a Bus Free condition or by setting CLRSELDI (bit 5, CLRSINT0). Interrupts may be enabled by setting ENSELDI (bit 5, SIMOED0) to one.
4	(0)	(r)	SELINGO	**Selecting Out.** After successful arbitration, this bit is set to one when you start the attempt to select or reselect another device. This interrupt is used to start looking for SELDO or bus time-out. When a successful selection has been completed (SELDO is one), this bit will be cleared. This bit may also be cleared by setting CLRSELINGO (bit 4, CLRSINT0).
3	(0)	(r)	IOERR	**I/O Error Status.** This bit will be a 1 if the I/O operating mode is changed. The Initial mode set, following a chip reset, does not cause this interrupt.

Bit			Name	Definition
2	(0)	(r)	SDONE	**SCSI DMA Done.** The SCSI DMA logic sets this to one when the DMA transfer of an SG segment is completed. It will be cleared when another SG segment is programmed, or by CLRCHANNEL.
1	(0)	(r)	SPIORDY	**SCSI PIO Ready.** When this bit is one, the Automatic SCSI PIO function has been enabled and data is ready or needed by the SCSI data transfer logic. As an Initiator, this bit is set to one on the leading edge of REQ. In Target mode, this bit is set on the leading edge of ACK. In both Initiator and Target mode, during a transfer to SCSI, the bit is cleared on a write to SCSIDATL. During a transfer from SCSI, it is cleared on a read from SCSIDATL. It may also be cleared by setting CLRSPIORDY (bit 1, CLRSINT0) or by clearing SPIOEN (bit 3, SXFRCTL0).
0	(0)	(r)	DMADONE	**DMA Done.** This bit is the logical AND of HDONE (bit 3, DFSTATUS) and SDONE. Warning: under the new-for-Bayonet "seamless" handling of SG segments, it is possible that host and SCSI could both be "done" at the same time, but be done with different segments. Bit 0 of the SG_CACHE_POINTER register indicates both are done with the LASTSEGMENT, and may be less misleading.

Clear SCSI Interrupt 1 (CLRSINT1)

Type:W
Address:M-0Ch, DS-0Ch

Writing a one to a bit in this register clears the associated SCSI interrupt bit in SSTAT1. Each bit is self-clearing and writing a zero to any bit in this register will have no effect.

CLRSINT1 W	
7	CLRSELTIMO
6	CLRATNO
5	CLRSCSIRSTI
4	RSVD
3	CLRBUSFREE
2	CLRSCSIPERR
1	CLRPHASECHG
0	CLRREQINIT

Bit		Name	Definition
7	(w)	CLRSELTIMO	Clears the SELTO interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
6	(w)	CLRATNO	In Initiator mode, clears the SCSI ATN bit if set by the sequencer or any automatic mode. ATN is also cleared by the Bus Free condition. In Target mode, clears ATNTARG interrupt and status. No effect when zero is written.This bit is self-clearing.
5	(w)	CLRSCSIRSTI	Clears SCSIRSTI interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
4	(w)	Not used	Undefined.
3	(w)	CLRBUSFREE	Clears BUSFREE interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
2	(w)	CLRSCSIPERR	Clears SCSIPERR interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
1	(w)	CLRPHASECHG	Clears PHASECHG interrupt and status when is set to 1. No effect when zero is written.This bit is self-clearing.
0	(w)	CLRREQINIT	See description of REQINIT bit for more details. CLRREQINIT clears REQINIT interrupt and status under some conditions.

SCSI Status 1 (SSTAT1)

Type:R
Address:M-0Ch, DS-0Ch

This register contains the status of SCSI interrupt bits. Any interrupt bit may be read at any time whether or not it has been enabled in SIMODE1. If enabled and set to one, it will cause the interrupt line to go to the active state. All are cleared by the corresponding bits in CLRSINT1 register (except PHASEMIS and SCSIPERR)

SSTAT1 R	
7	SELTO
6	ATNTARG
5	SCSIRSTI
4	PHASEMIS
3	BUSFREE
2	SCSIPERR
1	PHASECHG
0	REQINIT

Bit			Name	Definition
7	(0)	(r)	SELTO	**Selection Time-out.** This bit is set when the hardware selection timer is enabled and a Selection or Reselection time-out occurs. The timer is enabled by setting ENSTIMER (bit 2, SXFRCTL1) to one along with the time-out value in bits 3 and 4. The bit is cleared by setting CLRSELTIMO (bit 7, CLRSINT1) to one.
6	(0)	(r)	ATNTARG	**Attention Target.** This bit is set to one when you are a Target and the Initiator asserts ATN. It is latched and will be cleared when ATN is deasserted or when CLRATNO (bit 6, CLRSINT1) is set.
5	(0)	(r)	SCSIRSTI	**SCSI Reset In.**This bit is set to one when another device asserts RESET# on the SCSI bus. It remains set until cleared by writing a one to CLRSCSIRSTI (bit 5, CLRSINT1).
4	(0)	(r)	PHASEMIS	**Phase Mismatch.** Initiator mode only. This bit is set to one when the last phase on the SCSI bus sampled by REQ does not match the expected phase which is in the SCSISIGO register and the REQINIT (bit 0, SSTAT1) is set due to an incoming asynchronous REQ (see below). PHASEMIS can be cleared by writing the matching phase in SCSISIGO or by clearing REQINIT.
3	(0)	(r)	BUSFREE	**Bus Free.** This bit is set to one when the BSY and SEL signals have been negated on the SCSI bus for 400ns. This signal is latched and may be cleared by setting CLRBUSFREE in CLRSINT1 to one. This bit will be initially set to zero, but will reflect the state of the SCSI bus after 400ns.

Bit			Name	Definition
2	(0)	(r)	SCSIPERR	**SCSI Parity Error.** This bit is set to one when a parity error is detected on the incoming SCSI information transfer. Parity is sampled on the leading edge of REQ if in Initiator mode or the leading edge of ACK if in Target mode. If WIDEXFER in SXFRCTL0 is set, then parity will be checked on the upper byte of the SCSI bus during the Data phase only. If parity is enabled (ENSPCHK in SXFRCTL1 is set to one), a parity error will cause a one to be latched in this bit until cleared by writing one to CLRSCSIPERR in CLRSINT1. After writing to CLRSCSIPERR, this bit reflects the status of the parity of the last byte transferred on the bus. If ENSPCHK is set to zero, this bit will always be read as a zero.
1	(0)	(r)	PHASECHG	**SCSI Phase Change.** This bit is set to one when the phase on the SCSI bus changes to a phase that does not match the expected phase which is in the SCSISIGO register. It is not qualified with REQ. It can be cleared by writing a one to CLRPHASECHG in CLRSINT1.
0	(0)	(r)	REQINIT	**Request Initialized.** There are two distinct things that set this bit: ■ In Initiator mode, during asynchronous transfers (either DMA, automatic-PIO or manual) this bit is set by an incoming REQ and cleared by an outgoing ACK, or by an access to the SCSIDATL register with SPIOEN enabled (which is one way of generating an outgoing ACK). When the bit is set by an incoming asynchronous REQ, it may also be cleared using CLRREQINIT (bit 0, CLRSINT1). ■ REQINIT will also be true anytime the SCSI offset is non-zero in either Initiator or Target mode. The offset would be non-zero during a synchronous DMA transfer. Note that CLRREQINIT won't affect REQINIT when it's set because of the SCSI offset

SCSI Status 2 (SSTAT2)

Type:R

Address:M-0Dh, DS-0Dh

This register contains the status of SCSI module.

SSTAT2 R	
7	OVERRUN
6	SHVALID
5	WIDE_RES
4	EXP_ACTIVE
3	RSVD
2	RSVD
1	RSVD
0	RSVD

Bit			Name	Definition
7	(0)	(r)	OVERRUN	**Overrun Detect.** During synchronous transfers, this bit is set to one when an offset overrun is detected for Initiator mode only. An offset overrun is defined as the situation where the maximum offset programmed into SCSIOFFSET has been reached and another REQ is detected before an ACK is asserted on the SCSI bus. This status bit is cleared with CLRCHN (bit 1, SXFRCTL0).
6	(0)	(r)	SHVALID	**Shadow Valid.** This bit is 1 when the SCSI DMA transfer count (STCOUNT) is non-zero. This information is useful to initiator mode software at phase changes: it tells the software whether the shadow registers are worth saving or not.
5	(0)	(r)	WIDE_RES	**Wide Residue.** The SCSI DMA logic may set this bit between SG segments to indicate it's handling an "odd byte". This should not affect Initiator mode software, but may be used by Target mode software to determine whether it's safe to disconnect between SG segments. See Functional Description section for additional details.
4	(0)	(r)	EXP_ACTIVE	**SCSI Expander Active.** Allows software to see the level of the AIC-7890A/91 EXPACT input pin. The intended use is to see, when AIC-7890A/91 is communicating with a SCSI device, whether the SCSI device is on the other side of an AIC-3860 SCSI expander chip
3-0	(0)	(r)	RSVD	Always read 0.

SCSI Status 3 (SSTAT3)

Type:R
Address:M-0Eh, DS-0Eh

This register is the status of the current Synchronous SCSI Offset count. *This register must not be read while SCSI DMA transfers are in progress.* Doing so would result in spurious results and possibly in parity errors on the **CIOBUS**. The offset status during DMA transfers may be tracked to some extent via the **REQINIT** bit in **SSTAT1**, which will be 1 anytime the offset is non-zero.

SSTAT3 R	
7	RSVD
6	OFFCNT6
5	OFFCNT5
4	OFFCNT4
3	OFFCNT3
2	OFFCNT2
1	OFFCNT1
0	OFFCNT0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6-0	(0)	(r/w)	OFFCNT[6:0]	**SCSI Offset Count [6:0].** Gives the current SCSI offset count. Do not read this counter unless DMA transfers are stopped.

SCSI ID (SCSIID)

Type:R/W
Address:M-0Fh, DS-0Fh

This register contains the devices own ID (**OID**) and the ID of the SCSI device that you want to communicate with (**TID**). The value in **OID** is also our target I.D. if selection in is enabled (**ENSELI** set). The module may be programmed to respond to more than 1 target I.D. See *Target ID High/Low (TARGIDH, TARGIDL)* on page 4-89 for a description of this multi-target I.D. option.

SCSIID R/W	
7	TID3
6	TID2
5	TID1
4	TID0
3	OID3
2	OID2
1	OID1
0	OID0

Bit			Name	Definition
7-4	(0)	(r/w)	TID[3:0]	**Target (Other) ID**. This is a binary representation of the other device ID on the SCSI bus during a Selection/Reselection sequence performed by the AIC-7890A/91. It is the Target ID during Selection Out (ENSELO=1, TEMODEO=0). It is the Initiator ID during Reselection Out (ENSELO, TEMODEO=1). In any case, it is *the other ID.*
3-0	(0)	(r/w)	OID[3:0]	**Own ID.** This is a binary representation of the AIC-7890A/91 ID on the SCSI bus during any Selection/Reselection sequence. It is the AIC-7890A/91 Initiator ID during Selection Out (ENSELO=1, TEMODEO=0) and Reselection In (ENRSELI). It is the AIC-7890A/91 Target ID during Selection In (ENSELI) and Reselection Out (ENSELO, TEMODEO=1). In any case, it is the AIC-7890A/91 *ID.*

SCSI Interrupt Mode 0 (SIMODE0)

Type:R/W
Address:M-10h, DS-10h

Setting any bit will enable the corresponding function in **SSTAT0** to interrupt via the IRQA# pin.

SIMODE0 R/W	
7	ENSCAMSELD
6	ENSELDO
5	ENSELDI
4	ENSELINGO
3	ENIOERR
2	ENSDONE
1	ENSPIORDY
0	ENDMADONE

Bit			Name	Definition
7	(0)	(r/w)	ENSCAMSELD	Enables SCAMSELD to assert SCSIINT.
6	(0)	(r/w)	ENSELDO	Enables SELDO status to assert SCSIINT.
5	(0)	(r/w)	ENSELDI	Enables SELDI status to assert SCSIINT.
4	(0)	(r/w)	ENSELINGO	Enables SELINGO status to assert SCSIINT.
3	(0)	(r/w)	ENIOERR	Enables IOERR status to assert SCSIINT.
2	(0)	(r/w)	ENSDONE	Enables SDONE status to assert SCSIINT.
1	(0)	(r/w)	ENSPIORDY	Enables SPIORDY status to assert SCSIINT.
0	(0)	(r/w)	ENDMADONE	Enables DMADONE status to assert SCSIINT.

SCSI Interrupt Mode 1 (SIMODE1)

Type:R/W
Address:M-11h, DS-11h

Setting any bit will enable the corresponding function in SIMODE1 to interrupt via the IRQA# pin.

SIMODE1 R/W	
7	ENSELTIMO
6	ENATNTARG
5	ENSCSIRST
4	ENPHASEMIS
3	ENBUSFREE
2	ENSCSIPERR
1	ENPHASECHG
0	ENREQINIT

Bit			Name	Definition
7	(0)	(r/w)	ENSELTIMO	Enables the SELTO status to assert SCSIINT.
6	(0)	(r/w)	ENATNTARG	Enables ATNTARG status to assert SCSIINT.
5	(0)	(r/w)	ENSCSIRST	Enables SCSIRST status to assert SCSIINT.
4	(0)	(r/w)	ENPHASEMIS	Enables PHASEMIS status to assert SCSIINT.
3	(0)	(r/w)	ENBUSFREE	Enables BUSFREE status to assert SCSIINT.
2	(0)	(r/w)	ENSCSIPERR	Enables the latched SCSIPERR status to assert SCSIINT.
1	(0)	(r/w)	ENPHASECHG	Enables PHASECHG status to assert SCSIINT.
0	(0)	(r/w)	ENREQINIT	Enables REQINIT status to assert SCSIINT.

SCSI Data Bus (SCSIBUSH, SCSIBUSL)

Type:R/W
Address:M-13h~12h, DS-13h~12h

This register provides direct access to the SCSI data bus. During a read operation data is gated from the SCSI data bus to the internal data bus, the data is not latched. During write operations any data written to these addresses are actually written to the **SCSIDAT** register pair at addresses 06h and 07h. This register pair is used to transfer data between to chip and the SCSI data bus during SCAM operations.

SCSIBUSH R/W		SCSIBUSL R/W	
7	SDB15	7	SDB07
6	SDB14	6	SDB06
5	SDB13	5	SDB05
4	SDB12	4	SDB04
3	SDB11	3	SDB03
2	SDB10	2	SDB02
1	SDB09	1	SDB01
0	SDB08	0	SDB00

Shadow Host Address (SHADDR[7:0])

Type:R
Address:M-17h~14h, DS-17h~14h

The SCSI module contains an 8-byte address counter for "shadowing" the host (PCI) address that is being transferred to or from during DMA operation (SHADDR). These 8 bytes are read here. At the addresses stated, the high or low 4 bytes of SHADDR are read according to the HADDRSEL[1:0] field in the HST module DSCOMMAND1 register: if HADDRSEL = 00 then SHADDR[3:0] are read, if HADDRSEL = 01 then SHADDR[7:4] are read.

These bytes are not directly writable. This counter is loaded by the preload circuit during DMA operations. The SHADDR registers must not be read while SCSI DMA is enabled.

SHADDR3 R		SHADDR2 R		SHADDR1 R		SHADDR0 R	
7	SHADDR31	7	SHADDR23	7	SHADDR15	7	SHADDR07
6	SHADDR30	6	SHADDR22	6	SHADDR14	6	SHADDR06
5	SHADDR29	5	SHADDR21	5	SHADDR13	5	SHADDR05
4	SHADDR28	4	SHADDR20	4	SHADDR12	4	SHADDR04
3	SHADDR27	3	SHADDR19	3	SHADDR11	3	SHADDR03
2	SHADDR26	2	SHADDR18	2	SHADDR10	2	SHADDR02
1	SHADDR25	1	SHADDR17	1	SHADDR09	1	SHADDR01
0	SHADDR24	0	SHADDR16	0	SHADDR08	0	SHADDR00

SHADDR7 R		SHADDR6 R		SHADDR5 R		SHADDR4 R	
7	SHADDR63	7	SHADDR55	7	SHADDR47	7	SHADDR39
6	SHADDR62	6	SHADDR54	6	SHADDR46	6	SHADDR38
5	SHADDR61	5	SHADDR53	5	SHADDR45	5	SHADDR37
4	SHADDR60	4	SHADDR52	4	SHADDR44	4	SHADDR36
3	SHADDR59	3	SHADDR51	3	SHADDR43	3	SHADDR35
2	SHADDR58	2	SHADDR50	2	SHADDR42	2	SHADDR34
1	SHADDR57	1	SHADDR49	1	SHADDR41	1	SHADDR33
0	SHADDR56	0	SHADDR48	0	SHADDR40	0	SHADDR32

Target ID In (TARGIDIN)

Type:R
Address:M-18h, DS-18h

The **CLKOUT** signal is used by software doing direct SCAM to provide a time tick.

The **TARGID[3:0]** is required for the multiple target ID support, it tells which one of the target IDs AIC-7890A/91 was selected as the target.

TARGIDIN R	
7	CLKOUT
6	RSVD
5	RSVD
4	RSVD
3	TARGID3
2	TARGID2
1	TARGID1
0	TARGID0

Bit			Name	Definition
7	(0)	(r)	CLKOUT	**Clock Out.** A free-running timer provided for the software driver to use when performing SCAM protocol. The frequency is determined by the CLKIN source (40 MHz) divided to provide a 102.40 µs period. The default value of "1" indicated is true while the chip is being reset and for 51.2usec thereafter.
6-4	(0)	(r)	RSVD	Always reads 0.
3-0	(0)	(r)	TARGID [3:0]	The hex value in this field is the SCSI target I.D. present on the SCSI bus during a valid SELECT operation detected by the SCSI module. The field is set when the module asserts BSY claiming control of the bus. The field is cleared by PCIRST#, CHIPRST, or bus free.

Selection/Reselection ID (SELID)

Type:R
Address:M-19h, DS-19h

This register contains the SCSI ID of the selecting or reselecting device which was asserted during the last Selection/Reselection SCSI bus phase. AIC-7890A/91's own device ID and decode the remaining ID. After a Selection/Reselection in has taken place, the ID may be read from this register to determine the ID of the device which initiated the Selection/Reselection. If a selection occurred by a SCSI device which did not set its own ID, then ONEBIT will be set to indicate that condition. If ONEBIT is zero, then 2 bits were active on the SCSI bus

SELID R	
7	SELID3
6	SELID2
5	SELID1
4	SELID0
3	ONEBIT
2	RSVD
1	RSVD
0	RSVD

Bit			Name	Definition
7-4	(0)	(r)	SELID(3:0)	**Selection ID.** This is the ID of the selecting or reselecting SCSI device.
3	(0)	(r)	ONEBIT	This bit is set when only one bit is detected on the SCSI bus during Selection. It is zero when 2 bits are detected during a Selection.
2-0	(0)	(r)	RSVD	Always reads 0.

SCAM Control (SCAMCTL)

Type:W
Address:M-1Ah, DS-1Ah

This register controls semi-automatic level 1 and level 2 SCAM operations.

SCAMCTL W	
7	ENSCAMSELO
6	CLRSCAMSELD
5	ALTSTIM
4	DFLTID
3	Not used
2	Not used
1	SCAMLVL1
0	SCAMLVL0

Bit		Name	Definition
7	(w)	ENSCAMSELO	**Enable SCAM Selection Out.** When set, this bit causes the SCAM logic to begin a SCAM initiation sequence as an initiator. The logic will automatically arbitrate for control of the SCSI bus, perform a SCAM selection, and initiate the SCAM protocol. The Selection Timeout Delay counter provides the SCAM selection delay during the SCAM select phase. This bit is held clear if SCAMLVL(1:0) = 0.
6	(w)	CLRSCAMSELD	**Clear SCAM Selection Done.** When this bit is set it will allow the next bus free phase to clear the SCAMSELD status bit. The ENSCAMSELO bit should be cleared before the status is cleared to prevent an unintended second SCAM selection.
5	(w)	ALTSTIM	**Alternate Selection Timeout.** When this bit is set it changes the meaning of the Selection Timeout values encoded in the STIMESEL field in the SXFRCTL1 register, a 0 here leaves the original encoding unchanged. These alternate timeout values support the fast selection cycles used during SCAM/SCAM tolerant bus scan.This bit is held clear if SCAMLVL(1:0) = 0.
4	(w)	DFLTID	**Default SCSI ID.** Software sets this if the module is supporting SCAM level 2 operations to indicate that we do not have a definite I.D. assigned to us (Initiator soft I.D. option). If set it will disable our Initiator I.D. output to the SCSI bus during arbitrations. DFLTID set and the SCAMLVL field = 2 also delays the modules response to selections to approximately 4.1 msec.
3-2	(w)	Not used	Undefined.

Bit		Name	Definition
1-0	(w)	SCAMLVL [1:0]	**SCAM Level.** The value in this 2 bit field controls determines the type of SCAM support provided by hardware in the SCSI module. The support modes are described below:

Value	Description
0	All automatic support is disabled, the upper 4 bits in this register are held in reset when SCAMLVL = 0. Only software direct SCAM facilities (controlled by SCAMEN bit in SXFRCTL1) are operable.
1	SCAM level 1 support is provided by the upper three bits in this register. SCAM protocol may be initiated and the ALTSTIM alternate time-outs are available. The module will not detect a SCAM selection initiated by another SCSI device and soft Initiator I.D. are not supported. The DFLTID bit is held reset when SCAMLVL =1.
2	SCAM level 2 is supported by hardware controlled by the upper four bits in this register. SCAMLVL = 2 enabled the DFLTID bit and SCAM select detection.
3	Reserved for future use.

SCAM Status (SCAMSTAT)

Type:R
Address:M-1Ah, DS-1Ah

This register provides status information needed by software to implement semi-automatic SCAM level 1 and 2 support. If **SCAMLVL[1:0]** = 0 all bits in this register will read 0.

	SCAMSTAT R
7	SCAMSELOSTAT
6	SCAMSELD
5	ALTSTIM
4	DFLTID
3	RSVD
2	RSVD
1	SCAMLVL1
0	SCAMLVL0

Bit			Name	Definition
7	(0)	(r)	SCAMSELOSTAT	**SCAM Selection Out Status.** This bit reflects the state of the ENSCAMSEL0 control bit in SCAMCTL.
6	(0)	(r)	SCAMSELD	**SCAM Selection Done.** This bit is set when a SCAM selection has been successfully completed. If SCAM 1 support is enabled it indicates that a SCAM select initiated by this module is complete. If SCAM 2 is set then the CAM selection may have been initiated by another device on the bus. The SCSI interrupt output is asserted when this bit is true. There is no mask for this interrupt.
5	(0)	(r)	ALTSTIM	**Alternate Selection Timeout.** This bit reflects the state of the ALSTIM bit in SCAMCTL.
4	(0)	(r)	DFLTID	**Default SCSI I.D.** This bit reflects the state of the ALSTIM bit in SCAMCTL.
3-2	(0)	(r)	RSVD	Always reads 0.
1-0	(0)	(r)	SCAMLVL[1:0]	**SCAM Level.** This bit reflects the state of the SCAMLVL bits in SCAMCTL.

Target ID High/Low (TARGIDH, TARGIDL)

Type:R/W
Address:M-1Ch~1Bh, DS-1Ch~1Bh

This register pair supports the multi target ID feature. Software will load this register pair with a bit map of the SCSI target IDs that the module should recognize. For example if we wish to respond to SCSI target IDs 3, 7, 8, and 9 then the software should write to TARGIDL with bits 3 and 7 true and to TARGIDH with bits 8 and 9 true. Following a valid select in phase the software may determine which ID the module responded to by reading the contents of the TARGIDIN register, the target ID will be encoded in the lower 4 bits.

The contents of this register pair is used only for Selection In decoding. To perform a reselection out as a target the desired target ID must be written to the OID field of the SCSIID register.

TARGIDH,TARGIDL R/W	
7	CLKOUT
6	RSVD
5	RSVD
4	RSVD
3	TARGID3
2	TARGID2
1	TARGID1
0	TARGID0

Bit			Name	Definition
7	(0)	(r)	CLKOUT	**Clock Out.** A free-running timer provided for the software driver to use when performing SCAM protocol. The frequency is determined by the CLKIN source (40 MHz) divided to provide a 102.40 µs period. The default value of "1" is true while the chip is being reset and for 51.2usec thereafter.
6-4	(0)	(r)	RSVD	Always reads 0.
3-0	(0)	(r)	TARGID [3:0]	The hex value in this field is the SCSI target ID present on the SCSI bus during a valid SELECT operation when detected by the AIC-7890A/91. The field is set when the AIC-7890A/91 asserts BSY claiming control of the bus. The field is cleared by PCIRST#, CHIPRST, or bus free.

Board Control (BRDCTL)

Type:R/W
Address:M-1Dh, DS-1Dh

The Board Control register provides the capability to control reading and writing of external device(s) interconnected to the AIC-7890A/91's FLEX Port which may be shared with an SRAM, ROM/EEPROM and SEEPROM. The timing provided to the external devices is a function of a software routine that matches the device's timing. The SEECTL bits as indicated may also be used for board logic control if desired.

BRDCTL R/W	
7	BRDDAT7
6	BRDDAT6
5	BRDDAT5
4	BRDDAT4
3	BRDDAT3
2	BRDDAT2
1	BRDRW
0	BRDSTB

Bit			Name	Definition
7-2	(0)	(r/w)	BRDDAT[7:2]	**Board Data [7:2].** Bits are read/write data bits which BRDDAT[7:3]are only connected to MD[7:3] and BRDDAT2 is connected to MDP when SEEMS is active and EXTARBACK# is asserted. These bits are write bits when BRDRW is inactive (=0) and their written value will be driven on MD[7:3] and MDP pins. These bits are read bits when BRDRW is active and the values read will be those present on MD[7:3] and MDP pins.
1	(0)	(r/w)	BRDRW	**Board Read/Write.** This read/write bit combined with BRDSTB bit controls the output state of BRDOE# and BRDWE pins when SEEMS is active and EXTARBACK# is asserted. See the equations below. The state of BRDRW also controls the data direction of BRDDAT[7:2], when BRDRW is inactive (=0) BRDDAT[7:2] are outputs.
0	(0)	(r/w)	BRDSTB	**Board Strobe.** This read/write bit combined with BRDRW bit controls the output state of BRDOE# and BRDWE pins when SEEMS is active and EXTARBACK# is asserted. See the equations below.

BRDWE = !BRDRW & BRDSTB;

BRDOE# = !BRDRW;

Serial EEPROM Control (SEECTL)

Type:R/W
Address:M-1Eh, DS-1Eh

The Serial EEPROM Control register provides the capability to control reading and writing an external serial 1-bit EEPROM device that contains a 4-pin interface (typical devices are NM93C06/C46/C56/C66). The SEEPROM is interconnected to the AIC-7890A/91's FLEX Port which may be shared with an SRAM, a ROM/FLASH EPROM and board logic devices. The timing required by the external SEEPROM is a function of a software routine that matches the device's timing. Due to the slow clock rate, typically 1MHz maximum, a hardware timer is provided that may be accessed to ease software development and provide portability.

SEECTL R/W	
7	EXTARBACK
6	EXTARBREQ
5	SEEMS
4	SEERDY
3	SEECS
2	SEECK
1	SEEDO
0	SEEDI

Bit			Name	Definition
7	1	(r)	EXTARBACK	**External Arbitration Acknowledge.** This read only bit enables the sequencer or host driver to determine the external level of input pin EXTARBACK#. See *FLEXPort Interface* on page 3-20 for additional information. EXTARBACK# contains a weak internal pull-up and depending on the application may require an external pull-up resistor.
6	(0)	(r)	EXTARBREQ	**External Arbitration Request.** This read only bit enables the sequencer or host driver to determine the level of output pin EXTARBREQ#. See *FLEXPort Interface* on page 3-20 for additional information. EXTARBREQ# requires an external pull-up resistor for multi-user applications.

Bit			Name	Definition
5	(0)	(r/w)	SEEMS	**Serial EEPROM Mode Select.** This read/write bit when active (=1) generates a request to the FLEX Port for access to the external SEEPROM/board logic devices. When the FLEX Port is not busy servicing another request, sequencer/host to SRAM or host to ROM/EEPROM, then SEEMS active will cause EXTARBREQ# to be asserted. When EXTARBACK# becomes asserted in response to EXTARBREQ# assertion, then the FLEX Port is re-configured to allow SEECTL bits to control MD[2:0] and SEECS for the SEEPROM/board logic device access. **Note:** Once EXTARBACK# is asserted so that the AIC-7890A/91 drives the FLEX Port, no other device may gain access to the external devices until SEEMS is inactive. Prior to beginning the external access process verify that the FLEX Port access has been granted by sampling SEERDY active after a write to set SEEMS active.
4	(0)	(r)	SEERDY	**Serial EEPROM Ready.** This read only bit provides a hardware timer that may be used instead of a software timer when accessing the external SEEPROM/board logic devices. Each time the SEECTL register is written to, SEERDY will become inactive and after an 800 ns delay will become active (=1). In addition, SEERDY provides the initial indication that the FLEX Port arbitration has been completed following setting SEEMS active. In this case SEERDY will not become active after the normal 800 ns time-out, but will stay inactive until EXTARBACK# is sampled asserted in response to EXTARBREQ# being asserted as a result of SEEMS being active. **Note:** The FLEXPort outputs will not become driven until EXTARBACK# is asserted after SEEMS is set active. The access acknowledge and independent timing are the only hardware function performed by SEERDY.
3	(0)	(r/w)	SEECS	**Serial EEPROM Chip Select.** This read/write bit is used to control the AIC-7890A/91 output SEECS. The SEECS bit being active (=1) can only assert the AIC-7890A/91 output SEECS when SEEMS is active and has completed arbitration for FLEX Port use. SEECS is also used with the BRDCTL register when both SEEPROM and board logic devices are present. SEECS requires an external pull-down resistor.
2	(0)	(r/w)	SEECK	**Serial EEPROM Clock.** This read/write bit controls the state of MD2 which is connected to the shift clock input of the SEEPROM. When SEECK and SEEMS are active (=1), MD2 will be at a high level. This bit may also be utilized for board logic devices as an output.

Bit			Name	Definition
1	(0)	(r/w)	SEEDO	**Serial EEPROM Data Out.** This read/write bit controls the state of MD1 which is connected to the data input of the SEEPROM. When SEEDO and SEEMS are active (+1), MD1 will be at a high level for writing a 1 bit into the EEPROM. This bit may also be utilized for board logic devices as an output.
0	[2]	(r)	SEEDI	**Serial EEPROM Data In.** This read only bit is used to access data from the SEEPROM. Its value reflects the value of MD0 which is connected to the data output of the SEEPROM and SEEMS is active. This bit may also be utilized for board logic devices as an input.

[1] Level is sampled by reset, EXTARBACK# is expected to be high for multi-user configurations and low for single user configuration.

[2] Level following reset is expected to be high when an external pull-up is provided otherwise unknown.

SCSI Block Control (SBLKCTL)

Type:R/W
Address:M-1Fh, DS-1Fh

This register controls the hardware selection options outside of the SCSI cells. This control includes address decodes and data multiplexing.

SBLKCTL R/W	
7	DIAGLEDEN
6	DIAGLEDON
5	AUTOFLUSHDIS
4	RSVD
3	ENAB40
2	ENAB20
1	SELWIDE
0	XCVR

Bit			Name	Definition
7	(1)	(r/w)	DIAGLEDEN	**Diagnostic LED Enable.** When this bit is active (=1), the LED# assertion output state reflects the state of the DIAGLEDON bit, except during and after PCIRST# assertion. During and immediately after PCIRST# assertion when the LED output is used for clocking in IDDAT, see section on IDDAT. When DIAGLEDEN bit is not active (normal operation), the LED# assertion output state reflects the OR result of active bits SELINGO, SELDI and SELDO in the SSTAT0 register.
6	(1)	(r/w)	DIAGLEDON	**Diagnostic LED On.** When this bit is active (=1) and DIAGLEDEN is active, the LED# output will be asserted. When this bit is inactive and DIAGLEDEN is active, the LED# output will not be asserted. When DIAGLEDEN is inactive, the state of DIAGLEDON has no effect on the assertion state of LED#. The use of DIAGLEDEN and DIAGLEDON provide a diagnostic capability where the assertion state of LED# may be used for an external trigger for occurrence of internal events.

Bit			Name	Definition
5	(0)	(r/w)	AUTOFLUSHDIS	**Auto Flush Disable.** Normally, when SCSI has been doing a DMA transfer into the data FIFO and it becomes apparent that no more data will be written to the data FIFO (due to completion of the transfer or a phase change on the SCSI bus), the SCSI module sends an "autoflush" signal to the HOST indicating that it should do transfers to flush the FIFO without waiting for any FIFO threshold conditions to be met. However, the auto-flush can be disabled by setting this bit.
4	(0)	(r)	RSVD	Always reads 0.
3	(0)	(r)	ENAB40	**Enable 40 Mtransfer Mode** This bit will be one if the SCSI I/O controls have enabled LVD or SCSI I/O option. The bit will be 0 if either the single ended or HVD option is enabled or if SCSI I/O is disabled.
2	(0)	(r)	ENAB20	**Enable 20 Mtransfer Mode** This bit will be one if the SCSI I/O controls have enabled the single ended or the High Voltage DIfferential I/O option. The bit will be 0 if the Low Voltage differential option is enabled or if SCSI I/O is disabled. If this bit is set the software should not negotiate for a data rate above 20 Mtransfers/sec.
1	(*)	(r/w)	SELWIDE	**Select Wide.** When this bit is set, the internals of the device are configured for one 16-bit Wide SCSI channel with the control lines for the one 8-bit channel (not wide selection) used for phase detection and transfer control of data (SCD[15:8]# with SCDPH# and SCD[7:0]# with SCDPL#). It is expected that the external bus is Wide when SELWIDE is enabled. When this bit is cleared, the device is configured for one 8-bit channel using only SCD[7:0]# and SCDPL#, with SCD[15:08]# and SCDPH# not used. When the device is configured for one 8-bit channel the I/O inputs SCD[15:08]# and SCDPH# are internally terminated so that external termination is not required. **Note:** (*) SELWIDE may be initialized at chip reset to indicate the hardware connection to the WIDEPS# input. When WIDEPS# is deasserted, SELWIDE will be cleared. When WIDEPS# is asserted, it indicates a wide connection and SELWIDE will be set. After this chip reset initialization SELWIDE may be written to either state when desired.
0	(*)	(r/w)	XCVR	**External Transceiver** This bit will be 1 if the EXTXCVR# pin is low indicating the presence of external SCSI transceivers. This bit will be 0 if the EXTXCVR# pin is high.

If both **ENAB20** and **ENAB40** are read 0, then the SCSI I/O logic has disabled all SCSI I/O drivers. If an IOERR interrupt has occurred, then the software should check these two bits to see if SCSI transfer rates should be re-negotiated.

Sequencer Control (SEQCTL)

Type:R/W
Address:M-60h, DS-60h

This register selects the Sequencer operating features. Some features affect the operation of other logic blocks in AIC-7890A/91.

SEQCTL R/W	
7	PERRORDIS
6	PAUSEDIS
5	FAILDIS
4	FASTMODE
3	BRKADRINTEN
2	STEP
1	SEQRESET
0	LOADRAM

Bit			Name	Definition
7	(1)	(r/w)	PERRORDIS	**Parity Error Disable.** When cleared, allows Sequencer instruction RAM parity errors to be detected. When set, disables parity error detection.
6	(0)	(r/w)	PAUSEDIS	**PAUSEDIS.** If set, disables the Pause function when PAUSE (bit 2, HCNTRL) is set. Pause due to interrupts or error conditions is still enabled. SCSI interrupts, an illegal opcode interrupt, or a sequencer RAM parity error interrupt resets this bit. Host software may not write to this bit.
5	(1)	(r/w)	FAILDIS	**Fail Disable.** When set, disables Instruction RAM parity and Illegal Opcode detection from latch-pausing the Sequencer. When cleared, the detection of an instruction RAM parity or Illegal OPcode will cause the Sequencer to be latch-paused. The state of FAILDIS is also used by other modules to modify their action to error conditions.
4	(0)	(r/w)	FASTMODE	**FASTMODE.** When cleared, all sequencer instructions default to a 10 MIPS instruction cycle speed. If set to one, then all instruction execution cycles are at 20 MIPS.
3	(0)	(r/w)	BRKADRINTEN	**Break Address Interrupt Enable.** When set, the breakpoint status is enabled to drive the interrupt pin. When cleared and the breakpoint is enabled (clear BRKDIS in BRKADDR1), BRKADRINT (bit3, INTSTAT) will be set, but IRQA# will not be asserted.

Bit			Name	Definition
2	(0)	(r/w)	STEP	**Step.** When set, the Sequencer when unpaused will execute one instruction and then self-pause. This bit will normally be set and cleared by the software driver for diagnostic purposes. Multiple single steps may be done by clearing PAUSE multiple times. Should the Sequencer set this bit it will be paused and require HIM service to clear it before the Sequencer may continue.
1	(0)	(r/w)	SEQRESET	**Sequencer RAM Address Reset.** When set, the address pointer for the instruction RAM is cleared, and then the Sequencer instruction at location zero is loaded into the Sequencer instruction register. When the sequencer is unpaused, program execution starts with this instruction. This bit is self-clearing. The Sequencer must be paused before setting this bit.
0	(0)	(r/w)	LOADRAM	**Load RAM.** When set, allows instructions to be loaded into or read from the Sequencer instruction RAM. Note, each instruction is 32-bit wide which requires four bytes to be written or read for each instruction. The Sequencer must be paused before setting this bit. PAUSEACK cannot be cleared by clearing PAUSE while LOADRAM is set. LOADRAM, and PAUSE bits must be cleared for the Sequencer to operation. Should the Sequencer set this bit it will be paused and require HIM service to clear it before the Sequencer may continue.

Sequencer RAM Data (SEQRAM)

Type:R/W
Address:M-61h, DS-61h

This register operates as a data port to the instruction RAM (space for 768 instructions x 32-bits). Instruction data may be written or read by first writing to set the LOADRAM bit in SEQCTL. Then writing the desired starting instruction address in SEQADDR. Each instruction access requires four bytes to be transferred. The byte ordering is from the least significant byte SEQRAM[7:0] to the most significant SEQRAM[31:24]. The most significant bit of the most significant byte contains the odd-parity for the instruction. The address will be auto-incremented after the most significant byte is accessed.

The parity of the instruction in the Sequencer RAM is checked when executed. When PERRORDIS and FAILDIS are cleared, detected SEQRAM parity errors will cause the Sequencer to be latch paused with PAUSE set in the HCNTRL register, and SQPARERR set in the ERROR register. When FAILDIS is cleared, detected ILLOPCODE errors will cause the Sequencer to be latch paused with PAUSE set in the HCNTRL register, and ILLOPCODE set in the ERROR register. Both of these errors are latched in the Sequencer and require LOADRAM to be set to clear them.

SEQRAM R/W	
7	SEQRAM07
6	SEQRAM06
5	SEQRAM05
4	SEQRAM04
3	SEQRAM03
2	SEQRAM02
1	SEQRAM01
0	SEQRAM00

Sequencer RAM Address (SEQADDR[1:0])

Type:R/W
Address:M-63h~62h, DS-63h~62h.

These registers contain the address of the sequencer RAM location that will be executed on the next instruction cycle. They may be written to for the purpose of changing the address execution location in the instruction RAM. They are also used to specify the starting location when loading the program. The address will automatically increment while loading the program after every fourth byte. **SEQADDR is** cleared to 0h by **PCIRST#, CHIPRST** or writing a 1h to **SEQRESET**.

SEQADDR1 R/W		SEQADDR0 R/W	
7	RSVD	7	SEQADDR07
6	RSVD	6	SEQADDR06
5	RSVD	5	SEQADDR05
4	RSVD	4	SEQADDR04
3	RSVD	3	SEQADDR03
2	RSVD	2	SEQADDR02
1	SEQADDR09	1	SEQADDR01
0	SEQADDR08	0	SEQADDR00

Bit			Name	Definition
7-2	(0)	(r)	RSVD	Always read 0.
1-0	(0)	(r/w)	SEQADDR[9:8]	**SEQ instruction SRAM address register.** Contains the address pointer to the desired instruction in the Sequencer SRAM

Bit			Name	Definition
7-0	(0)	(r/w)	SEQADDR[7:0]	**SEQ instruction SRAM address register.** Contains the address pointer to the desired instruction in the Sequencer SRAM

Accumulator (ACCUM)

Type:R/W
Address:M-64h, DS-64h

This register is a temporary holding place for arithmetic or logical operations. The contents of ACCUM are used in place of the Immediate field in the instruction when the Immediate field value is 0. When specified as the destination, it is loaded by the output of the ALU. When not specified as the destination, Accumulator is not altered by the instruction execution. When specified as a source, it is read like any other source register. But in addition, ACCUM is the only register that can be implicitly accessed as a source in the same instruction that a different register is explicitly specified as a source by the Source Address field.

ACCUM R/W	
7	ACCUM07
6	ACCUM06
5	ACCUM05
4	ACCUM04
3	ACCUM03
2	ACCUM02
1	ACCUM01
0	ACCUM00

Bit			Name	Definition
7-0	(0)	(r/w)	ACCUM[07:00]	**Accumulator.** Contains the result of the selected previous instruction operation.

Source Index Register (SINDEX)

Type:R/W
Address:M-65h, DS-65h

This register is a default destination register, a temporary holding register or may be used as an indirect address for source operands for Sequencer instructions. It will increment by 1 for each data transfer. When SINDEX is addressing a data port SINDEX will not increment. Increment by 1 is determined by any address value (odd/even) or the use of an ALU instruction.

SINDEX will be updated, as the default destination, for ALU instructions (JUM, JC, JNC, CALL) where SINDEX is the default destination of the instruction result and the destination address bus will also default to the NONE register address (the instruction field for these instructions contains the next instruction address instead of the destination address).

SINDEX may be read or written alone with a separate instruction to set its desired state.

SINDEX R/W	
7	SINDEX07
6	SINDEX06
5	SINDEX05
4	SINDEX04
3	SINDEX03
2	SINDEX02
1	SINDEX01
0	SINDEX00

Bit			Name	Definition
7-0	(0)	(r/w)	SINDEX[07:00]	Source Index 0 register.

Destination Index Register (DINDEX)

Type:R/W
Address:M-66h, DS-66h

This register is a temporary holding register or may be used as an indirect address for destination operands for Sequencer instructions. It will increment by 1 for each data transfer. When DINDEX is addressing a data port DINDEX will not increment. Increment by 1 is determined by any address value (odd/even) or the use of an ALU instruction. DINDEX may be read or written alone with a separate instruction to set its desired state.

DINDEX R/W	
7	DINDEX07
6	DINDEX06
5	DINDEX05
4	DINDEX04
3	DINDEX03
2	DINDEX02
1	DINDEX01
0	DINDEX00

Bit			Name	Definition
7-0	(0)	(r/w)	DINDEX[07:00]	Destination Index 0.

Break Address 0 (BRKADDR0)

Type:R/W
Address:M-67h, DS-67h

This register is used for diagnostic purposes to halt the sequencer at a specific address. It is loaded with the lower byte of the desired break address. **BRKADDR0** is cleared to 0h by **PCIRST#** or **CHIPRST. BRKDIS** in **BRKADDR1** register must be cleared for the function to operate.

BRKADDR0 may be read or written alone with a separate instruction to set its desired state. Care must be taken to ensure merged functions in **BRKADDR1** are properly controlled.

BRKADDR0 R/W	
7	BRKADDR07
6	BRKADDR06
5	BRKADDR05
4	BRKADDR04
3	BRKADDR03
2	BRKADDR02
1	BRKADDR01
0	BRKADDR00

Bit			Name	Definition
7-0	(0)	(r/w)	BRKADDR[07:00]	**Break Address[07:00].** The low byte of break address.

Break Address 1 (BRKADDR1)

Type:R/W
Address:M-68h, DS-68h

This register is used for diagnostic purposes to halt the sequencer at a specific address. It is loaded with the high bits of the desired break address. In addition, bit 7 is a break address function disable which must be cleared for the function to operate. Bits 6:4 Control the RAM BIST function of the sequencer SEQRAM. BRKADDR1 is cleared to 80h by PCIRST# or CHIPRST.

BRKADDR1 R/W	
7	BRKDIS
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	BRKADDR09
0	BRKADDR08

Bit			Name	Definition
7	(1)	(r/w)	BRKDIS	**Break Address Function Disable.** When set, the Sequencer does not halt at the break address.
6-2	(0)	(r)	RSVD	Always reads 0.
1-0	(0)	(r/w)	BRKADDR[09:08]	**Break Address[09:08].** The upper 2 bits of the break address.

All Ones (ALLONES)

Type:R
Address:M-69h, DS-69h

This data port returns all ones as data when read. It may be used for certain logical, arithmetic and initializing functions.

Bit			Name	Definition
7-0	(FFh)	(r)	ALLONES	**ALL ONES register.** Always reads FFh.

All Zeros (ALLZEROS)

Type:R
Address:M-6Ah, DS-6Ah

This data port returns all zeros when read. It may be used for certain logical, arithmetic and initializing functions.

Bit			Name	Definition
7-0	(0)	(r)	ALLZEROS	**ALL ZEROS register.** Always reads 0.

No Destination (NONE)

Type:W
Address:M-6Ah, DS-6Ah

When this data port is selected as the destination, no change will be made to any write location. The read portion of this address is the ALLZEROS register. This register is typically used by Sequencer only.

Flags (FLAGS)

Type:R
Address:M-6Bh, DS-6Bh

This register provides access to the Sequencer instruction status flags. The ZERO flag is affected by all type instructions. The CARRY flag is affected only by Arithmetic, Shifts, Rotates, and Flag-Operation instructions.

	FLAGS R
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	ZERO
0	CARRY

Bit			Name	Definition
7-2	(0)	(r)	RSVD	Always reads 0.
1	(0)	(r)	ZERO	**Zero flag.** Contains the result of the current instruction operation, where the desired result is flag status of Zero or not Zero.
0	(0)	(r)	CARRY	**CARRY flag.** Contains the result of the selected previous instruction operation, where the desired flag status is a Carry or not a Carry.

Source Index Indirect (SINDIR)

Type:R
Address:DS-6Ch

When the **SINDIR** register is read, the value of the register pointed by **SINDEX** register is returned to Sequencer. This provides indirect addressing capability for the Sequencer. This register is usable only by the Sequencer.

SINDIR **R**	
	CONTENTS POINTED TO BY SINDEX

Destination Index Indirect (DINDIR)

Type:W
Address:DS-6Dh

When the **DINDIR** register is written, the register pointed by **DINDEX** register is written by Sequencer. This provides indirect addressing capability for the Sequencer. This register is usable only by the Sequencer.

DINDIR **W**	
	CONTENTS POINTED TO BY DINDEX

Function One (FUNCTIONONE)

Type:R/W
Address:M-6Eh, DS-6Eh

This register provides a specific hardware performed function that minimizes the number of instructions to obtain the desired result. Data is written to FUNCTIONONE with valid data in bits 6-4. This octal value is decoded into a 1 of 8 bit position. A value of 0 gives a 1 in bit position 0, a value of 1 gives a 1 in bit position 1, etc. with all other bit positions having a value of 0. The function is performed as a result of the write and the results of the function are obtained from the read.

FUNCTIONONE W		FUNCTIONONE R	
7	NOT USED	7	FUNONEDAT7
6	FUNCTION2	6	FUNONEDAT6
5	FUNCTION1	5	FUNONEDAT5
4	FUNCTION0	4	FUNONEDAT4
3	NOT USED	3	FUNONEDAT3
2	NOT USED	2	FUNONEDAT2
1	NOT USED	1	FUNONEDAT1
0	NOT USED	0	FUNONEDAT0

Bit		Name	Definition
7	(w)	NOT USED	Undefined
6-4	(w)	FUNCTION[2:0]	**Function One Write Data [2:0].** Write data bits for the function.
3-0	(w)	NOT USED	Undefined

Bit			Name	Definition
7-0	(0)	(r)	FUNONEDAT[7:0]	**Function One Read Data [7:0].** Read data bits for the function. 1 of 8 decoded value of FUNCTION[2:0].

Stack (STACK)

Type:R
Address:M-6Fh, DS-6Fh

The contents of the stack can be read and written by the Sequencer directly one byte at a time when the Seqeuncer is unpaused. The stack normally contains Instruction RAM address values, and is used by the Sequencer only. The Sequencer pushes and pops values from the stack as a result of program instruction operation. They are reported one byte at a time starting from the last location pushed on the stack until all entries are reported. The stack entries are reported by consecutive reads alternating low byte then high byte. The stack is 4 deep by 10 bits wide. The stack pointer will be incremented after a read of the high byte, therefore eight reads must be made in order to restore the location of the stack pointer to the original value if it is intended to continue program execution. The stack is read only from the system host and usually is read for diagnostic reasons only.

Bit			Name	Definition
7-0	(0)	(r)	STACK[7:0]	**STACK [07:00] register.** Contains stack data values.

Device Space Command 0 (DSCOMMAND0)

Type:R/W
Address:M-84h, DS-84h

The **DSCOMMAND0** register may be accessed by the sequencer when not paused. Bits[7:3] & bit[1] may be changed by writing to the **DSCOMMAND0** register, **CHIPRST** bit or the assertion of **PCIRST#**.

DSCOMMAND0 R/W	
7	CACHETHEN
6	DPARCKEN
5	MPARCKEN
4	EXTREQLCK
3	INTSCBRAMSEL
2	RAMPSM
1	SCBSIZE32
0	CIOPARCKEN

Bit			Name	Definition
7	(0)	(r/w)	CACHETHEN	**Cache Threshold Enable.** When active (=1), will cause the PCI master to determine when to request use of the PCI bus based on the definition of the DFF_THRSH register. Selecting the appropriate LAT_TIME and CACHESIZE register values when CACHETHEN is active will cause data transfers when the AIC-7890A/91 is a master to match the selected cache size (deterministic transfer) using cache line referenced PCI commands. This use presumes that software has located buffers on cache line boundaries or a small transfer will be performed to reach the first cache line boundary. The final transfer indicated by FIFOFLUSH active, for system memory write direction, will be flushed even if not a full cache size.
6	(0)	(r/w)	DPARCKEN	**Data Parity Check Enable.** When inactive (=0), disables the AIC-7890A/91 byte parity checking being performed as follows on internal data path byte accesses. For PIO read operations from the SCSI bus, the SCSI bus parity check control is controlled by the Device SIMODE1 register and is independent of DPARCKEN. When DPARCKEN is active, byte parity checking is performed and parity errors will cause DPARERR to be active in the ERROR register, BRKADRINT to be active in the INTSTAT register and (if INTEN is active and POWRDN is inactive) in the HCNTRL register the IRQA# output will become active.

Bit			Name	Definition
5	(0)	(r/w)	MPARCKEN	**Memory Parity Check Enable.** When inactive (=0), disables the AIC-7890A/91 parity checking on scratch RAM, and SCB Array (internal, or external when EXTSCBPEN is active) byte read accesses. When MPARCKEN is active, byte odd-parity checking is performed and parity errors will cause MPARERR to be active in the ERROR register, BRKADRINT to be active in the INTSTAT register and (if INTEN is active and POWRDN is inactive) in the HCNTRL register the IRQA# output will become active. Memory byte odd-parity is always generated.
4	(0)	(r/w)	EXTREQLCK	**External Request Lock.** When active (=1) causes the Memory Port output EXTARBREQ#, once it is asserted, to remain asserted until EXTREQLCK is inactive. This capability enables shared resource semaphore based accesses to be completed by a single user without being interrupted. EXTREQLCK active period should be limited as all other users are locked out from accessing the external devices at this time.
3	(1)	(r/w)	INTSCBRAMSEL	**Internal SCB RAM Select.** This bit is only used when RAMPS# is sampled low to indicate the existence of external SCB RAM when PCIRST# is asserted. When active (=1), selects the internal SCB RAM. When inactive (=0), selects the external SCB RAM if it exists. INTSCBRAMSEL is set active for internal SCB RAM upon writing to the CHIPRST bit.
2	(*)	(r)	RAMPSM	**RAM Present Mode**. Provides the capability to determine when the AIC-7890A/91's Memory Port has external RAM present (=1) that will be used for SCB data storage. When RAMPSM is (=0), the external RAM does not exist, and SCB data has to stored internally in the AIC-7890A/91. **Note:** (*) The state following reset is determined by the state of input RAMPS# during reset. RAMPSM is inverse of RAMPS#.
1	(0)	(r/w)	SCBSIZE32	**32-Byte SCB.** When this bit is set, a single SCB page size of 32 bytes is selected. When this bit is cleared, a single SCB page size of 64 bytes is selected
0	(0)	(r/w)	CIOPARCKEN	**CIOBUS Parity Check Enable**. When this bit is set (=1), any ciobus parity error will set the ERROR register bit 7 (CIOPARERR). When this bit is cleared (=0), ERROR register bit 7 (CIOPARERR) will never get set when a ciobus parity error occurs.

Device Space Command 1 (DSCOMMAND1)

Type:R/W
Address:M-85h, DS-85h

The DSCOMMAND1 register provides the ability to select between HADDR[3:0] and HADDR[7:4] registers, and between SHADDR[3:0] and SHADDR[7:4] registers. HADDR[3:0] and HADDR[7:4] registers share the same addresses 8Bh~88h. SHADDR[3:0] and SHADDR[7:4] registers share the same addresses 17h~14h.

DSCOMMAND1 R/W	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	HADDRLDSEL1
0	HADDRLDSEL0

Bit			Name	Definition
7-2	(0)	(r)	RSVD	Always reads 0.
1-0	(0)	(r/w)	HADDRLDSEL[1:0]	**Host Address Load Select [1:0].** Enable page expansion of the Host Address register (M/DS-8Bh~88h) and Shadow Address registers (M/DS-17h~14h) as follows:

[1:0]	Bit Value Assignment
0	Allows HADDR[3:0] and SHADDR[3:0] registers to be accessible.
1	Allows HADDR[7:4] and SHADDR[7:4] registers to be accessible.
3, 2	Reserved.

Host/Sequencer Mailbox (HS_MAILBOX)

Type:R/W
Address:M-86h, DS-86h

The Host/Sequencer Mailbox register provides two functions:

- Allows PCI Host to communicate with the Sequencer without pausing the Sequencer by writing to the upper 4 bits of **HOST_MAILBOX[3:0]**. PCI Host write to the lower 4 bits **SEQ_MAILBOX[3:0]** remain unaffected.
- Allows the Sequencer to communicate with the PCI Host without pausing by writing to the lower 4 bits of **SEQ_MAILBOX[3:0]**. Sequencer write to the upper 4 bits of **HOST_MAILBOX[3:0]** remain unaffected.

HS_MAILBOX R/W	
7	HOST_MAILBOX3
6	HOST_MAILBOX2
5	HOST_MAILBOX1
4	HOST_MAILBOX0
3	SEQ_MAILBOX3
2	SEQ_MAILBOX2
1	SEQ_MAILBOX1
0	SEQ_MAILBOX0

Bit			Name	Definition
7-4	(0)	(r/w)	HOST_MAILBOX[3:0]	**PCI HOST Mailbox**. The HOST Mailbox mechanism allows PCI Host to write 4 bits values for sequencer to read without pausing the SEQ.
3-0	(0)	(r/w)	SEQ_MAILBOX[3:0]	**SEQ Mailbox**. The SEQ Mailbox mechanism allows SEQ to write 4 bits values for PCI Host to read without pausing the SEQ.

Host Control (HCNTRL)

Type:R/W
Address:M-87h, DS-87h

The HCNTRL register provides the capability for the software driver to gain access to registers located on the AIC-7890A/91internal bus which are normally used by the sequencer and requires the sequencer to pause for access from the Host. HCNTRL also provides control features that only the software driver may access.

HCNTRL may be written to at any time without consideration of the state of the PAUSEACK bit. Writes to HCNTRL that change the state of PAUSE bit followed by a read of HCNTRL will extend the read access until the read value matches the written value.

HCNTRL R/W	
7	RSVD
6	POWRDN
5	RSVD
4	SWINT
3	HCNTRL3
2	PAUSE[ACK]
1	INTEN
0	CHIPRST[ACK]

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6	(0)	(r/w)	POWRDN	**Power Down.** When active (=1), disables the use of clock input CLKIN. Disables the SCSI bus inputs from external input levels. POWRDN also disables IRQA# from being asserted and limits Device register access to PCI Host only registers. Prior to placing POWRDN in the active state, software must ensure that SCSIENACK and HDMAENACK are in the inactive state and PAUSEACK is in the active state *from a latched PAUSE condition* to prevent errors from being transferred to the SCSI bus, System board, or System memory. Additionally a hardware interlock prevents writing a 0 to the PAUSE bit while writing a 1 to the POWRDN bit.
5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r/w)	SWINT	**Software Interrupt.** When active (=1), will cause the IRQA# to be active independent of other interrupt conditions. providing INTEN, MASTEREN and (MSPACEEN and/or ISPACEEN) are active and POWRDN is inactive. SWINT when active does not cause any changes to the INTSTAT register and its state must be monitored by reading the HCNTRL register.
3	(0)	(r/w)	HCNTRL3	A spare R/W capable bit with no current hardware control assignment.

Bit			Name	Definition
2	(1)	(w)	PAUSE	**Pause** (located in the write portion of the PAUSE[ACK] bit). When active, requests the sequencer to be paused in an latched condition.
		(r)	PAUSEACK	**Pause Acknowledge** (located in the read portion of the PAUSE[ACK] bit). When this bit is read, it gives the PAUSEACK status and should be polled to be sure that the sequencer is paused. The driver may start at the address that was paused or at this time change the sequencer program counter (SEQADDR). Clearing this bit will release the sequencer and it will continue at the current value of the program counter. When PAUSEACK is active, access is enabled for the host to Device registers normally restricted when it is not paused (also see POWRDN bit). This bit also becomes active due to certain hardware conditions, PCIRST# assertion, or writing to CHIPRST. For other conditions, see INTSTAT register and the sequencer section.
1	(0)	(r/w)	INTEN	**Interrupt Enable.** The interrupt enable bit when active will allow active interrupt conditions stored in the AIC-7890A/91 to assert the IRQA# pin, providing that the MASTEREN bit in the Configuration Command register is active.
0	(1)	(w)	CHIPRST	**Chip Reset** (located in the write portion of the CHIPRST[ACK]) This bit when written (=1) will produce the same condition as when PCIRST# is asserted to cause the device except for the Configuration register space to enter an initialized state.
		(r)	CHIPRSTACK	**Chip Reset Acknowledge** (located in the read portion of the CHIPRST[ACK] bit).This status bit when active (=1) indicates a write to CHIPRST has occurred or that PCIRST# has been asserted. CHIPRSTACK will remain active until explicitly writing to CHIPRST (=0).

Data Channel Low Host Address (HADDR[3:0])

Type:R/W
Address: M-8Bh~88h, DS-8Bh~88h and HADDRLDSEL[1:0] = 0

The Data Channel Low Host Address registers contain the low 32-bits of system memory address for which the data that will transfer to or from the data FIFO when the AIC-7890A/91 is the PCI bus master. They perform as count up counters and count up by one for each byte transferred between the device and system memory. **HADDR[3:0]** values are issued on the **AD[31:00]** lines during the **PCLK** cycle that **FRAME#** is asserted on for either SAC or DAC transactions. **HADDR[3:0]** initialize to zero by **CHIPRST** or **PCIRST#**.

Note, after **HADDR[3:0]** and **HCNT[2:0]** have been loaded with the desired values, **HDMAEN** is placed in the active state allowing transfers to commence. Then, at a later time, should **HDMAEN** be placed in the inactive state prior to **HCNT[2:0]** reaching a count of zero, it is disallowed to reload **HADDR[3:0]** with new values, placing **HDMAEN** back in the active state for the same disrupted transfer, unless the data FIFO is re-initialized.

HADDR3 R/W		HADDR2 R/W		HADDR1 R/W		HADDR0 R/W	
7	HADDR31	7	HADDR23	7	HADDR15	7	HADDR07
6	HADDR30	6	HADDR22	6	HADDR14	6	HADDR06
5	HADDR29	5	HADDR21	5	HADDR13	5	HADDR05
4	HADDR28	4	HADDR20	4	HADDR12	4	HADDR04
3	HADDR27	3	HADDR19	3	HADDR11	3	HADDR03
2	HADDR26	2	HADDR18	2	HADDR10	2	HADDR02
1	HADDR25	1	HADDR17	1	HADDR09	1	HADDR01
0	HADDR24	0	HADDR16	0	HADDR08	0	HADDR00

Data Channel High Host Address (HADDR[7:4])

Type:R/W
Address: M-8Bh~88h, DS-8Bh~88h and HADDRLDSEL[1:0] = 1

The Data Channel High Host Address registers contain the upper 32-bits of a 64-bit system memory address for which the data will transfer to or from the data FIFO when the AIC-7890A/91 is the PCI bus master. There are two possible scenarios:

- In 32-Bit PCI System: When **HADDR[7:4]** contain only the value of zero, the AIC-7890A/91 as a PCI master will only issue SACs. When **HADDR[7:4]** contain a value other than zero and **DACEN** is active in the Configuration **DEVCONFIG** register, the AIC-7890A/91 as a PCI master will issue DACs using the **HADDR[7:4]** values in the **PCLK** cycle following the **PCLK** cycle that asserted **FRAME#**. The AIC-7890A/91 as a target does not support DACs. **HADDR[7:4]** initialize to zero by **CHIPRST** or **PCIRST#**. When **DACEN** is not active **HADDR[7:4]** registers may be used for general-purpose storage if desired.
- In 64-Bit PCI System: **HADDR[7:4]** values are issued onto the **AD[63:32]** lines during the **PCLK** cycle that **FRAME#** is asserted when the AIC-7891 is the PCI bus master.

HADDR7 R/W		HADDR6 R/W		HADDR5 R/W		HADDR4 R/W	
7	HADDR63	7	HADDR55	7	HADDR47	7	HADDR39
6	HADDR62	6	HADDR54	6	HADDR46	6	HADDR38
5	HADDR61	5	HADDR53	5	HADDR45	5	HADDR37
4	HADDR60	4	HADDR52	4	HADDR44	4	HADDR36
3	HADDR59	3	HADDR51	3	HADDR43	3	HADDR35
2	HADDR58	2	HADDR50	2	HADDR42	2	HADDR34
1	HADDR57	1	HADDR49	1	HADDR41	1	HADDR33
0	HADDR56	0	HADDR48	0	HADDR40	0	HADDR32

Data Channel Host Count (HCNT[2:0])

Type:R/W
Address:M-8Eh~8Ch, DS-8Eh~8Ch

HCNT[2:0]. The Host Count registers contain a count of the number of bytes to be transferred between system memory and the data FIFO when the AIC-7890A/91 is an active bus master. HCNT[2:0] perform as count down counters and count down by one for each byte transferred between system memory and data FIFO. Transfers are inhibited when the count value of HCNT[2:0] is zero.

Note: Address M/DS-8Fh is reserved for future expansion. Always reads as 0h, and writes are ignored.

HCNT2 R/W		HCNT1 R/W		HCNT0 R/W	
7	HCNT23	7	HCNT15	7	HCNT07
6	HCNT22	6	HCNT14	6	HCNT06
5	HCNT21	5	HCNT13	5	HCNT05
4	HCNT20	4	HCNT12	4	HCNT04
3	HCNT19	3	HCNT11	3	HCNT03
2	HCNT18	2	HCNT10	2	HCNT02
1	HCNT17	1	HCNT09	1	HCNT01
0	HCNT16	0	HCNT08	0	HCNT00

SCB Pointer (SCBPTR)

Type:R/W
Address:M-90h, DS-90h

The SCB Pointer register provides the page address to the SCB Array. The data value loaded in this register selects one of 16 pages of 64 registers to be accessed through the SCB address range (A0h-DFh) when the on-chip SCB memory is selected. The data value loaded in this register selects one of 256 pages of 64 registers to be accessed through the SCB address range (A0-DF) when the external SRAM is selected for SCB storage. Changing this value during execution will not alter any data, but will address a different page of the array.

SCBPTR R/W	
7	SCBVAL7
6	SCBVAL6
5	SCBVAL5
4	SCBVAL4
3	SCBVAL3
2	SCBVAL2
1	SCBVAL1
0	SCBVAL0

Bit			Name	Definition
7-0	(0)	(r/w)	SCBVAL[7:0]	SCB page selection.

Interrupt Status (INTSTAT)

Type:R/W
Address:M-91h, DS-91h

INTSTAT register provides device interrupt status for the driver when an interrupt condition occurs. The INTSTAT register is written to by the sequencer, and may be read from the PCI bus without pausing the sequencer. The sequencer is automatically paused when the SEQINT, SCSIINT or BRKADRINT bit(s) are active. The INTCODE is only valid when SEQINT bit is active. Bits [3:0] may also be individually reset by use of the CLRINT register.

When IRQA# is asserted, the software driver must check both the INTSTAT and ERROR registers to determine the cause(s) of the interrupt. Status bits (DPE, DPR) become active as a result of a PCI master or target transaction and cause an interrupt, provided that PERRESPEN is active and FAILDIS is inactive. Status bits (STA, RTA, RMA, SSI) become active as a result of a PCI master or target transaction and cause an interrupt, provided that FAILDIS is inactive.

INTSTAT R/W	
7	INTCODE3
6	INTCODE2
5	INTCODE1
4	INTCODE0
3	BRKADRINT
2	SCSIINT
1	CMDCMPLT
0	SEQINT

Bit			Name	Definition
7-4	(0)	(r/w)	INTCODE(3:0)	**Interrupt Code.** These bits enable a code to be stored to identify the condition causing the SEQINT bit to be active. By convention the INTCODE[3:0] bits are only considered valid when the SEQINT bit is active and should be written in the same write operation that activates SEQINT. See the discussion on interrupts for a definition of this code.
3	(0)	(r/w)	BRKADRINT	**Break Address Interrupt.** This bit becomes active (=1) when using the sequencer firmware breakpoint feature (see registers BRKADDR[1:0] in the sequencer section). Note when the current sequencer instruction breakpoint is an access to an SCB Array address with RAMPSM active (external SRAM), the sequencer instruction may be stretched while arbitration is being performed for the external SRAM, and a PAUSE request due to an active BRKADRINT will be delayed until arbitration is completed. BRKADRINT is also used for selected error conditions as follows:

Bit			Name	Definition
				■ When the program counter of the sequencer and the break address are equal and the Breakpoint feature is enabled (BRKDIS=0). ■ When ILLOPCODE becomes active (FAILDIS=0). ■ When SQPARERR becomes active (FAILDIS and PERRORDIS=0). ■ When DPARERR becomes active (DPARCKEN=1 and FAILDIS=0). ■ When MPARERR becomes active (MPARCKEN=1 and FAILDIS=0). ■ When CIOPARERR becomes active (PERROR-DIS=1 and FAILDIS=0). While the BRKADRINT bit is active it forces the PAUSE bit in HCNTRL register to be active and IRQA# to be asserted when INTEN and MASTEREN are active and POWRDN is inactive. When BRKADRINT is active due to source 1, it may be set inactive by a write to the CLRINT register with CLRBRKADRINT bit 3 (=1). When BRKADRINT is active due to source 2, it may be set inactive by a write to CHIPRST (=1) in the HCNTRL register. When BRKADRINT is active due to source 3-5, it may be set inactive by a write to CLRPARERR (=1) in the CLRINT register. This action will also clear any PCIERRSTAT latched interrupt conditions that may exist, but will not clear the Configuration STATUS1 register bits.
2	(0)	(r/w)	SCSIINT	**SCSI Interrupt.** This bit is latched in the INTSTAT register and is active when there is a catastrophic SCSI event. Causes are SCSI Reset, Parity Error, Selection Time-out, or Unexpected Bus Free. Any interrupt condition in the SCSI section may cause this interrupt if the corresponding interrupt is enabled in SIMODE0 or SIMODE1. When this bit is set, the sequencer is paused immediately. IRQA# is also asserted when INTEN and MASTEREN are active and POWRDN is inactive. The cause of SCSIINT being active must be cleared, then a write to CLRSCSIINT =1 in the CLRINT register to cause SCSIINT to be read in the inactive state.
1	(0)	(r/w)	CMDCMPLT	**Command Complete Interrupt.** This bit is set active by the sequencer writing to the INTSTAT register with CMDCMPLT (=1) during normal operation after a SCSI command has been completed. The sequencer will continue running while this bit is active. While the CMDCMPLT bit is active IRQA# is asserted when INTEN and MASTEREN is active. CMDCMPLT is inactive after a write to the CLRINT register with CLRCMDINT bit (=1).

Bit			Name	Definition
0	(0)	(r/w)	SEQINT	**Sequencer Interrupt.** This bit is set active by the sequencer writing to the INTSTAT register with SEQINT (=1) when the sequencer requires driver intervention to complete a command or to handle an exception condition. The sequencer is paused by this interrupt immediately (no instruction is performed following the write to set this bit). While SEQINT is active, IRQA# is also asserted when INTEN and MASTEREN is active and POWRDN is inactive. SEQINT is inactive after a write to the CLRINT register with CLRSEQINT bit (=1).

Clear Interrupt (CLRINT)

Type:W
Address:M-92h

The CLRINT register allows the driver to clear the cause of the interrupt from the device. Selected interrupts are cleared by writing with the desired bit pattern =1. The bits in this register are self-clearing. The sequencer cannot write to this register and the driver may write to it without pausing the sequencer.

Note: When PCIRST# is active it also forces CLRPARERR, CLRBRKADRINT, CLRSCSIINT, CLRCMDINT and CLRSEQINT to also be active.

CLRINT W	
7	RSVD
6	RSVD
5	RSVD
4	CLRPARERR
3	CLRBRKADRINT
2	CLRSCSIINT
1	CLRCMDINT
0	CLRSEQINT

Bit		Name	Definition
7-5	(r)	RSVD	Always reads 0.
4	(w)	CLRPARERR	**Clear Parity Errors.** When this bit is written (=1), the CIOPARERR, SQPARERR, MPARERR and DPARERR bits are cleared if set in the ERROR register. To clear these bits, see the *Configuration Status Register* section. This bit will self-clear.
3	(w)	CLRBRKADRINT	**Clear Break Address Interrupt.** When this bit is written (=1), the BRKADRINT bit is cleared in the INTSTAT register. CLRBRKADRINT bit will self-clear. See the INTSTAT register for causes of BRKADRINT being active which may have to be cleared prior to clearing the BRKADRINT bit. ILLOPCODE may only be cleared by writing CHIPRST (=1) or asserting PCIRST#.
2	(w)	CLRSCSIINT	**Clear SCSI Interrupt.** When this bit is written (=1), the SCSIINT bit is cleared in the INTSTAT register. This bit will self-clear.
1	(w)	CLRCMDINT	**Clear Command Complete Interrupt.** When this bit is written (=1), the CMDCMPLT bit is cleared in the INTSTAT register. This bit will self-clear.
0	(w)	CLRSEQINT	**Clear Sequencer Interrupt.** When this bit is written (=1), the SEQINT bit is cleared in the INTSTAT register. This bit will self-clear.

Error (ERROR)

Type:R
Address:M-92h

This register reports errors that are catastrophic in nature due to (software/firmware/hardware) error conditions that must be corrected for the device to operate properly. These errors will cause BRKADRINT to be active (except PCI errors) and the sequencer to be paused. Clearing of these bits (except for PCIERRSTAT and ILLOPCODE) requires writing to CLRPARERR for (SQPARERR, MPARERR, DPARERR and CIOPARERR). Writing to CHIPRST (=1) will clear ILLOPCODE, and asserting input PCIRST# will clear all latched bits. This register can only be accessed from the PCI Host.

ERROR R	
7	CIOPARERR
6	PCIERRSTAT
5	MPARERR
4	DPARERR
3	SQPARERR
2	ILLOPCODE
1	RSVD
0	RSVD

Bit			Name	Definition
7	(0)	(r)	CIOPARERR	**CIOBUS Parity Error.** When active (=1), indicates an odd-parity error has been detected on the CIOBUS (internal bus). The MPARCKEN bit in the Device Space COMMAND register must be active to enable CIOPARERR to be become active.
6	(0)	(r)	PCIERRSTAT	**PCI Error Status.** When active (=1), indicates a PCI error has been detected by AIC-7890A/91 and is stored in Configuration STATUS1 register. PCIERRSTAT is the OR of any bit [5:0] active in the Device PCISTATUS register. PCIERRSTAT becomes inactive when the PCI errors are inactive. This bit is read-only; writing to this register or the CHIPRST bit has no effect. Writing to Configuration STATUS registers or asserting PCIRST# is required to clear it.
5	(0)	(r)	MPARERR	**Memory Parity Error.** When active (=1), indicates an odd-parity error has been detected in the SCRATCH or SCB Array (internal or external) RAM cells. MPARCKEN bit in Device Space COMMAND register must be active to enable MPARERR to be become active.
4	(0)	(r)	DPARERR	**Data-path Parity Error.** When active (=1), indicates an odd-parity error has been detected in the device internal data path (check logic is located in the host, data FIFO and the SCSI blocks) byte parity. The DPARCKEN bit in the Device Space Command register must be active to enable DPARERR to be become active.

Bit			Name	Definition
3	(0)	(r)	SQPARERR	**Sequencer Parity Error.** When active (=1), indicates a parity error has been detected in the sequencer control store RAM. PERRORDIS in the Sequencer SEQCTL register must be inactive for SQPARERR to become active.
2	(0)	(r)	ILLOPCODE	**Illegal Opcode Error.** When active (=1), indicates a undefined sequencer instruction has been detected in the sequencer's firmware fetch from its control store RAM.
1-0	(0)	(r)	RSVD	Always reads 0.

Data FIFO Control (DFCNTRL)

Type:R/W
Address:M-93h, DS-93h

The DFCNTRL register provides data path hardware control. DIRECTIONACK, HDMAENACK, SCSIENACK and FIFOFLUSH bits have hardware enforced state changes to ensure proper control of the data path. This control allows several hardware functions to be combined into a single write to the DFCNTRL register. Some bits are self-clearing and some must be cleared by the driver. When PCIRST# or CHIPRST is active, all DFCNTRL register bits are forced to zero.

DFCNTRL R/W	
7	PRELOADEN
6	RSVD
5	SCSIEN[ACK]
4	RSVD
3	HDMAEN[ACK]
2	DIRECTION[ACK]
1	FIFOFLUSH[ACK]
0	RSVD

Bit			Name	Definition
7	(0)	(r/w)	PRELOADEN	**Preload Enable.** When this bit is set and PRELOAD_AVAIL is active, the values in the HADDR and HCNT registers are validated and stored for next Data FIFO DMA operation. This bit is self-clearing.
6	(0)	(r)	RSVD	Always reads 0.
5	(0)	(r/w)	SCSIEN[ACK]	**SCSI Transfer Enable/SCSI Transfer Enable Acknowledge.** When this bit is active (=1) it enables transfers between the SCSI bus and the Data FIFO. Clearing this bit will cleanly halt the transfer by preventing another ACK to the SCSI bus. Reading this bit (SCSIENACK) provides status which indicates the state of the hardware. When this bit is cleared, it must be read back as zero before the transfer is guaranteed to have halted. Synchronous data-in transfers to the Data FIFO will always be enabled when the synchronous offset value programmed in SCSIRATE is nonzero and the SCSI bus is in Data-in phase.
4	(0)	(r)	RSVD	Always reads 0.

Bit			Name	Definition
3	(0)	(r/w)	HDMAEN[ACK]	**Data Channel DMA Enable/Data Channel DMA Enable Acknowledge.** When this bit is active it enables the PCI host interface to transfer data to or from system memory. The Host Address and Host Count registers must be set up and the data FIFO initialized prior to activating this bit. Clearing this bit will halt transfers without losing data, status, or byte count. Transfers may be continued after halting. Reading this bit (HDMAENACK) provides status which indicates the state of the hardware. When this bit is cleared it must be read back as zero before the transfer is guaranteed to have halted.
2	(0)	(r/w)	DIRECTION[ACK]	**Data Path Direction Acknowledge.** This bit when active (=1), will condition data transfers to be from the PCI bus to the data FIFO and from the data FIFO to the SCSI bus. The Direction bit when not active (=0,) will condition data transfers to be from the SCSI bus to the data FIFO and from the data FIFO to the PCI bus. When both HDMAENACK and SCSIEN are inactive, the sequencer cell may both read and write DFDAT without regard for the state of the DIRECTION bit. The state of DIRECTIONACK will not change unless the enable bits (bits 3, 4 and 5) are cleared.
1	(0)	(r/w)	FIFOFLUSH[ACK]	**Data FIFO Flush.** During a SCSI bus to PCI bus transfer (a SCSI read operation as initiator), FIFOFLUSH may be set (manual flush) to force the remaining bytes in the data FIFO to be sent to the PCI host memory. If FIFOEMP is active, attempts to set this bit active will have no effect. This bit is self-clearing and has no effect during a PCI bus to SCSI bus operation. An Autoflush to force the remaining bytes to be transferred will occur by the hardware when STCNT counts down to zero or a SCSI phase change occurs (providing AUTOFLUSHDIS=0 in the SBLKCTL register). When this bit is read as a one, it indicates a flush operation is pending or in operation due to either a firmware or hardware flush. It will read as a zero when the flush operation is completed.
0	(0)	(r)	RSVD	Always reads 0.

Data FIFO Status (DFSTATUS)

Type:R
Address:M-94h, DS-94h

The DFSTATUS register contains data channel status.

DFSTATUS R	
7	PRELOAD_AVAIL
6	RSVD
5	RSVD
4	MREQPEND
3	HDONE
2	DFTHRSH
1	FIFOFULL
0	FIFOEMP

Bit			Name	Definition
7	(1)	(r)	PRELOAD_AVAIL	**Preload HADDR and HCNT Available.** This active high status bit is used to indicate that HADDR and HCNT registers are available to store next scatter/gather address and count for data channel DMA operation. HADDR and HCNT registers can store up to three sets of scatter/gather address and count.
6	(0)	(r)	RSVD	Always reads 0.
5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r)	MREQPEND	**Memory Request Pending.** When active, it indicates that AIC-7890A/91 is requesting to access the PCI bus to perform DMA operation.
3	(1)	(r)	HDONE	**Host Done** status bit. When active (=1), indicates that the count previously stored in HCNT[2:0] has expired (count=0) and the last transfer between system memory and the data FIFO has completed.
2	(0)	(r)	DFTHRSH	**Data FIFO Threshold Status**. When active, it indicates that the threshold condition has been met based on the settings on the DFF_THRSH register and CACHETHEN bit.
1	(0)	(r)	FIFOFULL	**Data FIFO Full Status**. When active (=1) indicates that all byte locations in the data FIFO contain data. Data must not be written to the data FIFO when FIFOFULL is active. **Note:** The current full position for normal operation in the data FIFO will change depending on the number of data bytes read from the data FIFO prior to writing it. FIFOFULL will be forced to be inactive when CHIPRST is written (=1), or PCIRST# is asserted.

Bit			Name	Definition
0	(1)	(r)	FIFOEMP	**Data FIFO Empty Status.** When active (=1) indicates that no data bytes are stored in the data FIFO. The data FIFO must not be read from when FIFOEMP is active. **Note:** The current empty position for normal operation in the data FIFO will change depending on the number of data bytes written to the data FIFO prior to reading it. FIFOEMP will be forced to be active when CHIPRST is written (=1) or PCIRST# is asserted.

Data FIFO Write Address (DFWADDR)

Type:R/W
Address:M-95h, DS-95h

This register contains the address (write pointer) of the current data FIFO location to be written to. Each value points to a 72-bit Quad Word (QWD) location in the Data FIFO. The DFWADDR register is automatically incremented when the high byte in a QWD is written through the DFDAT register or data path transfers between the PCI and SCSI buses This register should only be accessed when HDMAEN and SCSIEN are not active.

DFWADDR R/W	
7	RSVD
6	DFWADDR6
5	DFWADDR5
4	DFWADDR4
3	DFWADDR3
2	DFWADDR2
1	DFWADDR1
0	DFWADDR0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6	(0)	(r/w)	DFWADDR6	**Data FIFO Write Address 6.** Provides access to the data FIFO write address roll-over status bit which is used to determine data FIFO full and empty status.
5-0	(0)	(r/w)	DFWADDR[5:0]	**Data FIFO Write Address [5:0].** The QWD address lines to the data write port of the data FIFO.

Data FIFO Read Address (DFRADDR)

Type:R/W
Address:M-97h, DS-97h

This register contains the address (read pointer) of the current data FIFO location to be read from. Each value points a 72-bit Quad Word (QWD) location in the Data FIFO. The **DFRADDR** register is automatically incremented when the high byte in a QWD is read through the **DFDAT** register or data path transfers between the PCI and SCSI buses. This register should only be accessed when **HDMAEN** and **SCSIEN** are not active.

DFRADDR R/W	
7	RSVD
6	DFRADDR6
5	DFRADDR5
4	DFRADDR4
3	DFRADDR3
2	DFRADDR2
1	DFRADDR1
0	DFRADDR0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6	(0)	(r/w)	DFRADDR6	**Data FIFO Read Address 6.** Provides access to the data FIFO read address roll-over status bit which is used to determine data FIFO full and empty status.
5-0	(0)	(r/w)	DFRADDR[5:0]	**Data FIFO Read Address [5:0].** The QWD address lines to the data read port of the data FIFO

Data FIFO Data (DFDAT)

Type:R/W
Address:M-99h, DS-99h

This register stores data into the data FIFO using register DFWADDR when written and reads data from the data FIFO using register DFRADDR when read. DFWADDR and DFRADDR registers may be adjusted if a specific data FIFO QWD location is desired. For more information, see reading and writing the data FIFO. This register should only be accessed when HDMAEN and SCSIEN are not active.

	DFDAT R/W
7	DFDAT7
6	DFDAT6
5	DFDAT5
4	DFDAT4
3	DFDAT3
2	DFDAT2
1	DFDAT1
0	DFDAT0

SCB Counter (SCBCNT)

Type:R/W
Address:M-9Ah, DS-9Ah

The SCBCNT register provides two modes for SCB Array page byte address access:

- Direct SCB Array page byte addressing for random access within the page.
- Indirect SCB Array page byte addressing by use of **SCBCNT[5:0]** where each access causes the value in **SCBCNT[5:0]** to increment for linear access within the selected page. When **SCBCNT[5:0]** are being used both the read and write addresses of the SCB Array are the same address and when not used (for sequencer access only) may be different addresses in the page.

SCBCNT R/W	
7	SCBAUTO
6	RSVD
5	SCBCNT5
4	SCBCNT4
3	SCBCNT3
2	SCBCNT2
1	SCBCNT1
0	SCBCNT0

Bit			Name	Definition
7	(0)	(r/w)	SCBAUTO	**SCB Auto Address.** When active (=1), enables SCBCNT[5:0] to supply the offset address into the selected SCB Array page in place of the address supplied by the host or sequencer. When SCBAUTO is inactive, the value stored in SCBCNT[5:0] is not used. When SCBAUTO is active, accesses to the SCB Array may be made repeatedly to the same address, which must be within the normal SCB Array address range (M/DS-A0 - M/DS-DFh) when SCBs are stored either internal or external to the AIC-7890A/91.
6	(0)	(r)	RSVD	Always reads 0.
5-0	(0)	(r/w)	SCBCNT[5:0]	**SCB Counter.** Stores the address of the byte location that will be accessed in the selected SCB Array page. The value in SCBCNT[5:0] is only used when SCBAUTO is active.

Special Function (SFUNCT)

Type:R/W
Address:M-9Fh, DS-9Fh

SFUNCT bits [7:4] select certain sections of the chip for test purposes. SFUNCT bits [2:0] select a specific test in that section of the chip. To access PCI configuration space registers of the AIC-7890A/91 through PCI I/O or memory cycles, write 0Eh to the SFUNCT register, and the complete PCI configuration space is mapped to the PCI memory space or memory-mapped I/O space assigned to this chip, starting at the offset of zero. To return to the normal mapping for the device space registers, write 00h to the SFUNCT register. The PCI configuration space registers can only be accessed from the PCI interface, and not by the sequencer through the internal bus.

SFUNCT R/W	
7	ALT_MODE
6	GROUP3
5	GROUP2
4	GROUP1
3	GROUP0
2	TEST2
1	TEST1
0	TEST0

Bit			Name	Definition
7	(0)	(r/w)	ALT_MODE	**Alternate Mode.** When active, the 256-byte device register space is mapped to another page for an additional register space, called alternate mode. When inactive (default), the device register space is called functional mode.
6-3	(0)	(r/w)	GROUP[3:0]	For production test purposes only.
2-0	(0)	(r/w)	TEST[2:0]	For production test purposes only.

Command Channel Low Host Address (CCHADDR[3:0])

Type:R/W
Address:M-E3h~E0h, DS-E3h~E0h

The Command Channel Low Host Address registers contain the low 32-bits of system memory address of the data that will transfer to or from the Command Channel SRAM as an active bus master. They perform as count up counters and count up by one for each byte transferred between the device and system memory. **CCHADDR[7:0]** values are issued on the **AD[31:00]** lines during the **PCLK** cycle that **FRAME#** is asserted on for either SAC or DAC transactions. **CCLHADDR[3:0]** initialize to zero by **CHIPRST** or **PCIRST#**.

Note, after **CCHADDR[7:0]** and **CCHCNT** have been loaded with the desired values and either bits **CCSGEN** or **CCSCBEN** is placed in the active state allowing transfers to commence. Then, at a later time, placing either bits **CCSGEN** or **CCSCBEN** in the inactive state prior to **CCHCNT** reaching a count of zero, it is disallowed to reload **CCLHADDR[3:0]** with new values, placing either bits **CCSGEN** or **CCSCBEN** back in the active state for the same disrupted transfer, unless the Command channel SRAM is re-initialized.

CCHADDR3 R/W		CCHADDR2 R/W		CCHADDR1 R/W		CCHADDR0 R/W	
7	CCLHADDR31	7	CCLHADDR23	7	CCLHADDR15	7	CCLHADDR07
6	CCLHADDR30	6	CCLHADDR22	6	CCLHADDR14	6	CCLHADDR06
5	CCLHADDR29	5	CCLHADDR21	5	CCLHADDR13	5	CCLHADDR05
4	CCLHADDR28	4	CCLHADDR20	4	CCLHADDR12	4	CCLHADDR04
3	CCLHADDR27	3	CCLHADDR19	3	CCLHADDR11	3	CCLHADDR03
2	CCLHADDR26	2	CCLHADDR18	2	CCLHADDR10	2	CCLHADDR02
1	CCLHADDR25	1	CCLHADDR17	1	CCLHADDR09	1	CCLHADDR01
0	CCLHADDR24	0	CCLHADDR16	0	CCLHADDR08	0	CCLHADDR00

Command Channel High Host Address (CCHADDR[7:4])

Type:R/W
Address:M-E7h~E4h, DS-E7h~E4h

The Command Channel High Host Address registers contain the upper 32-bits of a 64-bit system memory address for which the data will transfer to or from the Command Channel SRAM when the AIC-7890A/91 is the PCI bus master. Two scenarios are possible:

- In 32-Bit PCI System: When **CCHADDR[7:4]** contain only the value of zero, the AIC-7890A/91 as a PCI master will only issue SACs. When **CCHADDR[7:4]** contain a value other than zero and **DACEN** is active in the Configuration **DEVCONFIG** register, the AIC-7890A/91 as a PCI master will issue DACs using the **CCHADDR[7:4]** values in the **PCLK** cycle following the **PCLK** cycle that asserted **FRAME#**. The AIC-7890A/91 as a target does not support DACs. **CCHADDR[7:4]** initialize to zero by **CHIPRST** or **PCIRST#**. When **DACEN** is not active **CCHADDR[7:4]** registers may be used for general-purpose storage if desired.
- In 64-Bit PCI System: **CCHADDR[7:4]** values are issued on the **AD[63:32]** lines during the **PCLK** cycle that **FRAME#** is asserted when the AIC-7891 is the PCI bus master.

CCHADDR7 R/W		CCHADDR6 R/W		CCHADDR5 R/W		CCHADDR4 R/W	
7	CCHADDR63	7	CCHADDR55	7	CCHADDR47	7	CCHADDR39
6	CCHADDR62	6	CCHADDR54	6	CCHADDR46	6	CCHADDR38
5	CCHADDR61	5	CCHADDR53	5	CCHADDR45	5	CCHADDR37
4	CCHADDR60	4	CCHADDR52	4	CCHADDR44	4	CCHADDR36
3	CCHADDR59	3	CCHADDR51	3	CCHADDR43	3	CCHADDR35
2	CCHADDR58	2	CCHADDR50	2	CCHADDR42	2	CCHADDR34
1	CCHADDR57	1	CCHADDR49	1	CCHADDR41	1	CCHADDR33
0	CCHADDR56	0	CCHADDR48	0	CCHADDR40	0	CCHADDR32

Command Channel Host Count (CCHCNT)

Type:R/W
Address:M-E8h, DS-E8h

The Command Channel Host Count register contains a count of the number of bytes to be transferred between system memory and the Command Channel SRAM when the AIC-7890A/91 is an active bus master. CCHCNT performs as a count down counter and counts down by one for each byte transferred between system memory and Command Channel SRAM. Transfers are inhibited when the count value of CCHCNT is zero.

Note: Writes to this register address E8h, also writes the same value to register CCSCBCNT, address EFh if and only if bit CCARREN is inactive (=0) in register CCSCBCTL.

CCHCNT R/W	
7	CCHCNT7
6	CCHCNT6
5	CCHCNT5
4	CCHCNT4
3	CCHCNT3
2	CCHCNT2
1	CCHCNT1
0	CCHCNT0

Command Channel S/G RAM Data Port (CCSGRAM)

Type:R
Address:M-E9h, DS-E9h

CCSGRAM. This register is a data port to the Command Channel Scatter/Gather SRAM area. This port allows the access to the Command Channel Scatter/Gather SRAM by SEQ or through host PIO. For DMA write transfers between host memory and this SRAM, CCHADDR[7:0], and CCHCNT must be first initialized with the system memory address and the count of the number of bytes to be transferred via Command Channel. The Command Channel can then be enabled by writing a 9h value to register CCSGCTL (CCSGRESET = 1, and CCSGEN = 1). Writing a 1 value to bit CCSGRESET resets the Scatter/Gather SRAM address pointer to zero. Writing a 1 value to bit CCSGEN enables the DMA transfer. For every byte transferred between the system memory and the Scatter/Gather SRAM counter CCSGADR will increment by one and CCHCNT will decrement by one. The Sequencer is not allowed to access this CCSGRAM dataport when the SG DMA channel is active. It must check for CCSGDONE status = 1 before accessing it. Accessing CCSGRAM dataport when SG RAM DMA is in progress will corrupt the DMA transfer. On the other hand, the Sequencer is allowed to access CCSCBRAM dataport when the CCSCBRAM DMA is not active.

CCSGRAM R	
7	CCSGRAM7
6	CCSGRAM6
5	CCSGRAM5
4	CCSGRAM4
3	CCSGRAM3
2	CCSGRAM2
1	CCSGRAM1
0	CCSGRAM0

Command Channel S/G RAM Address Pointer (CCSGADR)

Type:R/W
Address:M-EAh, DS-EAh

CCSGADR. This register contains the address of the Scatter/Gather SRAM that will be used to either write or read data. The contents of this register increments by one for every byte written or read by either DMA write transfers, or Sequencer reads/writes. CCSGADR is cleared to zero by PCIRST#, CHIPRST, or CCSGRESET.

CCSGADR R/W	
7	CCSGADR7
6	CCSGADR6
5	CCSGADR5
4	CCSGADR4
3	CCSGADR3
2	CCSGADR2
1	CCSGADR1
0	CCSGADR0

Command Channel S/G Control (CCSGCTL)

Type:R/W
Address:M-EBh, DS-EBh

CCSGCTL. This register provides Command channel hardware control. It is exclusively used to DMA Scatter/Gather list elements into the Command channel Scatter/Gather SRAM. *This DMA channel is unidirectional, i.e., DMA transfers occur only from the system memory to the Command channel Scatter/Gather SRAM* and not vice versa. When PCIRST# or CHIPRST is active, all CCSGCTL register bits are forced to zero.

CCSGCTL R/W	
7	CCSGDONE
6	RSVD
5	RSVD
4	RSVD
3	CCSGEN[ACK]
2	RSVD
1	FLAG
0	CCSGRESET

Bit			Name	Definition
7	(0)	(r)	CCSGDONE	**Command Channel Scatter/Gather List Elements Prefetch Done.** When active (=1), indicates that the count previously stored in CCHCNT has expired (count = 0) and the last transfer between system memory and the Scatter/Gather SRAM has completed, including any temporary storage in the PCI host module.
6-4	(0)	(r)	RSVD	Always reads 0.
3	(0)	(r/w)	CCSGEN[ACK]	**Command channel Scatter/Gather SRAM Transfer Enable/Acknowledge.** When this bit is active (=1), it enables transfers between system memory and Scatter/Gather SRAM. Clearing this bit will cleanly halt the transfer. Reading this bit (CCSGENACK) provides status which indicates the state of the hardware. When this bit is cleared, it must be read back as zero before the transfer is guaranteed to have halted. *The Sequencer firmware should never enable two DMA transfers at the same time into the Command channel by setting both the enable bits, CCSGEN and CCSCBEN.* This bit is exclusively used to DMA bytes into the Scatter/Gather SRAM. The CCSCBEN bit is exclusively used to DMA SCBs into the command channel SCB SRAM or DMA bytes (status) from the command channel SCB SRAM to system memory.
2	(0)	(r)	RSVD	Always reads 0.
1	(0)	(r/w)	FLAG	Read write bit only. Has no other function.

Bit			Name	Definition
0	(0)	(r/w)	CCSGRESET	**Command Channel Scatter/Gather SRAM Reset Bit**. When written (=1), forces the Command channel Scatter/Gather SRAM address pointer to a value of 0. This bit is self-clearing. Note that it is illegal to assert CCSGRESET while the Scatter/Gather DMA channel operation is happening.

Command Channel SCB RAM Data Port (CCSCBRAM)

Type:R/W
Address:M-ECh, DS-ECh

CCSCBRAM. This register is a port to the Command channel SCB SRAM area. For DMA transfers between host memory and this SRAM, **CCHADDR**[7:0] and **CCHCNT** must be first initialized with the system memory address and the count of the number of bytes to be transferred via DMA. The DMA channel can then be enabled by writing a 9h value to register **CCSCBCTL** (**CCSCBRESET** = 1, and **CCSCBEN** = 1). Writing a 1 value to bit **CCSCBRESET** resets the SCB SRAM address pointer to zero. Writing a 1 value to bit **CCSCBEN** enables the DMA transfer. For every byte transferred between the system memory and the SCB SRAM counter **CCSCBADR** will increment by one and **CCHCNT** will decrement by one. For host writers to this SRAM, **CCSCBADR** is first initialized and a stream of bytes are sent to this register. For Sequencer reads from this SRAM, **CCSCBADR** if first initialized and then bytes are read from this register. The host is allowed to write to or read from this port. The Sequencer is not allowed to access this **CCSCBRAM** dataport when the SCB DMA channel is active. It must check for **CCSCBDONE** status = 1 before accessing it. Accessing **CCSCBRAM** dataport when SCB DMA is in progress will corrupt the DMA transfer. On the other hand, the Sequencer is allowed to access **CCSGRAM** dataport.

CCSCBRAM R/W	
7	CCSCBRAM7
6	CCSCBRAM6
5	CCSCBRAM5
4	CCSCBRAM4
3	CCSCBRAM3
2	CCSCBRAM2
1	CCSCBRAM1
0	CCSCBRAM0

Command Channel SCB RAM Address Pointer (CCSCBADR)

Type:R/W
Address:M-EDh, DS-EDh

CCSCBADR. This register contains the address of the SCB SRAM that will be used to either write or read data. The contents of this register increments automatically by one for every byte written or read by either DMA write transfers, host PIO read/write transfers, or Sequencer read/write transfers. **CCSCBADR** is cleared to 0h by **PCIRST#**, **CHIPRST**, or **CCSCBRESET**.

CCSCBADR R/W	
7	CCSCBADR7
6	CCSCBADR6
5	CCSCBADR5
4	CCSCBADR4
3	CCSCBADR3
2	CCSCBADR2
1	CCSCBADR1
0	CCSCBADR0

Command Channel SCB Control (CCSCBCTL)

Type:R/W
Address:M-EEh, DS-EEh

CCSCBCTL. This register provides Command channel hardware control. It is exclusively used to DMA SCB's into the Command channel SCB SRAM or DMA out to the host from the Command channel SCB SRAM status bytes.When PCIRST# or CHIPRST is active, all CCSCBCTL register bits are forced to zero.

CCSCBCTL R/W	
7	CCSCBDONE
6	ARRDONE
5	RSVD
4	CCARREN[ACK]
3	CCSCBEN[ACK]
2	CCSCBDIR[ACK]
1	RSVD
0	CCSCBRESET

Bit			Name	Definition
7	(0)	(r)	CCSCBDONE	**SCB Command Channel Done.** When active (=1), indicates that data has been completely moved between system memory and the Command channel SCB SRAM (either direction). CCSCBDONE is set when CCHCNT has expired (=0).
6	(0)	(r)	ARRDONE	**SCB Array Prefetch Done.** When active (=1), indicates that data has been completely moved between the Command channel SCB SRAM and the SCB array. It is set when CCSCBCNT has expired (=0).
5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r/w)	CCARREN[ACK]	**SCB Array DMA Enable/SCB Array DMA Enable Acknowledge.** When this bit is active (=1), it enables transfers between the Command channel SCB SRAM block and the SCB array. Reading this bit (CCARRENACK) provides status which indicates the state of the hardware. When this bit is cleared, it must be read back as zero before the transfer is guaranteed to have halted.

Bit			Name	Definition
3	(0)	(r/w)	CCSCBEN[ACK]	Command Channel SCB SRAM Transfer Enable/Acknowledge. When this bit is active (=1), it enables transfers between the system memory and the SCB SRAM. Clearing this bit will cleanly halt the transfer. Reading this bit (CCSCBACK) provides status which indicates the state of the hardware. When this bit is cleared it must be read back as zero before the transfer is guaranteed to have halted. The Sequencer firmware should never enable two DMA transfers at the same time into the command channel by setting both the enable bits, CCSGEN and CCSBEN. This bit is exclusively used to DMA bytes between system memory and the command channel SCB SRAM depending on the value of bit SSSCBDIR. The CCSGEN bit is exclusively used to DMA Scatter/Gather list elements from the system memory into the Command channel Scatter/Gather SRAM.
2	(0)	(r/w)	CCSCBDIR[ACK]	**Command Channel SCB SRAM Data Path Direction.** When active (=1), will condition data transfers to be from the PCI bus (system memory) to the Command channel SCB SRAM and from the Command channel SCB SRAM to the SCB array. The Direction bit when not active (=0), will condition data transfers to be from the Command channel SCB SRAM to the PCI bus (system memory). When both CCARRENACK and CCSCBENACK are inactive, the Sequencer may both read and write CCSCBRAM without regard for the state of the CCSCBDIR bit. The state of CCSCBDIRACK will not change unless the enable bits (bits 3 and 4) are cleared.
1	(0)	(r)	RSVD	Always reads 0.
0	(0)	(r/w)	CCSCBRESET	Command Channel SCB SRAM Reset. When written (=1), will force the Command channel SCB SRAM address pointer to a value of 0. This bit is self-clearing.

Command Channel SCB Count (CCSCBCNT)

Type:R/W
Address:M-EFh, DS-EFh

CCSCBCNT. The Command channel SCB array count register contains a count of the number of bytes to be transferred between the Command channel SCB SRAM and the SCB array when this path is enabled via bit CCARREN (=1). CCSCBCNT perform as count down counters and count down by one for each byte transferred between the Command channel SCB SRAM and the SCB array. Transfers are inhibited when the count value of CCSCBCNT is zero.

Note: Any value written to CCHCNT is also written to CCSCBCNT if and only if CCARREN in CCSCBCTL register is inactive (=0).

CCSCBCNT R/W	
7	CCSCBCNT7
6	CCSCBCNT6
5	CCSCBCNT5
4	CCSCBCNT4
3	CCSCBCNT3
2	CCSCBCNT2
1	CCSCBCNT1
0	CCSCBCNT0

Command Channel SCB Base Address (SCBBADDR)

Type:R/W
Address:M-F0h, DS-F0h

This register contains the base address of SCBs allowing relocation of 256 SCBs (16k) in one of two 16K pages when SCBs are located external to the AIC-7890A/91. Please see definition of RAMPSM and INTSCBRAMSEL bits in host DSCOMMAND0 registers. When SCBs are located internal to the AIC-7890A/91, this register does not provide any address bits for the SCB array address.

SCBBADDR R/W	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	RSVD
0	SCBBADDR0

Command Channel SCB Pointer (CCSCBPTR)

Type:R/W
Address:M-F1h, DS-F1h

This register provides the page address to the SCB array. This register is exclusively used in DMA operations to move data (SCBs) from system memory to the SCB array. The data value loaded in this register selects a page of 64 registers within the SCB address range when SCBs are located either internal or external to the AIC-7890A/91.

CCSCBPTR R/W	
7	CCSCBPTR7
6	CCSCBPTR6
5	CCSCBPTR5
4	CCSCBPTR4
3	CCSCBPTR3
2	CCSCBPTR2
1	CCSCBPTR1
0	CCSCBPTR0

Host New SCB Queue Offset (HNSCB_QOFF)

Type:R/W
Address:M-F4h, DS-F4h

The Host New SCB Queue Offset register and the Sequencer New SCB Queue Offset register are used as a SCB delivery mechanism between the host and the sequencer. This delivery mechanism indicates if there are SCBs available for the sequencer to process and if so, how many. Only the system host can read from or write to this register. This register may be accessed any time without consideration of the state of the PAUSEACK bit

HNSCB_QOFF R/W	
7	HNSCB_QOFF07
6	HNSCB_QOFF06
5	HNSCB_QOFF05
4	HNSCB_QOFF04
3	HNSCB_QOFF03
2	HNSCB_QOFF02
1	HNSCB_QOFF01
0	HNSCB_QOFF00

Sequencer New SCB Queue Offset (SNSCB_QOFF)

Type:R/W
Address:M-F6h, DS-F6h

The Sequencer New SCB Queue Offset register and the Host New SCB Queue Offset register are used as a SCB delivery mechanism between the host and the sequencer. This register is typically read by the sequencer. A read operation of this register increments the value by 1. This register can also be written to by the sequencer or the host. When written to in this manner, the new value becomes the valid value. This write operation is typically used for initialization or diagnostic purposes. This delivery mechanism indicates if there are SCBs available for the sequencer to process and if so, how many. The maximum value of this register is set by the QOFF_CTLSTA register. When the value in this register is zero, SNSCB_ROLLOVER bit is set.

SNSCB_QOFF R/W	
7	SNSCB_QOFF07
6	SNSCB_QOFF06
5	SNSCB_QOFF05
4	SNSCB_QOFF04
3	SNSCB_QOFF03
2	SNSCB_QOFF02
1	SNSCB_QOFF01
0	SNSCB_QOFF00

Sequencer Done SCB Queue Offset (SDSCB_QOFF)

Type:R/W
Address:M-F8h, DS-F8h

The Sequencer Done SCB Queue Offset register is used as part of the Done SCB Queue for the sequencer. This register is typically read by the sequencer. A read operation of this register increments the value by 1. This register can also be written to by the sequencer or the host. When written to in this manner, the new value becomes the valid value. This write operation is only used for diagnostic purposes. This register is used to indicate how many Done SCBs have been sent to the host. The maximum value of this register is set by the QOFF_CTLSTA register. When the value in this register is zero, SDSCB_ROLLOVER bit is set.

SDSCB_QOFF R/W	
7	SDSCB_QOFF07
6	SDSCB_QOFF06
5	SDSCB_QOFF05
4	SDSCB_QOFF04
3	SDSCB_QOFF03
2	SDSCB_QOFF02
1	SDSCB_QOFF01
0	SDSCB_QOFF00

Queue Offset Control & Status (QOFF_CTLSTA)

Type:R/W
Address:M-FAh, DS-FAh

The Queue Offset Control and Status register is used to determine the maximum count value in the Sequencer New SCB Queue Offset register and Sequencer Done SCB Queue Offset register which are used to detect roll-over conditions. The firmware sets a value in this register at system initialization.

QOFF_CTLSTA R/W	
7	RSVD
6	SCB_AVAIL
5	SNSCB_ROLLOVER
4	SDSCB_ROLLOVER
3	RSVD
2	SCB_QSIZE2
1	SCB_QSIZE1
0	SCB_QSIZE0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6	(0)	(r)	SCB_AVAIL	**SCB Available** - When active (=1), indicates there are SCBs available for the sequencer to process. This means that there is a difference between the values in the Host New SCB Queue Offset (HNSCB_QOFF) register and the Sequencer New SCB Queue Offset (SNSCB_QOFF) register.
5	(0)	(r)	SNSCB_ROLLOVER	**Sequencer New SCB Queue Roll-over** - When active (=1), indicates that the value in the Sequencer New SCB Queue Offset register is zero. This condition is caused by a reset or when the register rolls over to zero. The firmware can use this bit to reset the base address of the software pointers.
4	(0)	(r)	SDSCB_ROLLOVER	**Sequencer Done SCB Queue Roll-over** - When active (=1), indicates that the value in the Sequencer Done SCB Queue Offset register is zero. This condition is caused by a reset or when the register rolls over to zero. The firmware can use this bit to reset the base address of the software pointers.
3	(0)	(r)	RSVD	Always reads 0.

Bit			Name	Definition
2-0	(0)	(r/w)	SCB_QSIZE[2:0]	**SCB Queue Size[2:0]** - These bits set the New SCB System Memory Queue Size and the Done SCB System Memory Queue Size. The queue size determines the maximum count value in the Sequencer New SCB Queue Offset register and the Sequencer Done SCB Queue Offset register which is used to determine a roll-over condition. See the following table for the queue sizes that are supported.

SCB_QSIZE[2:0]	Queue Size	SNSCB_QOFF_REG or SD_QOFF_REG
000	4 Elements (default)	xxxx_xx00 ==> RollOver = 1
001	8 Elements	xxxx_x000 ==> RollOver = 1
010	16 Elements	xxxx_0000 ==> RollOver = 1
011	32 Elements	xxx0_0000 ==> RollOver = 1
100	64 Elements	xx00_0000 ==> RollOver = 1
101	128 Elements	x000_0000 ==> RollOver = 1
110	256 Elements	0000_0000 ==> RollOver = 1
111	RSVD (Map to 256)	0000_0000 ==> RollOver = 1

Data FIFO Threshold (DFF_THRSH)

Type:R/W
Address:M-FBh, DS-FBh

The Data FIFO Threshold register provides the threshold levels in the Data FIFO that initiate PCI Data Channel DMA operations in both read and write transfers. DFTHRSH bit of DFSTATUS register is active as long as the threshold condition is met.

DFF_THRSH R/W	
7	RSVD
6	WR_DFTHRSH2
5	WR_DFTHRSH1
4	WR_DFTHRSH0
3	RSVD
2	RD_DFTHRSH2
1	RD_DFTHRSH1
0	RD_DFTHRSH0

Bit			Name	Definition
7	(0)	(r)	RSVD	Always reads 0.
6-4	(0)	(r/w)	WR_DFTHRSH[2:0]	**Data FIFO Threshold Select in the Write Direction.** The value stored in the WR_THRSH[2:0] bits along with CACHETHEN bit determines when AIC-7890A/91's PCI master starts and ends a DMA data transfer from the data FIFO to the system memory. See the tables below for different combinations and conditions.
3	(0)	(r)	RSVD	Always reads 0.
2-0	(0)	(r/w)	RD_DFTHRSH[2:0]	**Data FIFO Threshold Select in the Read Direction.** The value stored in the RD_THRSH[2:0] bits along with CACHETHEN bit determines when AIC-7890A/91's PCI master starts and ends a DMA data transfer from the system memory to the data FIFO. See the tables below for different combinations and conditions.

Table 4-1. CACHETHEN = 0, Transfer from Data FIFO to System Memory

WR_DFTHRSH [2:0]	DMA Start (amount of data in Data FIFO)	DMAStop
000	32 Bytes	Empty
001	128 Bytes (25% Full)	Empty
010	256 Bytes (50% Full)	Empty
011	320 Bytes (62.5% Full)	Empty
100	384 Bytes (75% Full)	Empty
101	432 Bytes (~85% Full)	Empty
110	464 Bytes (~90% Full)	Empty
111	480 Bytes (Full - 32 bytes space)	Empty

Table 4-2. CACHETHEN = 0, Transfer from System Memory to Data FIFO

RD_DFTHRSH [2:0]	DMA Start (amount of space in Data FIFO)	DMA Stop
000	32 Bytes	Full
001	128 Bytes (25% Empty)	Full
010	256 Bytes (50% Empty)	Full
011	320 Bytes (62.5% Empty)	Full
100	384 Bytes (75% Empty)	Full
101	432 Bytes (~85% Empty)	Full
110	464 Bytes (~90% Empty)	Full
111	480 Bytes (32 bytes data)	Full

Table 4-3. CACHETHEN = 1, Transfer from Data FIFO to System Memory

	Transfer from Data FIFO to System Memory (AIC-7890A/91 writes as a PCI master)							
	Start (amount of data in Data FIFO)							Stop (amount of data in Data FIFO)
Cache Line Size (bytes)	0	16	32	64	128	256	512	Any Cache Line Size
WR_DFTHRSH[2:0] = 000	*	1#	1#	1#	1#	1#	1#a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 001	*	8	4	2	1	1	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 010	*	16	8	3	2	1	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 011	*	20	10	4	2	1	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 100	*	24	12	5	3	2a	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 101	*	27	13	6	3	2a	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 110	*	29	14	7	4a	2a	1a	Less than 1 cache line size
WR_DFTHRSH[2:0] = 111	*	30	15	8a	4a	2a	1a	Less than 1 cache line size

* Same as when cachethen = 0
\# AIC-7890A/91 stops PCI transfer at the boundary of every cache line size.
a Threshold trigger level is 511 bytes.

Table 4-4. CACHETHEN = 1, Transfer from System Memory to Data FIFO

	Transfer from System Memory to Data FIFO (AIC-7890A/91 reads as a PCI master)							
	Start (amount of space in Data FIFO)							Stop (amount of space in Data FIFO)
Cache Line Size (bytes)	0	16	32	64	128	256	512	Any Cache Line Size
RD_DFTHRSH[2:0] = 000	*	1#	1#	1#	1#	1#	1#a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 001	*	8	4	2	1	1	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 010	*	16	8	3	2	1	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 011	*	20	10	4	2	1	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 100	*	24	12	5	3	2a	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 101	*	27	13	6	3	2a	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 110	*	29	14	7	4a	2a	1a	Less than 1 cache line size
RD_DFTHRSH[2:0] = 111	*	30	15	8a	4a	2a	1a	Less than 1 cache line size

* - Same as when cachethen = 0
\# - AIC-7890A/91 stops PCI transfer at the boundary of every cache line size.
a - Threshold trigger level is 511 bytes.

SG Cache Pointer (SG_CACHEPTR)

Type:R/W
Address: M-FCh, DS-FCh

The Scatter/Gather Cache pointer register contains the Scatter/Gather list management information to the shadow level. Sequencer firmware identifies this as **SG_CACHE_PRE** register when WRITE to this register, and identifies this as **SG_CACHE_SHADOW** register when READ from this register. This register will be loaded by the sequencer at the same time as **HADDR** and **HCNT**, when **PRELOAD_AVL** bit is active, and its contents will drop to the shadow level at the same as the drop of **HADDR** and **HCNT**.

SG_CACHEPTR R/W	
7	SG_CACHEPTR7
6	SG_CACHEPTR6
5	SG_CACHEPTR5
4	SG_CACHEPTR4
3	SG_CACHEPTR3
2	SG_CACHEPTR2
1	SG_CACHEPTR1
0	SG_CACHEPTR0

Bit			Name	Definition
7-2	(0)	(r/w)	SG_CACHEPTR[7:2]	Write only at the Preload level. Read only at the Shadow level. These bits are all passed along with the Scatter/Gather segment. PCI address and transfer length from the preload level to the shadow level.
1	(0)	(r/w)	SG_CACHEPTR[1]	Write only at the Preload level. Read only at the Shadow level. This bit is identified as LAST_SEG by the sequencer. It is set to '1' when the Sequencer loads the last Scatter/Gather list element into the preload level.
0		(w)	Not used	Undefined.
	(0)	(r)	SG_CACHEPTR[0]	LAST SEGMENT DONE status bit. This bit is set to '1' when both Host and SCSI have reached last DMA segment done status.

Device Registers in the Alternate Mode (ALT_MODE = 1)

Bus Free Counter (BUSFREE[3:0])

Type:R
Address:M-03h~00h, DS-03h~00h (alternate)

This read only register increments every 100 nsec if the SCSI bus is free and the PFREG_ENABLE signal is true.

BUSFREE3 R M/DS 03h (alt)	BUSFREE2 R M/DS 02h (alt)	BUSFREE1 R M/DS 01h (alt)	BUSFREE0 R M/DS 00h (alt)
7 BFREE31	7 BFREE23	7 BFREE15	7 BFREE07
6 BFREE30	6 BFREE22	6 BFREE14	6 BFREE06
5 BFREE29	5 BFREE21	5 BFREE13	5 BFREE05
4 BFREE28	4 BFREE20	4 BFREE12	4 BFREE04
3 BFREE27	3 BFREE19	3 BFREE11	3 BFREE03
2 BFREE26	2 BFREE18	2 BFREE10	2 BFREE02
1 BFREE25	1 BFREE17	1 BFREE09	1 BFREE01
0 BFREE24	0 BFREE16	0 BFREE08	0 BFREE00

Bus BSY Counter (BUSBSY[3:0])

Type:R
Address:M-07h~04hh, DS-07h~04hh (alternate)

This read only register increments every 100 nsec if the SCSI bus is not free and the PFREG_ENABLE signal is true.

BUSBSY3 R M/DS 07h (alt)	BUSBSY2 R M/DS 06h (alt)	BUSBSY1 R M/DS 05h (alt)	BUSBSY0 R M/DS 04h (alt)
7 BBSY31	7 BBSY23	7 BBSY15	7 BBSY07
6 BBSY30	6 BBSY22	6 BBSY14	6 BBSY06
5 BBSY29	5 BBSY21	5 BBSY13	5 BBSY05
4 BBSY28	4 BBSY20	4 BBSY12	4 BBSY04
3 BBSY27	3 BBSY19	3 BBSY11	3 BBSY03
2 BBSY26	2 BBSY18	2 BBSY10	2 BBSY02
1 BBSY25	1 BBSY17	1 BBSY09	1 BBSY01
0 BBSY24	0 BBSY16	0 BBSY08	0 BBSY00

Frequency Synthesizer Control 0 (FRQSYNCTL0)

Type:R/W
Address:M-10h, DS-10h (alternate)

At reset the values in this register are preset assuming a 40-MHz reference clock and an 80-MHz output.

FRQSYNCTL0 R/W	
7	EXT_CLK_PRSNT
6	FRQSYN_EN
5	FRQSYN_FCNT5
4	FRQSYN_FCNT4
3	FRQSYN_FCNT3
2	FRQSYN_FCNT2
1	FRQSYN_FCNT1
0	FRQSYN_FCNT0

Bit			Name	Definition
7	(x)	(r)	EXT_CLK_PRSNT	(Read Only) An active, switching signal is present at the AIC-7890A/91's SCSICLK input. Valid signals are a 66 MHz clock, Vdd, or Ground.
6	(1)	(r/w)	FRQSYN_EN	**Synthesizer Enable**. When set to 1 the PLL is powered up and enabled. When 0 PLL is shut down and draws no power.
5-0	(04)	(r/w)	FRQSYN_FCNT[5:0]	**Forward Count Divide**. This value sets the divide between the reference clock and the reference input to the PLL.

Frequency Synthesizer Control 1 (FRQSYNCTL1)

Type:R/W
Address:M-11h, DS-11h (alternate)

At reset the values in this register are preset assuming a 40-MHz reference clock and an 80-MHz output.

FRQSYNCTL0 R/W	
7	FRQSYN_SELPLL
6	FRQSYN_VCOD
5	FRQSYN_BCNT5
4	FRQSYN_BCNT4
3	FRQSYN_BCNT3
2	FRQSYN_BCNT2
1	FRQSYN_BCNT1
0	FRQSYN_BCNT0

Bit			Name	Definition
7	(X)	(r)	FRQSYN_SELPLL	(read Only) When true, indicates that the VCO output clock is being driven by the PLO, when false the output clock is being driven by the Input clock (CLK40).
6	(0)	(r/w)	FRQSYN_VCOD	**VCO Divide**. When 1 G1 frequency is 1/2 VCO frequency, when 0 G1 is equal to VCO frequency.
5-0	(0Ah)	(r/w)	FRQSYN_BCNT[5:0]	**Feedback Divide Count.** (valid values 3 to 65) Sets the VCO output to PLL feed back input ratio.

SCSI Test Control (SCSITEST)

Type:R/W
Address:M-12h, DS-12h (alternate)

This register provides special controls over the selection of SCSICLK and special test features.

SCSITEST R/W	
7	DISABEXT66
6	SELEXT80
5	RSVD
4	BOOSTDISAB
3	CNTRTEST
2	DATALOOPEN
1	RSVD
0	RSVD

Bit			Name	Definition
7	(0)	(r/w)	DISABEXT66	**Disable External 66MHz**. Tells SCSICLK multiplexor NOT to switch over to the external SCSICLK input when 33 MHz transfer is selected. (Switching to the external input will also be automatically disabled if there is not a switching signal present at the SCSICLK input, as indicated by EXT_CLK_PRSNT in the FRQSYNCTL0 register.
6	(0)	(r/w)	SELEXT80	**Select External 80 MHz**. Tells SCSICLK multiplexor to use external SCSICLK input for 80 MHz (rather than using the VCO). The same thing can also be achieved by clearing FRQSYN_EN in the FRQSYNCTL0 register. To use the SCSICLK input at all times rather than the VCO, the DISABEXT66 bit must not be set and there should be a live clock present at SCSICLK as indicated by EXT_CLK_PRSNT in the FRQSYNCTL0 register. If these conditions aren't met then SCSICLK will revert to 40MHz.
5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r/w)	BOOSTDISAB	**SCSI IO Cell Boost Disable**. This affects the SCSI IO cells in LVD IO mode (only). Normally, when the chip drives in LVD mode a bias cancellation circuit kicks in to counter the termination bias designed into LVD. When BOOSTDISAB is asserted, the bias cancellation is disabled.
3	(0)	(r/w)	CNTRTEST	**Counter Test**. A test feature, not for field use. Shortens time period of DIFFSENSE filter and SELTIMEOUT timers to allow more efficient test.
2	(0)	(r/w)	DATALOOPEN	**Data Loop Enable**. Enables the SCSI "data loopback" test feature.

Bit			Name	Definition
1 - 0	(0)	(r)	RSVD	Always read 0.

SCSI Transfer Control 2 (SXFRCTL2)

Type:R/W
Address:M13h, DS-13h (alternate)

This register provides special controls over the operation of the SCSI DMA logic.

SXFRCTL2 R/W	
7	RSVD
6	RSVD
5	RSVD
4	AUTORSTDIS
3	CMDDMAEN
2	ASU2
1	ASU1
0	ASU0

Bit			Name	Definition
7-5	(0)	(r)	RSVD	Always reads 0.
4	(0)	(r/w)	AUTORSTDIS	**Auto Reset Disable.** Normally, when SCSI has been doing a DMA transfer from FIFO to SCSI, at the completion of the transfer SCSI generates an "auto reset" signal to the FIFO. This is to prepare the FIFO for the possibility of incoming SCSI data. The generation of the "auto reset" can be disabled by setting this bit.
3	(0)	(r/w)	CMDDMAEN	**CMD DMA ENABLE.** This affects the Bayonet target mode operation only. If this bit is set, when Bayonet is selected as target and goes to the CMD phase to input a command from the initiator, the command bytes will be put in the FIFO. This allows use of DMA to bring in commands. Note that, if this bit is turned on, the command bytes will be put into the FIFO even if manual or automatic PIO transfers are used to bring in the command bytes rather than a DMA, which will be terribly confusing to whatever software next tries to set up a DMA.
2:0	(02h)	(r/w)	ASU[2:0]	**ASYNCHRONOUS SETUP.** Applies to SCSI DMA transfers using asynchronous transfer speed. The number here plus 3 is the number of SCSICLKs of setup time given when transferring data asynchronously (for example, the default setting of 2 gives 5 SCSICLKs of setup time). This does not affect asynchronous transfers carried out by the manual or automatic PIO modes.

SCSI IOCell Powerdown Control (IOPDNCTL)

Type:R/W
Address:M14h, DS-14h (alternate)

This register allows various IO cell bias generators to be placed in powerdown mode for IDDQ testing. This register is not intended to be used in normal operation. Where certain cells are not required to be powered for certain operating modes (for example, LVD or SE mode) then they are powered down automatically by other logic, not by writing to this register.

SXFRCTL2 R/W	
7	RSVD
6	RSVD
5	RSVD
4	PDN_LBGDMTL
3	PDN_VTBIAS
2	PDN_IDIST
1	PDN_BIAS1
0	PDN_DIFFSENSE

Bit			Name	Definition
7 - 5	(0)	(r)	RSVD	Always read 0.
4	(0)	(r/w)	PDN_LBGDMTL	Powers down LBGDMTL cell
3	(0)	(r/w)	PDN_VTBIAS	Powers down VTBIAS cell
2	(0)	(r/w)	PDN_IDIST	Powers down IDIST cell
1	(0)	(r/w)	PDN_BIAS1	Powers down BIAS1 cell
0	(0)	(r/w)	PDN_DIFFSENSE	Powers down DIFFSENSE cell

Sequencer Debug Control Register (SEQDBCTL)

Type:R/W
Address:M-60h, DS-60h

The contents of the SEQDBCTL register may be read and written by the Sequencer or PCI host when SFUNCT[7] = 1.

SEQDBCTL R/W	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	RAMBIST_FAIL
0	RAMBIST_EN

Bit		Name	Definition
7:2	(0)	RSVD	Always reads 0.
1	(0)	RAMBIST_FAIL	**Ram BIST Error.** Writing a 1 to this bit (bit is self clearing) will clear stored RAMBIST_FAIL Status. Reading this bit will provide the stored RAMBIST_FAIL Status. RAMBIST_FAIL status is also cleared when PCIRST# or CHIPRST# is active.
0	(0)	RAMBIST_EN	**RAMBIST Enable.** Ram Bist function starts when this bit is written 1. When function is completed, it will be reset to 0. Should an error be detected, the BIST function will halt prematurely allowing the SEQRAM address, where the error was detected, to be read.

Special Function (SFUNCT)

Type:R/W
Address:M-9Fh, DS-9Fh

SFUNCT bits [7:4] select certain sections of the chip for test purposes. SFUNCT bits [2:0] selects a specific test in that section of the chip. To access PCI configuration space registers of the AIC-7890A/91 through PCI I/O or memory cycles, write 0Eh to the SFUNCT register, and the complete PCI configuration space is mapped to the PCI memory space or memory-mapped I/O space assigned to this chip, starting at the offset of zero. To return to the normal mapping for the device space registers, write 00h to the SFUNCT register. The PCI configuration space registers can only be accessed from the PCI interface, and not by the sequencer through the internal bus.

SFUNCT R/W	
7	ALT_MODE
6	GROUP3
5	GROUP2
4	GROUP1
3	GROUP0
2	TEST2
1	TEST1
0	TEST0

Bit			Name	Definition
7	(0)	(r/w)	ALT_MODE	**Alternate Mode.** When active, the 256-byte device register space is mapped to another page for an additional register space, called alternate mode. When inactive (default), the device register space is called functional mode.
6-3	(0)	(r/w)	GROUP[3:0]	For production test purposes only.
2-0	(0)	(r/w)	TEST[2:0]	For production test purposes only.

PCI DMA Read/Write REQ# GNT# Cycle Count (PF_REQGNTCYCCNT[3:0])

Type:R
Address:M-A3h~A0h, DS-A3h~A0h (alternate)

The PF_REQGNTCYCCNT register indicates the running total count of PCI cycles starting from the time REQ# is asserted to the time (but not including) that GNT# is asserted during PCI DMA data FIFO read/write burst (Memory Read Multiple or Memory Read Line or Memory Write Invalidate) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that PFREG_ENABLE bit must be cleared before reading this register.

PF_REQGNTCYCCNT3 R		PF_REQGNTCYCCNT2 R	
07	PF_REQGNTCYCCNT31	07	PF_REQGNTCYCCNT23
06	PF_REQGNTCYCCNT30	06	PF_REQGNTCYCCNT22
05	PF_REQGNTCYCCNT29	05	PF_REQGNTCYCCNT21
04	PF_REQGNTCYCCNT28	04	PF_REQGNTCYCCNT20
03	PF_REQGNTCYCCNT27	03	PF_REQGNTCYCCNT19
02	PF_REQGNTCYCCNT26	02	PF_REQGNTCYCCNT18
01	PF_REQGNTCYCCNT25	01	PF_REQGNTCYCCNT17
00	PF_REQGNTCYCCNT24	00	PF_REQGNTCYCCNT16

PF_REQGNTCYCCNT1 R		PF_REQGNTCYCCNTR0 R	
07	PF_REQGNTCYCCNT15	07	PF_REQGNTCYCCNT07
06	PF_REQGNTCYCCNT14	06	PF_REQGNTCYCCNT06
05	PF_REQGNTCYCCNT13	05	PF_REQGNTCYCCNT05
04	PF_REQGNTCYCCNT12	04	PF_REQGNTCYCCNT04
03	PF_REQGNTCYCCNT11	03	PF_REQGNTCYCCNT03
02	PF_REQGNTCYCCNT10	02	PF_REQGNTCYCCNT02
01	PF_REQGNTCYCCNT09	01	PF_REQGNTCYCCNT01
00	PF_REQGNTCYCCNT08	00	PF_REQGNTCYCCNT00

Bit			Name	Definition
31-0	(0)	(r)	PF_REQGNTCYCCNT[31:0]	**PCI DMA Read/Write REQ# GNT Cycle Performance Register.** See description above.

PCI DMA-Read Burst Count (PFRD_BURSTCNT[3:0])

Type:R
Address:M-A7~A4h, DS-A7h~A4h (alternate)

The **PFRD_BURSTCNT** register indicates the running total count of PCI DMA data FIFO read requests (Memory Read Line or Memory Read Multiple) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that **PFREG_ENABLE** bit must be cleared before reading this register.

PFRD_BURSTCNT3 R		**PFRD_BURSTCNT2 R**	
07	PFRD_BURSTCNT31	07	PFRD_BURSTCNT23
06	PFRD_BURSTCNT30	06	PFRD_BURSTCNT22
05	PFRD_BURSTCNT29	05	PFRD_BURSTCNT21
04	PFRD_BURSTCNT28	04	PFRD_BURSTCNT20
03	PFRD_BURSTCNT27	03	PFRD_BURSTCNT19
02	PFRD_BURSTCNT26	02	PFRD_BURSTCNT18
01	PFRD_BURSTCNT25	01	PFRD_BURSTCNT17
00	PFRD_BURSTCNT24	00	PFRD_BURSTCNT16

PFRD_BURSTCNT1 R		**PFRD_BURSTCNT0 R**	
07	PFRD_BURSTCNT15	07	PFRD_BURSTCNT07
06	PFRD_BURSTCNT14	06	PFRD_BURSTCNT06
05	PFRD_BURSTCNT13	05	PFRD_BURSTCNT05
04	PFRD_BURSTCNT12	04	PFRD_BURSTCNT04
03	PFRD_BURSTCNT11	03	PFRD_BURSTCNT03
02	PFRD_BURSTCNT10	02	PFRD_BURSTCNT02
01	PFRD_BURSTCNT09	01	PFRD_BURSTCNT01
00	PFRD_BURSTCNT08	00	PFRD_BURSTCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFRD_BURSTCNT[31:0]	**PCI DMA-Read Burst Count Performance Register.** See description above.

PCI DMA-Read Double Word Transfer Count (PFRD_DWXFRCNT[3:0])

Type:R
Address:M-ABh~A8h, DS-ABh~A8h (alternate)

The **PFRD_DWXFRCNT** register indicates the running total of PCI double word data transfer count during PCI DMA data FIFO read burst (Memory Read Multiple or Memory Read Line) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that **PFREG_ENABLE** bit must be cleared before reading this register.

PFRD_DWXFRCNT3 **R**		**PFRD_DWXFRCNT2** **R**	
07	PFRD_DWXFRCNT31	07	PFRD_DWXFRCNT23
06	PFRD_DWXFRCNT30	06	PFRD_DWXFRCNT22
05	PFRD_DWXFRCNT29	05	PFRD_DWXFRCNT21
04	PFRD_DWXFRCNT28	04	PFRD_DWXFRCNT20
03	PFRD_DWXFRCNT27	03	PFRD_DWXFRCNT19
02	PFRD_DWXFRCNT26	02	PFRD_DWXFRCNT18
01	PFRD_DWXFRCNT25	01	PFRD_DWXFRCNT17
00	PFRD_DWXFRCNT24	00	PFRD_DWXFRCNT16

PFRD_DWXFRCNT1 **R**		**PFRD_DWXFRCNT0** **R**	
07	PFRD_DWXFRCNT15	07	PFRD_DWXFRCNT07
06	PFRD_DWXFRCNT14	06	PFRD_DWXFRCNT06
05	PFRD_DWXFRCNT13	05	PFRD_DWXFRCNT05
04	PFRD_DWXFRCNT12	04	PFRD_DWXFRCNT04
03	PFRD_DWXFRCNT11	03	PFRD_DWXFRCNT03
02	PFRD_DWXFRCNT10	02	PFRD_DWXFRCNT02
01	PFRD_DWXFRCNT09	01	PFRD_DWXFRCNT01
00	PFRD_DWXFRCNT08	00	PFRD_DWXFRCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFRD_DWXFRCNT[31:0]	**PCI DMA-Read Double Word Transfer Count Performance Register.** See description above.

PCI DMA Read REQ# Count (PFRD_PREQCNT[3:0])

Type:R
Address:M-AFh~ACh, DS-AFh~ACh (alternate)

The PFRD_PREQCNT register indicates the running total count of PCI REQ# that was generated during PCI DMA data FIFO read burst (Memory Read Multiple or Memory Read Line) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that PFREG_ENABLE bit must be cleared before reading this register.

PFRD_PREQCNT3 R		PFRD_PREQCNT2 R		PFRD_PREQCNT1 R		PFRD_PREQCNT0 R	
07	PFRD_PREQCNT31	07	PFRD_PREQCNT23	07	PFRD_PREQCNT15	07	PFRD_PREQCNT07
06	PFRD_PREQCNT30	06	PFRD_PREQCNT22	06	PFRD_PREQCNT14	06	PFRD_PREQCNT06
05	PFRD_PREQCNT29	05	PFRD_PREQCNT21	05	PFRD_PREQCNT13	05	PFRD_PREQCNT05
04	PFRD_PREQCNT28	04	PFRD_PREQCNT20	04	PFRD_PREQCNT12	04	PFRD_PREQCNT04
03	PFRD_PREQCNT27	03	PFRD_PREQCNT19	03	PFRD_PREQCNT11	03	PFRD_PREQCNT03
02	PFRD_PREQCNT26	02	PFRD_PREQCNT18	02	PFRD_PREQCNT10	02	PFRD_PREQCNT02
01	PFRD_PREQCNT25	01	PFRD_PREQCNT17	01	PFRD_PREQCNT09	01	PFRD_PREQCNT01
00	PFRD_PREQCNT24	00	PFRD_PREQCNT16	00	PFRD_PREQCNT08	00	PFRD_PREQCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFRD_PREQCNT[31:0]	**PCI DMA Read REQ# Count Performance Register.** See description above.

PCI DMA-Read Maximum Burst Length (PFRD_MAXBURSTLEN[1:0])

Type:R
Address:M-B1h~B0h, DS-B1h~B0h (alternate)

The PFRD_MACBURSTLEN register records the largest number of PCI read burst data transfer cycles (in DW) that occurred for a given PCI DMA data FIFO burst read (Memory Read Multiple or Memory Read Line) operation. This register will automatically get cleared after reading from it. Note that PFREG_ENABLE bit must be cleared before reading this register.

PFRD_MAXBURSTLEN1 R		PFRD_MAXBURSTLEN0 R	
07	PFRD_MAXBURSTLEN15	07	PFRD_MAXBURSTLEN07
06	PFRD_MAXBURSTLEN14	06	PFRD_MAXBURSTLEN06
05	PFRD_MAXBURSTLEN13	05	PFRD_MAXBURSTLEN05
04	PFRD_MAXBURSTLEN12	04	PFRD_MAXBURSTLEN04
03	PFRD_MAXBURSTLEN11	03	PFRD_MAXBURSTLEN03
02	PFRD_MAXBURSTLEN10	02	PFRD_MAXBURSTLEN02
01	PFRD_MAXBURSTLEN09	01	PFRD_MAXBURSTLEN01
00	PFRD_MAXBURSTLEN08	00	PFRD_MAXBURSTLEN00

Bit			Name	Definition
15-0	(0)	(r)	PFRD_MAXBURSTLEN[15:0]	PCI DMA-Read Maximum Burst Length Performance Register. See description above.

PPCI DMA-Write Burst Count (PFWR_BURSTCNT[3:0])

Type:R
Address:M-B7h~B4h, DS-B7h~B4h (alternate)

The PFWR_BURSTCNT register indicates the running total count of PCI DMA data FIFO write requests (Memory Write Invalidate) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that PFREG_ENABLE bit must be cleared before reading this register.

PFWR_BURSTCNT3 R		PFWR_BURSTCNT2 R		PFWR_BURSTCNT1 R		PFWR_BURSTCNT0 R	
07	PFWR_BURSTCNT31	07	PFWR_BURSTCNT23	07	PFWR_BURSTCNT15	07	PFWR_BURSTCNT07
06	PFWR_BURSTCNT30	06	PFWR_BURSTCNT22	06	PFWR_BURSTCNT14	06	PFWR_BURSTCNT06
05	PFWR_BURSTCNT29	05	PFWR_BURSTCNT21	05	PFWR_BURSTCNT13	05	PFWR_BURSTCNT05
04	PFWR_BURSTCNT28	04	PFWR_BURSTCNT20	04	PFWR_BURSTCNT12	04	PFWR_BURSTCNT04
03	PFWR_BURSTCNT27	03	PFWR_BURSTCNT19	03	PFWR_BURSTCNT11	03	PFWR_BURSTCNT03
02	PFWR_BURSTCNT26	02	PFWR_BURSTCNT18	02	PFWR_BURSTCNT10	02	PFWR_BURSTCNT02
01	PFWR_BURSTCNT25	01	PFWR_BURSTCNT17	01	PFWR_BURSTCNT09	01	PFWR_BURSTCNT01
00	PFWR_BURSTCNT24	00	PFWR_BURSTCNT16	00	PFWR_BURSTCNT08	00	PFWR_BURSTCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFWR_BURSTCNT[31:0]	**PCI DMA-Write Burst Count Performance Register.** See description above.

PCI DMA-Write Double Word Transfer Count (PFWR_DWXFRCNT[3:0])

Type:R
Address:M-BBh~B8h, DS-BBh~B8h (alternate)

The **PFWR_DWXFRCNT** register indicates the running total number of PCI double word data transfer that has occurred during PCI DMA data FIFO write burst (Memory Write Invalidate) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that **PFREG_ENABLE** bit must be cleared before reading this register.

PFWR_DWXFRCNT3 R		PFWR_DWXFRCNT2 R		PFWR_DWXFRCNT1 R		PFWR_DWXFRCNT0 R	
07	PFWR_DWXFRCNT31	07	PFWR_DWXFRCNT23	07	PFWR_DWXFRCNT15	07	PFWR_DWXFRCNT07
06	PFWR_DWXFRCNT30	06	PFWR_DWXFRCNT22	06	PFWR_DWXFRCNT14	06	PFWR_DWXFRCNT06
05	PFWR_DWXFRCNT29	05	PFWR_DWXFRCNT21	05	PFWR_DWXFRCNT13	05	PFWR_DWXFRCNT05
04	PFWR_DWXFRCNT28	04	PFWR_DWXFRCNT20	04	PFWR_DWXFRCNT12	04	PFWR_DWXFRCNT04
03	PFWR_DWXFRCNT27	03	PFWR_DWXFRCNT19	03	PFWR_DWXFRCNT11	03	PFWR_DWXFRCNT03
02	PFWR_DWXFRCNT26	02	PFWR_DWXFRCNT18	02	PFWR_DWXFRCNT10	02	PFWR_DWXFRCNT02
01	PFWR_DWXFRCNT25	01	PFWR_DWXFRCNT17	01	PFWR_DWXFRCNT09	01	PFWR_DWXFRCNT01
00	PFWR_DWXFRCNT24	00	PFWR_DWXFRCNT16	00	PFWR_DWXFRCNT08	00	PFWR_DWXFRCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFWR_DWXFRCNT[31:0]	**PCI DMA-Write Double Word Transfer Count Performance Register.** See description above.

PCI DMA Write REQ# Count (PFWR_PREQCNT[3:0])

Type:R
Address:M-BFh~BCh DS-BFh-BCh (alternate)

The PFWR_PREQCNT register indicates the running total number of PCI REQ# that was generated during PCI DMA data FIFO write burst (Memory Write Invalidate) operation. This register will wrap-around to 0 after its 4 byte counter reaches above its maximum count value of FFFF_FFFF_FFFF_FFFF. Note that PFREG_ENABLE bit must be cleared before reading this register.

PFWR_PREQCNT3 R		PFWR_PREQCNT2 R		PFWR_PREQCNT1 R		PFWR_PREQCNT0 R	
07	PFWR_PREQCNT31	07	PFWR_PREQCNT23	07	PFWR_PREQCNT15	07	PFWR_PREQCNT07
06	PFWR_PREQCNT30	06	PFWR_PREQCNT22	06	PFWR_PREQCNT14	06	PFWR_PREQCNT06
05	PFWR_PREQCNT29	05	PFWR_PREQCNT21	05	PFWR_PREQCNT13	05	PFWR_PREQCNT05
04	PFWR_PREQCNT28	04	PFWR_PREQCNT20	04	PFWR_PREQCNT12	04	PFWR_PREQCNT04
03	PFWR_PREQCNT27	03	PFWR_PREQCNT19	03	PFWR_PREQCNT11	03	PFWR_PREQCNT03
02	PFWR_PREQCNT26	02	PFWR_PREQCNT18	02	PFWR_PREQCNT10	02	PFWR_PREQCNT02
01	PFWR_PREQCNT25	01	PFWR_PREQCNT17	01	PFWR_PREQCNT09	01	PFWR_PREQCNT01
00	PFWR_PREQCNT24	00	PFWR_PREQCNT16	00	PFWR_PREQCNT08	00	PFWR_PREQCNT00

Bit			Name	Definition
31-0	(0)	(r)	PFWR_PREQCNT[31:0]	**PCI DMA Write REQ# Count Performance Register.** See description above.

PCI DMA-Write Maximum Burst Length (PFWR_MAXBURSTLEN[1:0])

Type:R
Address:M-C1h~C0h, DS-C1h~C0h (alternate)

The PFWR_MACBURSTLEN register records the largest number of PCI write burst data transfer cycles (in DW) that occurred for a given PCI DMA data FIFO burst write (Memory Write Invalidate) operation. This register automatically gets cleared after reading from it. Note that PFREG_ENABLE bit must be cleared before reading this register.

PFWR_MAXBURSTLEN1 R		PFWR_MAXBURSTLEN0 R	
07	PFWR_MAXBURSTLEN15	07	PFWR_MAXBURSTLEN07
06	PFWR_MAXBURSTLEN14	06	PFWR_MAXBURSTLEN06
05	PFWR_MAXBURSTLEN13	05	PFWR_MAXBURSTLEN05
04	PFWR_MAXBURSTLEN12	04	PFWR_MAXBURSTLEN04
03	PFWR_MAXBURSTLEN11	03	PFWR_MAXBURSTLEN03
02	PFWR_MAXBURSTLEN10	02	PFWR_MAXBURSTLEN02
01	PFWR_MAXBURSTLEN09	01	PFWR_MAXBURSTLEN01
00	PFWR_MAXBURSTLEN08	00	PFWR_MAXBURSTLEN00

Bit			Name	Definition
15-0	(0)	(r)	PFWR_MAXBURSTLEN[15:0]	**PCI DMA-Write Maximum Burst Length Performance Register.** See description above.

Performance Register Monitoring Control (PF_CNTRL)

Type:R
Address:M-DFh, DS-DFh (alternate)

The PF_CNTRL register allows either sequencer or PCI Host to enable/inhibit Performance Monitoring registers from being updated. The performance Monitoring registers include the following:

BUSFREE[3:0]
BUSBSY[3:0]
PF_REQGNTCYCCNT[3:0]
PFRD_BURSTCNT[3:0]
PFRD_DWXFRCNT[3:0]
PFRD_PREQCNT[3:0]
PFRD_MAXBURSTLEN[1:0]
PFWR_BURSTCNT[3:0]
PFWR_DWXFRCNT[3:0]
PFWR_PREQCNT[3:0]
PFWR_MAXBURSTLEN[1:0]

PF_CNTRL R	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	RSVD
0	PFREG_ENABLE

Bit			Name	Definition
7-1	(0)	(r)	RSVD	Always reads 0.
0	(0)	(r/w)	PFREG_ENABLE	**Performance Registers Enable**. When this bit is set (=1), the Performance registers during both DMA read or write operation will be allowed to count or record information regarding PCI or SCSI transfers such as the number of PCI bursts, number of PCI cycles from PREQ# to GNT#, number of ticks for SCSI busy and SCSI bus free, etc... When this bit is cleared (=0), all updating activity to Performance registers is inhibited. This register bit should be cleared prior to reading any of the Performance registers (either by sequencer or PCI Host). Clearing this bit will also save on power consumption.

Data FIFO Pointer (DFPTRS)

Type:R/W
Address:M-E0h, DS-E0h

In alternate mode, Bit[2:0] of this register contains the value of the Wptr[2:0] (byte offset bits). Bit[5:3] contains the value of the Rptr[2:0](byte offset bits). Bit[7:6] RSVD.

DFPTRS R/W	
7	RSVD
6	RSVD
5	DFRPTR02
4	DFRPTR01
3	DFRPTR00
2	DFWPTR02
1	DFWPTR01
0	DFWPTR00

Bit		Name	Definition
7-6	(X)	RSVD	Always read 0.
5-3	(0)	DFRPTR[2:0]	**Data FIFO Read Pointer[2:0]** The byte offset to the read data port of the Data FIFO.
2-0	(0)	DFWPTR[2:0]	**Data FIFO Write Pointer[2:0]** The byte offset to the write data port of the Data FIFO.

Data FIFO Backup Pointer (DFBKPTR0)

Type:R/W
Address:M-E1h, DS-E1h

The content of the **DFBKPTR0** register may be read and written by the Sequencer or PCI host when SFUNCT[7] = 1b.

DFBKPTR0 R/W	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	DFBKPTR02
1	DFBKPTR01
0	DFBKPTR00

Bit		Name	Definition
7-3	(X)	RSVD	Always reads 0.
2-0	(0)	DFBKPTR[2:0]	**Data FIFO Backup Pointer[2:0].** the byte offset bits of QWD.

Data FIFO Backup Read Pointer (DFBKPTR)

Type:R/W
Address:M-E2h, DS-E2h

In alternate mode, this register contains the 7 MSB of the Backup Rptr, Bit 6 is the roll-over bit. Bit[5:0] point to the row of Data FIFO.

DFBKPTR R/W	
7	RSVD
6	DFBKPTR09
5	DFBKPTR08
4	DFBKPTR07
3	DFBKPTR06
2	DFBKPTR05
1	DFBKPTR04
0	DFBKPTR03

Bit		Name	Definition
7	(X)	RSVD	Always reads 0.
6	(0)	DFBKPTR[9]	**Data FIFO Backup Read Pointer[9]**: roll over bit.
5-0	(0)	DFBKPTR[8:3]	**Data FIFO Backup Read Pointer[8:3]**: point to row of FIFO.

Data FIFO Debug Control (DFDBCTL)

Type: bit [7:3] Read only - bit [2:0] R/W
Address: M-E3h, DS-E3h

The contents of the DFDBCTL register may be read and written by the Sequencer or PCI host when SFUNCT[7] = 1b.

DFDBCTL R/W	
7	RSVD
6	RSVD
5	RSVD
4	DFF_CIO_WR_RDY
3	DFF_CIO_RD_RDY
2	DFF_DIR_ERR
1	DFF_RAMBIST_FAIL
0	DFF_RAMBIST_EN

Bit		Name	Definition
7-5	(X)	RSVD	Always reads 0.
4	(1)	DFF_CIO_WR_RDY	**Data FIFO CIOBus Write Ready:** When this bit set to one, DFF is ready for sequencer writing to it through CIOBus.
3	(1)	DFF_CIO_RD_RDY	**Data FIOF CIOBus Read Ready:** When this bit set to one, DFF is ready for sequencer reading from it through CIOBus.
2	(0)	DFF_DIR_ERR	**Data FIFO Direction Error.** When both SCSI and HST try to write to FIFO this bit shall be set. Write 1 to this bit (bit is self clearing) shall clear stored DFF ERR status.
1	(0)	DFF_RAMBIST_FAIL	**Data FIFO RAMBIST Fail.** Write 1 to this bit (bit is self clearing) will clear stored RAMBIST FAIL Status. Reading this bit will provide the stored RAMBIST FAIL Status.
0	(0)	DFF_RAMBIST_EN	**Data FIFO RAMBIST Enable.** Ram Bist function starts when this bit is written 1. When function is completed, it will be reset to 0. Should an error be detected, the BIST function will halt prematurely allowing the DFF RAM address where the error was detected to be read.

Data FIFO Space Count (DFSCNT0)

Type:R
Address:M-E4h, DS-E4h

DFSCNT0 register contains the value of the low byte of DFF_Space_Cnt value.The contents of the DFSCNT0 register may be read by the Sequencer or PCI host when SFUNCT[7] = 1.

DFSCNT0 R	
7	DFSCNT07
6	DFSCNT06
5	DFSCNT05
4	DFSCNT04
3	DFSCNT03
2	DFSCNT02
1	DFSCNT01
0	DFSCNT00

Bit			Definition
7-0	(0)	DFSCNT[7:0]	**Data FIFO Space Count**. The low byte of DFF_Space_Cnt value.

Data FIFO Space Count (DFSCNT1)

Type:R
Address: M-E5h, DS-E5h

DFSCNT1 register contains the value of the two most significant bit of DFF_Space_Cnt counter. The contents of the DFSCNT1 register may be read by the Sequencer or PCI host when SFUNCT[7] = 1.

DFSCNT1 R	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	DFSCNT09
0	DFSCNT08

Bit			Definition
7-2	(X)	RSVD	Always reads 0.
1	(1)	DFSCNT09	**Data FIFO Space Count bit 9:** The most significant bit of DFF_Space_Cnt counter.

Bit			Definition
0	(0)	DFSCNT08	**Data FIFO Space Count bit 8**: The 8 bit of DFF_Space_Cnt counter

Data FIFO Byte Count (DFBCNT0)

Type:R
Address: M-E6h, DS-E6h

DFBCNT0 register contains the value of the low byte of DFF_Byte_Cnt value.The contents of the DFBCNT0 register may be read by the Sequencer or PCI host when SFUNCT[7] = 1.

DFBCNT0 R	
7	DFBCNT07
6	DFBCNT06
5	DFBCNT05
4	DFBCNT04
3	DFBCNT03
2	DFBCNT02
1	DFBCNT01
0	DFBCNT00

Bit			Definition
7:0	(0)	DFBCNT[7:0]	Data FIFO Byte Count: The low byte of DFF_Byte_Cnt value.

Data FIFO Byte Count (DFBCNT1)

Type:R
Address:M-E7h, DS-E7h

DFBCNT1 register contains the value of the two most significant bit of DFF_Byte_Cnt counter. The contents of the DFBCNT1 register may be read by the Sequencer or PCI host when SFUNCT[7] = 1.

DFBCNT1 R	
7	RSVD
6	RSVD
5	RSVD
4	RSVD
3	RSVD
2	RSVD
1	DFBCNT09
0	DFBCNT08

Bit			Definition
7:2	(X)	RSVD	Always reads 0.
1	(1)	DFBCNT09	**Data FIFO Byte Count bit 9:** The most significant bit of DFF_Byte_Cnt counter.
0	(0)	DFBCNT08	**Data FIFO Byte Count bit 8**: The 8 bit of DFF_Byte_Cnt counter

Command Channel SCB RAM Back-Up Address Pointer (CCSCBADR_BK)

Type:R/W
Address:MEDh, DS-EDh

CCSCBADR_BK. This register contains the backup address of the SCB SRAM for any DMA read from SCB RAM in the Command Channel Block. The contents of this register increments by a number of bytes that have been successfully transferred to host memory in functional mode. Read access is allowed in alternate mode. **CCSCBADR_BK** is cleared to 0h by PCI**RST#**, **CHIPRST**, or **CCSCBRESET**.

CCSCBADR_BK R/W	
7	CCSCBADR_BK7
6	CCSCBADR_BK6
5	CCSCBADR_BK5
4	CCSCBADR_BK4
3	CCSCBADR_BK3
2	CCSCBADR_BK2
1	CCSCBADR_BK1
0	CCSCBADR_BK0

5

Pin Assignment

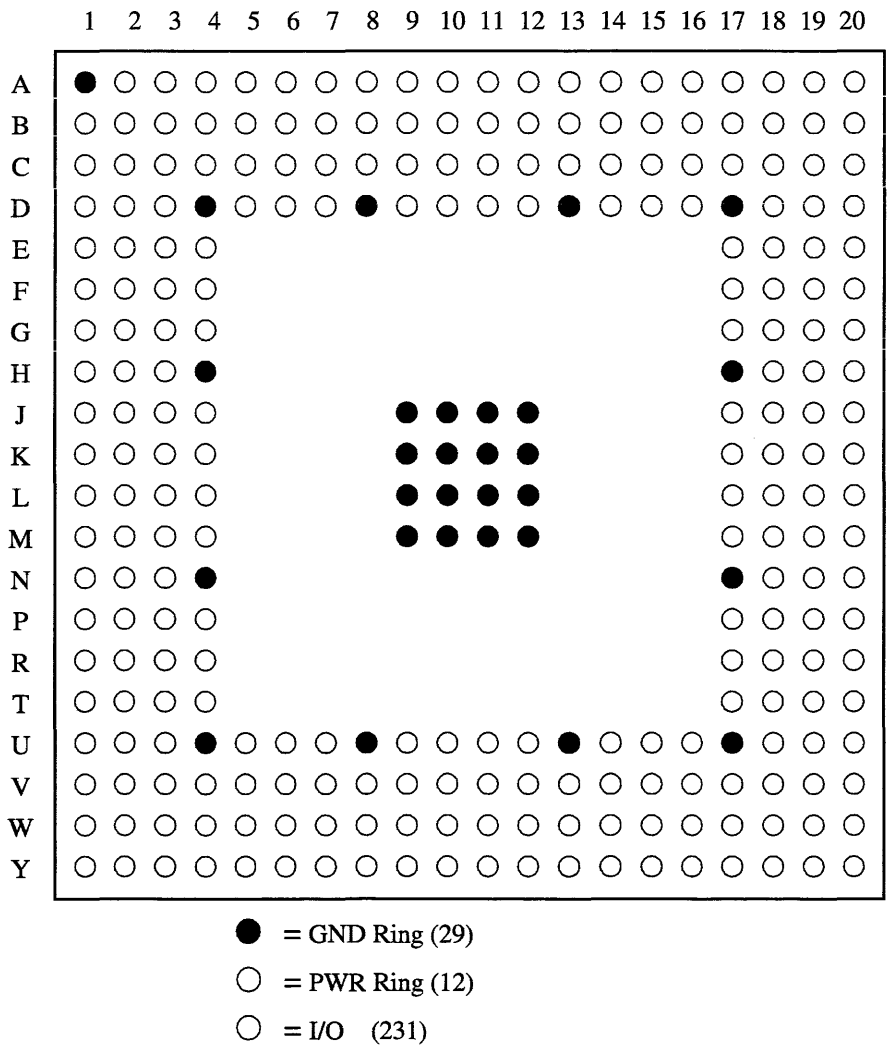


Figure 5-1. Top View of 272-PIN BGA (Ball Grid Array)

AIC-7890A Pinouts

Table 5-1. AIC-7890A Left Side

Pin Name	Type	BGA Pad	Description
SCDP6	I/O	B1	SCSI Data, bit-6, differential plus
SCDM6	I/O	C2	SCSI Data, bit-6, differential minus
SVCC0	P	D2	SCSI Power
SCDP5	I/O	D3	SCSI Data, bit-5, differential plus
SCDM5	I/O	E4	SCSI Data, bit-5, differential minus
GND	G	note 1	SCSI Ground
SCDP4	I/O	C1	SCSI Data, bit-4, differential plus
SCDM4	I/O	D1	SCSI Data, bit-4, differential minus
SCDP3	I/O	E3	SCSI Data, bit-3, differential plus
SCDM3	I/O	E2	SCSI Data, bit-3, differential minus
SVCC1	P	E1	SCSI Power
SCDP2	I/O	F3	SCSI Data, bit-2, differential plus
SCDM2	I/O	G4	SCSI Data, bit-2, differential minus
GND	G	note 1	SCSI Ground
SCDP1	I/O	F2	SCSI Data, bit-1, differential plus
SCDM1	I/O	F1	SCSI Data, bit-1, differential minus
CVCC0	P	G3	Core Power
SCDP0	I/O	G2	SCSI Data, bit-0, differential plus
SCDM0	I/O	G1	SCSI Data, bit-0, differential minus
SVCC2	P	H3	SCSI Power
SCDPHP	I/O	H2	SCSI Data Parity High, differential plus
SCDPHM	I/O	H1	SCSI Data Parity High, differential minus
GND	G	note 1	SCSI Ground
SCDP15	I/O	J4	SCSI Data, bit-15, differential plus
SCDM15	I/O	J3	SCSI Data, bit-15, differential minus
SCDP14	I/O	J2	SCSI Data, bit-14, differential plus
SCDM14	I/O	J1	SCSI Data, bit-14, differential minus
SVCC3	P	K2	SCSI Power
SCDP13	I/O	K3	SCSI Data, bit-13, differential plus
SCDM13	I/O	K1	SCSI Data, bit-13, differential minus
GND	G	note 1	SCSI Ground
SCDP12	I/O	L1	SCSI Data, bit-12, differential plus
SCDM12	I/O	L2	SCSI Data, bit-12, differential minus
GND	G	note 1	Core Ground
GND	G	note 1	Core Ground
PCLK	I	L3	PCI Clock
CVCC1	P	L4	Core Power

Table 5-1. AIC-7890A Left Side (Continued)

Pin Name	Type	BGA Pad	Description
PULLUP1	I	M1	Pull Up
TRST#	I	M2	JTAG Test Reset
N/C	-	M3	PCI Command/Byte Enable, bit-4
N/C	-	M4	No Connect
GND	G	note 1	PCI Ground
TCK	I	N1	JTAG Test Clock
TMS	I	N2	JTAG Test Mode Select
N/C	-	N3	No Connect
PVCC	P	note 2	PCI Power
TDO	O	P1	JTAG Test Output
GND	G	note 1	PCI Ground
TDI	I	P2	JTAG Test Input
PREQ#	O	R1	PCI Request
N/C	-	P3	No Connect
IRQA#	O	R2	PCI Interrupt
GND	G	note 1	PCI Ground
AD31	I/O	T1	PCI Address/Data, bit-31
PVCC	P	note 2	PCI Power
N/C	-	P4	No Connect
N/C	-	R3	No Connect
PCIRST#	I	T2	PCI Reset
GND	G	note 1	PCI Ground
AD29	I/O	U1	PCI Address/Data, bit-29
N/C	-	T3	No Connect
GNT#	I	U2	PCI Grant
PVCC	P	note 2	PCI Power
AD27	I/O	V1	PCI Address/Data, bit-27
GND	G	note 1	PCI Ground
N/C	-	T4	No Connect
PULLUP2	I	U3	Pull Up
AD30	I/O	V2	PCI Address/Data, bit-30
AD25	I/O	W1	PCI Address/Data, bit-25
GND	G	note 1	PCI Ground
N/C	-	V3	No Connect
PVCC	P	note 2	PCI Power
AD28	I/O	W2	PCI Address/Data, bit-28
CBE3#	I/O	Y1	PCI Command/Byte Enable, bit-3

Table 5-2. AIC-7890A Bottom Side

Pin Name	Type	BGA Pad	Description
AD26	I/O	W3	PCI Address/Data, bit-26
GND	G	note 1	PCI Ground
AD23	I/O	Y2	PCI Address/Data, bit-23
AD24	I/O	W4	PCI Address/Data, bit-24
N/C	-	V4	No Connect
N/C	-	U5	No Connect
PVCC	P	note 2	PCI Power
AD21	I/O	Y3	PCI Address/Data, bit-21
GND	G	note 1	PCI Ground
AD19	I/O	Y4	PCI Address/Data, bit-19
N/C	-	V5	No Connect
IDSEL	I	W5	PCI ID Select
N/C	-	Y5	No Connect
N/C	-	V6	No Connect
GND	G	note 1	PCI Ground
N/C	-	U7	No Connect
PVCC	P	note 2	PCI Power
AD22	I/O	W6	PCI Address/Data, bit-22
AD17	I/O	Y6	PCI Address/Data, bit-17
N/C	-	V7	No Connect
GND	G	note 1	PCI Ground
AD20	I/O	W7	PCI Address/Data, bit-20
CVCC2	P	Y7	Core Power
N/C	-	V8	No Connect
AD18	I/O	W8	PCI Address/Data, bit-18
PVCC	P	note 2	PCI Power
CBE2#	I/O	Y8	PCI Command/Byte Enable, bit-2
GND	G	note 1	PCI Ground
N/C	-	U9	No Connect
N/C	-	V9	No Connect
AD16	I/O	W9	PCI Address/Data, bit-16
IRDY#	I/O	Y9	PCI Initiator Ready
GND	G	note 1	PCI Ground
FRAME#	I/O	W10	PCI Frame
PVCC	P	note 2	PCI Power
N/C	-	V10	No Connect
DEVSEL#	I/O	Y10	PCI Device Select
N/C	-	Y11	No Connect
TRDY#	I/O	W11	PCI Target Ready
GND	G	note 1	PCI Ground
N/C	-	V11	No Connect

Table 5-2. AIC-7890A Bottom Side (Continued)

Pin Name	Type	BGA Pad	Description
N/C	-	U11	No Connect
PERR#	I/O	Y12	PCI Parity Error
PVCC	P	note 2	PCI Power
STOP#	I/O	W12	PCI Stop
GND	G	note 1	PCI Ground
N/C	-	V12	No Connect
N/C	-	U12	No Connect
SERR#	O	Y13	PCI System Error
PAR	I/O	W13	PCI Parity for AD[31:0]
GND	G	note 1	PCI Ground
N/C	-	V13	No Connect
PVCC	P	note 2	PCI Power
CBE1#	I/O	Y14	PCI Command/Byte Enable, bit-1
AD15	I/O	W14	PCI Address/Data, bit-15
AD14	I/O	Y15	PCI Address/Data, bit-14
GND	G	note 1	PCI Ground
N/C	-	V14	No Connect
AD13	I/O	W15	PCI Address/Data, bit-13
AD12	I/O	Y16	PCI Address/Data, bit-12
PVCC	P	note 2	PCI Power
GND	G	note 1	Core Ground
N/C	-	U14	No Connect
GND	G	note 1	PCI Ground
N/C	-	V15	No Connect
AD11	I/O	W16	PCI Address/Data, bit-11
N/C	-	Y17	No Connect
N/C	-	V16	No Connect
AD09	I/O	W17	PCI Address/Data, bit-09
GND	G	note 1	PCI Ground
AD10	I/O	Y18	PCI Address/Data, bit-10
PVCC	P	note 2	PCI Power
N/C	-	U16	No Connect
N/C	-	V17	No Connect
CBE0#	I/O	W18	PCI Command/Byte Enable, bit-0
GND	G	note 1	PCI Ground
AD08	I/O	Y19	PCI Address/Data, bit-08
N/C	-	V18	No Connect
AD06	I/O	W19	PCI Address/Data, bit-06
N/C	-	Y20	No Connect

Table 5-3. AIC-7890A Right Side

Pin Name	Type	BGA Pad	Description
PVCC	P	note 2	PCI Power
AD07	I/O	W20	PCI Address/Data, bit-07
GND	G	note 1	PCI Ground
AD04	I/O	V19	PCI Address/Data, bit-04
AD02	I/O	U19	PCI Address/Data, bit-02
N/C	-	U18	No Connect
N/C	-	T17	No Connect
GND	G	note 1	PCI Ground
AD05	I/O	V20	PCI Address/Data, bit-05
PVCC	P	note 2	PCI Power
AD03	I/O	U20	PCI Address/Data, bit-03
N/C	-	T18	No Connect
AD00	I/O	T19	PCI Address/Data, bit-00
GND	G	note 1	PCI Ground
AD01	I/O	T20	PCI Address/Data, bit-01
N/C	-	R18	No Connect
N/C	-	P17	No Connect
PVCC	P	note 2	PCI Power
N/C	-	R19	No Connect
GND	G	note 1	PCI Ground
GND	G	note 1	Memory Ground
PDPUDIS#	I	R20	Pull Down/Pull Up Disable
N/C	-	P18	-
TESTMODE#	I	P19	Test Mode
GND	G	note 1	Core Ground
CVCC3	P	P20	Core Power
MVCC0	P	N18	Memory Power
IDDAT	I	N19	ID Data
GND	G	note 1	Memory Ground
RAMPS#	I/O	N20	RAM Present
SEECS	O	M17	SEEPROM Chip Select
ROMCS#	O	M18	ROM Chip Select
RAMCS#	O	M19	RAM Chip Select
GND	G	note 1	Memory Ground
MRW	O	M20	Memory Read/Write
MVCC1	P	L19	Memory Power
MD0	I/O	L18	Memory Data, bit-0
MA0	O	L20	Memory Address, bit-0
MA1	O	K20	Memory Address, bit-1

Table 5-3. AIC-7890A Right Side (Continued)

Pin Name	Type	BGA Pad	Description
GND	G	note 1	Memory Ground
MA2	O	K19	Memory Address, bit-2
MD1	I/O	K18	Memory Data, bit-1
MD2	I/O	K17	Memory Data, bit-2
MVCC2	P	J20	Memory Power
MA3	O	J19	Memory Address, bit-3
GND	G	note 1	Memory Ground
MD3	I/O	J18	Memory Data, bit-3
MD4	I/O	J17	Memory Data, bit-4
MA4	O	H20	Memory Address, bit-4
MA5	O	H19	Memory Address, bit-5
GND	G	note 1	Memory Ground
MD5	I/O	H18	Memory Data, bit-5
MVCC3	P	G20	Memory Power
MA6	O	G19	Memory Address, bit-6
MA7	O	F20	Memory Address, bit-7
MD6	I/O	G18	Memory Data, bit-6
GND	G	note 1	Memory Ground
GND	G	note 1	Core Ground
MA8	O	F19	Memory Data, bit-3
MA9	O	E20	Memory Address, bit-9
MD7	I/O	G17	Memory Data, bit-7
MVCC4	P	F18	Memory Power
MA10	O	E19	Memory Address, bit-10
GND	G	note 1	Memory Ground
MA11	O	D20	Memory Address, bit-11
EXTARBACK#	I	E18	Acknowledge from External Arbiter
MA12	O	D19	Memory Address, bit-12
MA13	O	C20	Memory Address, bit-13
GND	G	note 1	Memory Ground
EXTARBREQ#	O	E17	Request to External Arbiter
MVCC5	P	D18	Memory Power
MA14	O	C19	Memory Address, bit-14
MA15	O	B20	Memory Address, bit-15
GND	G	note 1	Memory Ground
MDP	I/O	C18	Memory Data Parity
CVCC7	P	B19	Core Power
N/C	-	A20	No Connect

Table 5-4. AIC-7890A Top Side

Pin Name	Type	BGA Pad	Description
LED#	O	A19	LED Output
GND	G	note 1	Memory Ground
BRDWE	O	B18	Board Control Write Enable
BRDOE#	O	B17	Board Control Output Enable
MVCC6	P	C17	Memory Power
GND	G	note 1	Memory Ground
GND	G	note 1	Core Ground
CLKIN	I	D16	Clock Input
CVCC4	P	A18	Core Power
EXTPAUSE#	I	A17	External Sequencer Pause
EXTXCVR#	I	C16	External Transceiver Present
WIDEPS#	I	B16	Wide SCSI Present
EXPACT	I	A16	Expander Active
GND	G	note 1	Core Ground
STPWCTL	O	C15	SCSI Terminator Power Control
GND	G	note 1	Core Ground
GND	G	note 1	Core Ground
SCLKIN	I	D14	SCSI Clock Input
CVCC5	P	B15	Core Power
DIFFSENSE	I	A15	Differential Sense
AVCC0	P	C14	Analog Power
AVCC1	P	B14	Analog Power
SEREXT	O	A14	Analog Input 0
LVREXT	O	C13	Analog Input 1
AGND0	G	B13	Analog Ground
AGND1	G	A13	Analog Ground
AGND2	G	D12	Analog Ground
GND	G	note 1	Core Ground
SCDP11	I/O	C12	SCSI Data, bit-11, differential plus
SCDM11	I/O	B12	SCSI Data, bit-11, differential minus
SVCC4	P	A12	SCSI Power
SCDP10	I/O	B11	SCSI Data, bit-10, differential plus
SCDM10	I/O	C11	SCSI Data, bit-10, differential minus
GND	G	note 1	SCSI Ground
SCDP9	I/O	A11	SCSI Data, bit-9, differential plus
SCDM9	I/O	A10	SCSI Data, bit-9, differential minus
SCDP8	I/O	B10	SCSI Data, bit-8, differential plus
SCDM8	I/O	C10	SCSI Data, bit-8, differential minus
SVCC5	P	D10	SCSI Power

Table 5-4. AIC-7890A Top Side (Continued)

Pin Name	Type	BGA Pad	Description
IOP	I/O	A9	SCSI Input/Output, differential plus
IOM	I/O	B9	SCSI Input/Output, differential minus
GND	G	note 1	SCSI Ground
REQP	I/O	C9	SCSI Request, differential plus
REQM	I/O	D9	SCSI Request, differential minus
CDP	I/O	A8	SCSI Command/Data, differential plus
CDM	I/O	B8	SCSI Command/Data, differential minus
SVCC6	P	C8	SCSI Power
SELP	I/O	A7	SCSI Select, differential plus
SELM	I/O	B7	SCSI Select, differential minus
GND	G	note 1	SCSI Ground
MSGP	I/O	A6	SCSI Message, differential plus
MSGM	I/O	C7	SCSI Message, differential minus
GND	G	note 1	Core Ground
RESETP	I/O	B6	SCSI Reset, differential plus
RESETM	I/O	A5	SCSI Reset, differential minus
SVCC7	P	D7	SCSI Power
ACKP	I/O	C6	SCSI Acknowledge, differential plus
ACKM	I/O	B5	SCSI Acknowledge, differential minus
GND	G	note 1	SCSI Ground
BSYP	I/O	A4	SCSI Busy, differential plus
BSYM	I/O	C5	SCSI Busy, differential minus
ATNP	I/O	B4	SCSI Attention, differential plus
ATNM	I/O	A3	SCSI Attention, differential minus
SVCC8	P	D5	SCSI Power
SCDPLP	I/O	C4	SCSI Data Parity Low, differential plus
SCDPLM	I/O	B3	SCSI Data Parity Low, differential minus
GND	G	note 1	SCSI Ground
SCDP7	I/O	B2	SCSI Data, bit-7, differential plus
SCDM7	I/O	A2	SCSI Data, bit-7, differential minus
CVCC6	P	C3	Core Power

- **Note 1** - All ground pads except analog ground pads are connected to the GND ring in the package. Die pad and GND potential ring are connected to the following BGA ball pads: A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17.
- **Note 2** - The VCC of the PCI I/O Cells are connected to the PWR ring in the package. PWR potential ring are connected to the following BGA ball pads: D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15.

Table 5-5. I/O Ball Location Grids A1-7 through Y1-7 for AIC-7890A

	1	2	3	4	5	6	7
A	GND	SCDM7	ATNM	BSYP	RESETM	MSGP	SELP
B	SCDP6	SCDP7	SCDPLM	ATNP	ACKM	RESETP	SELM
C	SCDP4	SCDM6	CVCC6	SCDPLP	BSYM	ACKP	MSGM
D	SCDM4	SVCC0	SCDP5	GND	SVCC8	PVCC	SVCC7
E	SVCC1	SCDM3	SCDP3	SCDM5	--	--	--
F	SCDM1	SCDP1	SCDP2	PVCC	--	--	--
G	SCDM0	SCDP0	CVCC0	SCDM2	--	--	--
H	SCDPHM	SCDPHP	SVCC2	GND	--	--	--
J	SCDM14	SCDP14	SCDM15	SCDP15	--	--	--
K	SCDM13	SVCC3	SCDP13	PVCC	--	--	--
L	SCDP12	SCDM12	PCLK	CVCC1	--	--	--
M	PULLUP1	TRST#	N/C	N/C	--	--	--
N	TCK	TMS	N/C	GND	--	--	--
P	TDO	TDI	N/C	N/C	--	--	--
R	PREQ#	IRQA#	N/C	PVCC	--	--	--
T	AD31	PCIRST#	N/C	N/C	--	--	--
U	AD29	GNT#	PULLUP2	GND	N/C	PVCC	N/C
V	AD27	AD30	N/C	N/C	N/C	N/C	N/C
W	AD25	AD28	AD26	AD24	IDSEL	AD22	AD20
Y	CBE3#	AD23	AD21	AD19	N/C	AD17	CVCC2

Table 5-6. I/O Ball Location Grids A8-14 through Y8-14 for AIC-7890A

	8	9	10	11	12	13	14
A	CDP	IOP	SCDM9	SCDP9	SVCC4	AGND1	SEREXT
B	CDM	IOM	SCDP8	SCDP10	SCDM11	AGND0	AVCC1
C	SVCC6	REQP	SCDM8	SCDM10	SCDP11	LVREXT	AVCC0
D	GND	REQM	SVCC5	PVCC	AGND2	GND	SCLKIN
E	--	--	--	--	--	--	--
F	--	--	--	--	--	--	--
G	--	--	--	--	--	--	--
H	--	--	--	--	--	--	--
J	--	GND	GND	GND	GND	--	--
K	--	GND	GND	GND	GND	--	--
L	--	GND	GND	GND	GND	--	--
M	--	GND	GND	GND	GND	--	--
N	--	--	--	--	--	--	--
P	--	--	--	--	--	--	--
R	--	--	--	--	--	--	--
T	--	--	--	--	--	--	--
U	GND	N/C	PVCC	N/C	N/C	GND	N/C
V	N/C	N/C	N/C	N/C	N/C	N/C	N/C
W	AD18	AD16	FRAME#	TRDY#	STOP#	PAR	AD15
Y	CBE2#	IRDY#	DEVSEL#	N/C	PERR#	SERR#	CBE1#

Table 5-7. I/O Ball Location Grids A15-20 through Y15-20 for AIC-7890A

	15	16	17	18	19	20
A	DIFFSENSE	EXPACT	EXTPAUSE#	CVCC4	LED#	N/C
B	CVCC5	WIDEPS#	BRDOE#	BRDWE	CVCC7	MA15
C	STPWCTL	EXTXCVR#	MVCC6	MDP	MA14	MA13
D	PVCC	CLKIN	GND	MVCC5	MA12	MA11
E	--	--	EXTARBREQ#	EXTARBACK#	MA10	MA9
F	--	--	PVCC	MVCC4	MA8	MA7
G	--	--	MD7	MD6	MA6	MVCC3
H	--	--	GND	MD5	MA5	MA4
J	--	--	MD4	MD3	MA3	MVCC2
K	--	--	MD2	MD1	MA2	MA1
L	--	--	PVCC	MD0	MVCC1	MA0
M	--	--	SEECS	ROMCS#	RAMCS#	MRW
N	--	--	GND	MVCC0	IDDAT	RAMPS#
P	--	--	N/C	N/C	TESTMODE#	CVCC3
R	--	--	PVCC	N/C	N/C	PDPUDIS#
T	--	--	N/C	N/C	AD00	AD01
U	PVCC	N/C	GND	N/C	AD02	AD03
V	N/C	N/C	N/C	N/C	AD04	AD05
W	AD13	AD11	AD09	CBE0#	AD06	AD07
Y	AD14	AD12	N/C	AD10	AD08	N/C

AIC-7891 Pinouts

Table 5-8. AIC-7891 Left Side

Pin Name	Type	BGA Pad	Description
SCDP6	I/O	B1	SCSI Data, bit-6, differential plus
SCDM6	I/O	C2	SCSI Data, bit-6, differential minus
SVCC0	P	D2	SCSI Power
SCDP5	I/O	D3	SCSI Data, bit-5, differential plus
SCDM5	I/O	E4	SCSI Data, bit-5, differential minus
GND	G	note 1	SCSI Ground
SCDP4	I/O	C1	SCSI Data, bit-4, differential plus
SCDM4	I/O	D1	SCSI Data, bit-4, differential minus
SCDP3	I/O	E3	SCSI Data, bit-3, differential plus
SCDM3	I/O	E2	SCSI Data, bit-3, differential minus
SVCC1	P	E1	SCSI Power
SCDP2	I/O	F3	SCSI Data, bit-2, differential plus
SCDM2	I/O	G4	SCSI Data, bit-2, differential minus
GND	G	note 1	SCSI Ground
SCDP1	I/O	F2	SCSI Data, bit-1, differential plus
SCDM1	I/O	F1	SCSI Data, bit-1, differential minus
CVCC0	P	G3	Core Power
SCDP0	I/O	G2	SCSI Data, bit-0, differential plus
SCDM0	I/O	G1	SCSI Data, bit-0, differential minus
SVCC2	P	H3	SCSI Power
SCDPHP	I/O	H2	SCSI Data Parity High, differential plus
SCDPHM	I/O	H1	SCSI Data Parity High, differential minus
GND	G	note 1	SCSI Ground
SCDP15	I/O	J4	SCSI Data, bit-15, differential plus
SCDM15	I/O	J3	SCSI Data, bit-15, differential minus
SCDP14	I/O	J2	SCSI Data, bit-14, differential plus
SCDM14	I/O	J1	SCSI Data, bit-14, differential minus
SVCC3	P	K2	SCSI Power
SCDP13	I/O	K3	SCSI Data, bit-13, differential plus
SCDM13	I/O	K1	SCSI Data, bit-13, differential minus
GND	G	note 1	SCSI Ground
SCDP12	I/O	L1	SCSI Data, bit-12, differential plus
SCDM12	I/O	L2	SCSI Data, bit-12, differential minus
GND	G	note 1	Core Ground
GND	G	note 1	Core Ground
PCLK	I	L3	PCI Clock
CVCC1	P	L4	Core Power

Table 5-8. AIC-7891 Left Side (Continued)

Pin Name	Type	BGA Pad	Description
ACK64#	I	M1	PCI 64-bit Acknowledge
TRST#	I	M2	JTAG Test Reset
CBE4#	I/O	M3	PCI Command/Byte Enable, bit-4
CBE6#	I/O	M4	PCI Command/Byte Enable, bit-6
GND	G	note 1	PCI Ground
TCK	I	N1	JTAG Test Clock
TMS	I	N2	JTAG Test Mode Select
AD63	I/O	N3	PCI Address/Data, bit-63
PVCC	P	note 2	PCI Power
TDO	O	P1	JTAG Test Output
GND	G	note 1	PCI Ground
TDI	I	P2	JTAG Test Input
PREQ#	O	R1	PCI Request
AD59	I/O	P3	PCI Address/Data, bit-59
IRQA#	O	R2	PCI Interrupt
GND	G	note 1	PCI Ground
AD31	I/O	T1	PCI Address/Data, bit-31
PVCC	P	note 2	PCI Power
AD61	I/O	P4	PCI Address/Data, bit-61
AD57	I/O	R3	PCI Address/Data, bit-57
PCIRST#	I	T2	PCI Reset
GND	G	note 1	PCI Ground
AD29	I/O	U1	PCI Address/Data, bit-29
AD53	I/O	T3	PCI Address/Data, bit-53
GNT#	I	U2	PCI Grant
PVCC	P	note 2	PCI Power
AD27	I/O	V1	PCI Address/Data, bit-27
GND	G	note 1	PCI Ground
AD55	I/O	T4	PCI Address/Data, bit-55
REQ64#	I/O	U3	PCI Request 64-bit
AD30	I/O	V2	PCI Address/Data, bit-30
AD25	I/O	W1	PCI Address/Data, bit-25
GND	G	note 1	PCI Ground
CBE7#	I/O	V3	PCI Command/Byte Enable, bit-7
PVCC	P	note 2	PCI Power
AD28	I/O	W2	PCI Address/Data, bit-28
CBE3#	I/O	Y1	PCI Command/Byte Enable, bit-3

Table 5-9. AIC-7891 Bottom Side

Pin Name	Type	BGA Pad	Description
AD26	I/O	W3	PCI Address/Data, bit-26
GND	G	note 1	PCI Ground
AD23	I/O	Y2	PCI Address/Data, bit-23
AD24	I/O	W4	PCI Address/Data, bit-24
CBE5#	I/O	V4	PCI Command/Byte Enable, bit-5
AD51	I/O	U5	PCI Address/Data, bit-51
PVCC	P	note 2	PCI Power
AD21	I/O	Y3	PCI Address/Data, bit-21
GND	G	note 1	PCI Ground
AD19	I/O	Y4	PCI Address/Data, bit-19
PAR64	I/O	V5	PCI Parity for AD[63:32]
IDSEL	I	W5	PCI ID Select
N/C	-	Y5	No Connect
AD62	I/O	V6	PCI Address/Data, bit-62
GND	G	note 1	PCI Ground
AD49	I/O	U7	PCI Address/Data, bit-49
PVCC	P	note 2	PCI Power
AD22	I/O	W6	PCI Address/Data, bit-22
AD17	I/O	Y6	PCI Address/Data, bit-17
AD60	I/O	V7	PCI Address/Data, bit-60
GND	G	note 1	PCI Ground
AD20	I/O	W7	PCI Address/Data, bit-20
CVCC2	P	Y7	Core Power
AD58	I/O	V8	PCI Address/Data, bit-58
AD18	I/O	W8	PCI Address/Data, bit-18
PVCC	P	note 2	PCI Power
CBE2#	I/O	Y8	PCI Command/Byte Enable, bit-2
GND	G	note 1	PCI Ground
AD47	I/O	U9	PCI Address/Data, bit-47
AD56	I/O	V9	PCI Address/Data, bit-56
AD16	I/O	W9	PCI Address/Data, bit-16
IRDY#	I/O	Y9	PCI Initiator Ready
GND	G	note 1	PCI Ground
FRAME#	I/O	W10	PCI Frame
PVCC	P	note 2	PCI Power
AD54	I/O	V10	PCI Address/Data, bit-54
DEVSEL#	I/O	Y10	PCI Device Select
N/C	-	Y11	No Connect
TRDY#	I/O	W11	PCI Target Ready
GND	G	note 1	PCI Ground
AD52	I/O	V11	PCI Address/Data, bit-52

Table 5-9. AIC-7891 Bottom Side (Continued)

Pin Name	Type	BGA Pad	Description
AD45	I/O	U11	PCI Address/Data, bit-45
PERR#	I/O	Y12	PCI Parity Error
PVCC	P	note 2	PCI Power
STOP#	I/O	W12	PCI Stop
GND	G	note 1	PCI Ground
AD50	I/O	V12	PCI Address/Data, bit-50
AD43	I/O	U12	PCI Address/Data, bit-43
SERR#	O	Y13	PCI System Error
PAR	I/O	W13	PCI Parity for AD[31:0]
GND	G	note 1	PCI Ground
AD48	I/O	V13	PCI Address/Data, bit-48
PVCC	P	note 2	PCI Power
CBE1#	I/O	Y14	PCI Command/Byte Enable, bit-1
AD15	I/O	W14	PCI Address/Data, bit-15
AD14	I/O	Y15	PCI Address/Data, bit-14
GND	G	note 1	PCI Ground
AD46	I/O	V14	PCI Address/Data, bit-46
AD13	I/O	W15	PCI Address/Data, bit-13
AD12	I/O	Y16	PCI Address/Data, bit-12
PVCC	P	note 2	PCI Power
GND	G	note 1	Core Ground
AD41	I/O	U14	PCI Address/Data, bit-41
GND	G	note 1	PCI Ground
AD44	I/O	V15	PCI Address/Data, bit-44
AD11	I/O	W16	PCI Address/Data, bit-11
N/C	-	Y17	No Connect
AD42	I/O	V16	PCI Address/Data, bit-42
AD09	I/O	W17	PCI Address/Data, bit-09
GND	G	note 1	PCI Ground
AD10	I/O	Y18	PCI Address/Data, bit-10
PVCC	P	note 2	PCI Power
AD39	I/O	U16	PCI Address/Data, bit-39
AD40	I/O	V17	PCI Address/Data, bit-40
CBE0#	I/O	W18	PCI Command/Byte Enable, bit-0
GND	G	note 1	PCI Ground
AD08	I/O	Y19	PCI Address/Data, bit-08
AD38	I/O	V18	PCI Address/Data, bit-38
AD06	I/O	W19	PCI Address/Data, bit-06
N/C	-	Y20	No Connect

Table 5-10. AIC-7891 Right Side

Pin Name	Type	BGA Pad	Description
PVCC	P	note 2	PCI Power
AD07	I/O	W20	PCI Address/Data, bit-07
GND	G	note 1	PCI Ground
AD04	I/O	V19	PCI Address/Data, bit-04
AD02	I/O	U19	PCI Address/Data, bit-02
AD36	I/O	U18	PCI Address/Data, bit-36
AD37	I/O	T17	PCI Address/Data, bit-37
GND	G	note 1	PCI Ground
AD05	I/O	V20	PCI Address/Data, bit-05
PVCC	P	note 2	PCI Power
AD03	I/O	U20	PCI Address/Data, bit-03
AD34	I/O	T18	PCI Address/Data, bit-34
AD00	I/O	T19	PCI Address/Data, bit-00
GND	G	note 1	PCI Ground
AD01	I/O	T20	PCI Address/Data, bit-01
AD35	I/O	R18	PCI Address/Data, bit-35
AD33	I/O	P17	PCI Address/Data, bit-33
PVCC	P	note 2	PCI Power
AD32	I/O	R19	PCI Address/Data, bit-32
GND	G	note 1	PCI Ground
GND	G	note 1	Memory Ground
PDPUDIS#	I	R20	Pull Down/Pull Up Disable
N/C	-	P18	-
TESTMODE#	I	P19	Test Mode
GND	G	note 1	Core Ground
CVCC3	P	P20	Core Power
MVCC0	P	N18	Memory Power
IDDAT	I	N19	ID Data
GND	G	note 1	Memory Ground
RAMPS#	I/O	N20	RAM Present
SEECS	O	M17	SEEPROM Chip Select
ROMCS#	O	M18	ROM Chip Select
RAMCS#	O	M19	RAM Chip Select
GND	G	note 1	Memory Ground
MRW	O	M20	Memory Read/Write
MVCC1	P	L19	Memory Power
MD0	I/O	L18	Memory Data, bit-0
MA0	O	L20	Memory Address, bit-0
MA1	O	K20	Memory Address, bit-1

Table 5-10. AIC-7891 Right Side (Continued)

Pin Name	Type	BGA Pad	Description
GND	G	note 1	Memory Ground
MA2	O	K19	Memory Address, bit-2
MD1	I/O	K18	Memory Data, bit-1
MD2	I/O	K17	Memory Data, bit-2
MVCC2	P	J20	Memory Power
MA3	O	J19	Memory Address, bit-3
GND	G	note 1	Memory Ground
MD3	I/O	J18	Memory Data, bit-3
MD4	I/O	J17	Memory Data, bit-4
MA4	O	H20	Memory Address, bit-4
MA5	O	H19	Memory Address, bit-5
GND	G	note 1	Memory Ground
MD5	I/O	H18	Memory Data, bit-5
MVCC3	P	G20	Memory Power
MA6	O	G19	Memory Address, bit-6
MA7	O	F20	Memory Address, bit-7
MD6	I/O	G18	Memory Data, bit-6
GND	G	note 1	Memory Ground
GND	G	note 1	Core Ground
MA8	O	F19	Memory Data, bit-3
MA9	O	E20	Memory Address, bit-9
MD7	I/O	G17	Memory Data, bit-7
MVCC4	P	F18	Memory Power
MA10	O	E19	Memory Address, bit-10
GND	G	note 1	Memory Ground
MA11	O	D20	Memory Address, bit-11
EXTARBACK#	I	E18	Acknowledge from External Arbiter
MA12	O	D19	Memory Address, bit-12
MA13	O	C20	Memory Address, bit-13
GND	G	note 1	Memory Ground
EXTARBREQ#	O	E17	Request to External Arbiter
MVCC5	P	D18	Memory Power
MA14	O	C19	Memory Address, bit-14
MA15	O	B20	Memory Address, bit-15
GND	G	note 1	Memory Ground
MDP	I/O	C18	Memory Data Parity
CVCC7	P	B19	Core Power
N/C	-	A20	No Connect

Table 5-11. AIC-7891 Top Side

Pin Name	Type	BGA Pad	Description
LED#	O	A19	LED Output
GND	G	note 1	Memory Ground
BRDWE	O	B18	Board Control Write Enable
BRDOE#	O	B17	Board Control Output Enable
MVCC6	P	C17	Memory Power
GND	G	note 1	Memory Ground
GND	G	note 1	Core Ground
CLKIN	I	D16	Clock Input
CVCC4	P	A18	Core Power
EXTPAUSE#	I	A17	External Sequencer Pause
EXTXCVR#	I	C16	External Transceiver Present
WIDEPS#	I	B16	Wide SCSI Present
EXPACT	I	A16	Expander Active
GND	G	note 1	Core Ground
STPWCTL	O	C15	SCSI Terminator Power Control
GND	G	note 1	Core Ground
GND	G	note 1	Core Ground
SCLKIN	I	D14	SCSI Clock Input
CVCC5	P	B15	Core Power
DIFFSENSE	I	A15	Differential Sense
AVCC0	P	C14	Analog Power
AVCC1	P	B14	Analog Power
SEREXT	O	A14	Analog Input 0
LVREXT	O	C13	Analog Input 1
AGND0	G	B13	Analog Ground
AGND1	G	A13	Analog Ground
AGND2	G	D12	Analog Ground
GND	G	note 1	Core Ground
SCDP11	I/O	C12	SCSI Data, bit-11, differential plus
SCDM11	I/O	B12	SCSI Data, bit-11, differential minus
SVCC4	P	A12	SCSI Power
SCDP10	I/O	B11	SCSI Data, bit-10, differential plus
SCDM10	I/O	C11	SCSI Data, bit-10, differential minus
GND	G	note 1	SCSI Ground
SCDP9	I/O	A11	SCSI Data, bit-9, differential plus
SCDM9	I/O	A10	SCSI Data, bit-9, differential minus
SCDP8	I/O	B10	SCSI Data, bit-8, differential plus
SCDM8	I/O	C10	SCSI Data, bit-8, differential minus
SVCC5	P	D10	SCSI Power

Table 5-11. AIC-7891 Top Side (Continued)

Pin Name	Type	BGA Pad	Description
IOP	I/O	A9	SCSI Input/Output, differential plus
IOM	I/O	B9	SCSI Input/Output, differential minus
GND	G	note 1	SCSI Ground
REQP	I/O	C9	SCSI Request, differential plus
REQM	I/O	D9	SCSI Request, differential minus
CDP	I/O	A8	SCSI Command/Data, differential plus
CDM	I/O	B8	SCSI Command/Data, differential minus
SVCC6	P	C8	SCSI Power
SELP	I/O	A7	SCSI Select, differential plus
SELM	I/O	B7	SCSI Select, differential minus
GND	G	note 1	SCSI Ground
MSGP	I/O	A6	SCSI Message, differential plus
MSGM	I/O	C7	SCSI Message, differential minus
GND	G	note 1	Core Ground
RESETP	I/O	B6	SCSI Reset, differential plus
RESETM	I/O	A5	SCSI Reset, differential minus
SVCC7	P	D7	SCSI Power
ACKP	I/O	C6	SCSI Acknowledge, differential plus
ACKM	I/O	B5	SCSI Acknowledge, differential minus
GND	G	note 1	SCSI Ground
BSYP	I/O	A4	SCSI Busy, differential plus
BSYM	I/O	C5	SCSI Busy, differential minus
ATNP	I/O	B4	SCSI Attention, differential plus
ATNM	I/O	A3	SCSI Attention, differential minus
SVCC8	P	D5	SCSI Power
SCDPLP	I/O	C4	SCSI Data Parity Low, differential plus
SCDPLM	I/O	B3	SCSI Data Parity Low, differential minus
GND	G	note 1	SCSI Ground
SCDP7	I/O	B2	SCSI Data, bit-7, differential plus
SCDM7	I/O	A2	SCSI Data, bit-7, differential minus
CVCC6	P	C3	Core Power

- **Note 1** - All the ground pads except analog ground pads are connected to the GND ring in the package. Die pad and GND potential ring are connected to the following BGA ball pads: A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17.
- **Note 2** - The VCC of the PCI I/O Cells are connected to the PWR ring in the package. PWR potential ring are connected to the following BGA ball pads: D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15.

Table 5-12. I/O Ball Location Grids A1-7 through Y1-7 for AIC-7891

	1	2	3	4	5	6	7
A	GND	SCDM7	ATNM	BSYP	RESETM	MSGP	SELP
B	SCDP6	SCDP7	SCDPLM	ATNP	ACKM	RESETP	SELM
C	SCDP4	SCDM6	CVCC6	SCDPLP	BSYM	ACKP	MSGM
D	SCDM4	SVCC0	SCDP5	GND	SVCC8	PVCC	SVCC7
E	SVCC1	SCDM3	SCDP3	SCDM5	--	--	--
F	SCDM1	SCDP1	SCDP2	PVCC	--	--	--
G	SCDM0	SCDP0	CVCC0	SCDM2	--	--	--
H	SCDPHM	SCDPHP	SVCC2	GND	--	--	--
J	SCDM14	SCDP14	SCDM15	SCDP15	--	--	--
K	SCDM13	SVCC3	SCDP13	PVCC	--	--	--
L	SCDP12	SCDM12	PCLK	CVCC1	--	--	--
M	ACK64#	TRST#	CBE4#	CBE6#	--	--	--
N	TCK	TMS	AD63	GND	--	--	--
P	TDO	TDI	AD59	AD61	--	--	--
R	PREQ#	IRQA#	AD57	PVCC	--	--	--
T	AD31	PCIRST#	AD53	AD55	--	--	--
U	AD29	GNT#	REQ64#	GND	AD51	PVCC	AD49
V	AD27	AD30	CBE7#	CBE5#	PAR64	AD62	AD60
W	AD25	AD28	AD26	AD24	IDSEL	AD22	AD20
Y	CBE3#	AD23	AD21	AD19	N/C	AD17	CVCC2

Table 5-13. I/O Ball Location Grids A8-14 through Y8-14 for AIC-7891

	8	9	10	11	12	13	14
A	CDP	IOP	SCDM9	SCDP9	SVCC4	AGND1	SEREXT
B	CDM	IOM	SCDP8	SCDP10	SCDM11	AGND0	AVCC1
C	SVCC6	REQP	SCDM8	SCDM10	SCDP11	LVREXT	AVCC0
D	GND	REQM	SVCC5	PVCC	AGND2	GND	SCLKIN
E	--	--	--	--	--	--	--
F	--	--	--	--	--	--	--
G	--	--	--	--	--	--	--
H	--	--	--	--	--	--	--
J	--	GND	GND	GND	GND	--	--
K	--	GND	GND	GND	GND	--	--
L	--	GND	GND	GND	GND	--	--
M	--	GND	GND	GND	GND	--	--
N	--	--	--	--	--	--	--
P	--	--	--	--	--	--	--
R	--	--	--	--	--	--	--
T	--	--	--	--	--	--	--
U	GND	AD47	PVCC	AD45	AD43	GND	AD41
V	AD58	AD56	AD54	AD52	AD50	AD48	AD46
W	AD18	AD16	FRAME#	TRDY#	STOP#	PAR	AD15
Y	CBE2#	IRDY#	DEVSEL#	N/C	PERR#	SERR#	CBE1#

Table 5-14. I/O Ball Location Grids A15-20 through Y15-20 for AIC-7891

	15	16	17	18	19	20
A	DIFFSENSE	EXPACT	EXTPAUSE#	CVCC4	LED#	N/C
B	CVCC5	WIDEPS#	BRDOE#	BRDWE	CVCC7	MA15
C	STPWCTL	EXTXCVR#	MVCC6	MDP	MA14	MA13
D	PVCC	CLKIN	GND	MVCC5	MA12	MA11
E	--	--	EXTARBREQ#	EXTARBACK#	MA10	MA9
F	--	--	PVCC	MVCC4	MA8	MA7
G	--	--	MD7	MD6	MA6	MVCC3
H	--	--	GND	MD5	MA5	MA4
J	--	--	MD4	MD3	MA3	MVCC2
K	--	--	MD2	MD1	MA2	MA1
L	--	--	PVCC	MD0	MVCC1	MA0
M	--	--	SEECS	ROMCS#	RAMCS#	MRW
N	--	--	GND	MVCC0	IDDAT	RAMPS#
P	--	--	AD33	N/C	TESTMODE#	CVCC3
R	--	--	PVCC	AD35	AD32	PDPUDIS#
T	--	--	AD37	AD34	AD00	AD01
U	PVCC	AD39	GND	AD36	AD02	AD03
V	AD44	AD42	AD40	AD38	AD04	AD05
W	AD13	AD11	AD09	CBE0#	AD06	AD07
Y	AD14	AD12	N/C	AD10	AD08	N/C

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Electrical Information

Absolute Maximum Ratings

Storage Temperature:	-65 ℃ to 150 ℃
Power Supply Voltage:	0 to 7 V
Voltage on any Pin:	-0.5 to VCC+0.5 V

Operating/Test Conditions

Ambient Temperature:	0 ℃ to 70 ℃
Supply Voltage:	5.0 V ± 5%
Supply Current:	
Active	440 mA @ 80 MB/sec SCSI Transfer (Wide)
Paused	280 mA
Power Down	100 mA (PCLK & CLKIN running, POWRDN bit =1)
	1.5 mA (PCK & CLKIN stopped, POWRDN bit =1)
t_f	< 5 ns
t_r	< 5 ns
C_L	50 pf unless otherwise noted

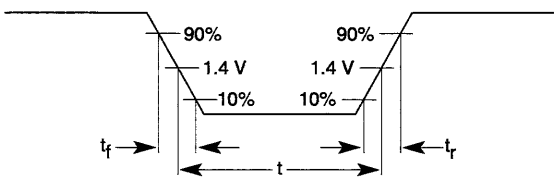
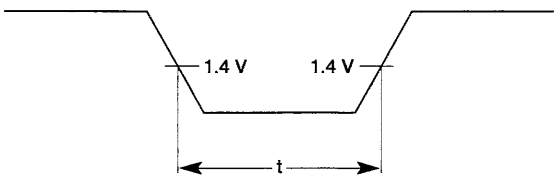


Figure 6-1. A.C. Input Conditions



C = 50 pf unless otherwise noted

Figure 6-2. A.C. Output Conditions

DC Parameters

PCI

Ta = 0 ℃ to 70 ℃
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
V_{cc}	Supply Voltage	4.75	5.25	V		
V_{ih}	Input High Voltage	2.0	Vcc+0.5	V		
V_{il}	Input Low Voltage	-0.5	0.8	V		
I_{ih}	Input High Leakage Current		70	µA	V_{in} = 2.7	1
I_{il}	Input Low Leakage Current		-70	µA	V_{in} = 0.5	1
V_{oh}	Output High Voltage	2.4		V	I_{out} = -2 MA	
V_{ol}	Output Low Voltage		0.55	V	I_{out} = 3 MA	2
V_{ol}	Output Low Voltage		0.55	V	I_{out} = 6 MA	3
C_{in}	Input Pin Capacitance		10	pf		4
C_{clk}	PCLK Pin Capacitance	5	12	pf		4
C_{IDSEL}	IDSEL Pin Capacitance		8	pf		4
L_{pin}	Pin Inductance		20	nH		

[1] Input leakage include hi-Z output leakage for bidirectional buffers with tri-state outputs.
[2] Signals without pull-up resistors (AD[63:00], CBE[7:0]#, PAR, PAR64).
[3] Signals with pull-up resistors (FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PERR#, SERR#).
[4] At 1 MHz.

Signal trace lengths on the printed circuit board where the AIC-7890A/91 is installed are 1.5 in maximum from the package pin to the PCI bus connection.

SCSI (Single Ended)

Ta = 0 ℃ to 70 ℃
VCC = 2.85 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
V_{cc}	Supply Voltage	2.71	3.00	V		
I_{il}	Input Low Leakage Current		+/-50	µA	Vin = 0.5 to VCC	1, 2
V_{ih}	Input High Voltage	2.0		V		
V_{il}	Input Low Voltage		0.8	V		
V_{ihys}	Input Hysteresis	0.2		V		
V_{oh1}	Output High Voltage	2.4		V	I_{o1} = -400 µA	3
V_{oh2}	Output High Voltage	2.4		V	I_{o2}= -2MA	
V_{ol}	Output Low Voltage		.5	V	I_{o3}= 48MA	
$V_{ih\ (Ultra)}$	Input High Voltage (Ultra)	1.6	1.9	V		4
$V_{il\ (Ultra)}$	Input Low Voltage (Ultra)	1.0	1.3	V		
V_{ihys} (Ultra)	Input Hysteresis (Ultra)	0.3	0.9	V		
$I_{oh3\ (Ultra)}$	Output High Current (Ultra)	22.0		MA	2.0 Volts	4
$I_{oh4\ (Ultra)}$	Output High Current (Ultra)		30.0	MA	3.0 Volts	
$I_{oh5\ (Ultra)}$	Output High Current (Ultra)		7.0	MA	3.24 Volts	

[1] Input leakage include hi-Z output leakage for bidirectional buffers with tri-state output (SCD[15:0]#, SCDPL#, SCDPH#, CD#, IO#, MSG#, REQ#, ACK#, RESET#, SEL#, BSY#, ATN#).
[2] Inputs are controlled to limit input current, see STPWEN.
[3] Outputs (BSY#, SEL#, RESET#).
[4] Inputs/Outputs (REQ#, ACK#, SCD[15:0]#, SCDPH#, SCDPL#)

SCSI Support Pins

Ta = 0 ℃ to 70 ℃
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
Vcc	Supply Voltage	4.75	5.25	V		
Vih	Input High Voltage	2.0	Vcc+0.5	V		
Vil	Input Low Voltage	-0.5	0.8	V		
Iil1	Input Leakage Current		10	µA	Vin = 2.7	1
Iil2	Input Leakage Current		-50	µA	Vin = 0.5	2
Iol	Output Leakage Current		+/-10	µA	Vout = 0.5 to Vcc	3
Voh1	Output High Voltage	2.4		V	Iout = -4 MA	3
Vol1	Output Low Voltage		0.5	V	Iout = 4 MA	
Voh2	Output High Voltage	2.4		V	Iout = -24 MA	4
Vol2	Output Low Voltage		0.5	V	Iout = 24 MA	4

[1] Input leakage include hi-Z output leakage for bidirectional buffer with input WIDEPS#.
[2] Input leakage includes internal pull-up resistor.
[3] Output (STPWCTL).
[4] Output (LED#).

Memory Port

Ta = 0 ℃ to 70 ℃
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
Vcc	Supply Voltage	4.75	5.25	V		
Iil1	Input Current Leakage		+/-10	µA	Vin - .4 to VCC	1
Iil2	Input Current Leakage		-50	µA	Vin - .4	2
Iol	Output Current Leakage		+/-10	µA	Vout = .5 to VCC	
Vih	Input High Voltage	2.0		V		
Vil	Input Low Voltage		.8	V		
Voh1	Output High Voltage	2.4			Io = -4mA	3
Voh2	Output High Voltage	2.4			Io = -8mA	4
Vol1	Output Low Voltage		.5	V	Io = 4mA	3
Vol2	Output Low Voltage		.5	V	Io = 8mA	4

[1] Input leakage include hi-Z output leakage for bidirectional buffers with tri-state outputs (MD[7:0], MDP).
[2] Input leakage includes internal pull-up resistor (EXTARBACK#, RAMPS#).
[3] Outputs (SEECS, RAMPS#, ROMCS#).
[4] Outputs (MD[7:0], MDP, MA[15:0], EXTARBREQ#, Outputs (RAMCS#, MRW).

Other Pins

Ta = 0 ℃ to 70 ℃
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Test Condition	Notes
Vcc	Supply Voltage	4.75	5.25	V		
I_{il1}	Input Current Leakage		+/-10	µA	V_{in} - .4 to VCC	1, 2
I_{il2}	Input Current Leakage		-50	µA	V_{in} - .4	2
V_{ih}	Input High Voltage	2.0		V		
V_{il}	Input Low Voltage		.8	V		

[1] Input leakage CLKIN.
[2] Input leakage includes internal pull-up resistor IDDAT.

Signal Test Loads

Signals	Circuit Values
SCD[15:0]#, SCDPH#, SCDPL#, RESET#, BSY#, SEL#, REQ#, MSG#, IO#, CD#, ATN#, ACK#	Capacitance (300pf) Pull-up Resistor (110 Ohm) Pull-down Resistor (165 Ohm)
FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PERR#, SEER#	Capacitance (50 pf max) Pull-up Resistor (936Ohm min) Pull-up Resistor (2.7KOhm typ) Pull-down Resistor——
AD[63:00], CBE[7:0]#, PAR, PREQ#, WIDEPS#	Capacitance (50 pf max) Pull-up Resistor—— Pull-down Resistor——
IRQA#	Capacitance (50 pf max) Pull-up Resistor (1.5KOhm min) Pull-down Resistor——
STPWCTL#, LED#, MA[15:0], MRW, MD[7:0], MDP, EXTARBREQ#, RAMPS#	Capacitance (50 pf max) Pull-up Resistor—— Pull-down Resistor——
ROMCS#, RAMCS#	Capacitance (50 pf) Pull-up Resistor (1KOhm) Pull-down Resistor——
SEECS	Capacitance (50 pf max) Pull-up Resistor—— Pull-down Resistor (1KOhm)

AC Parameters

PCI Pin V/I Curves

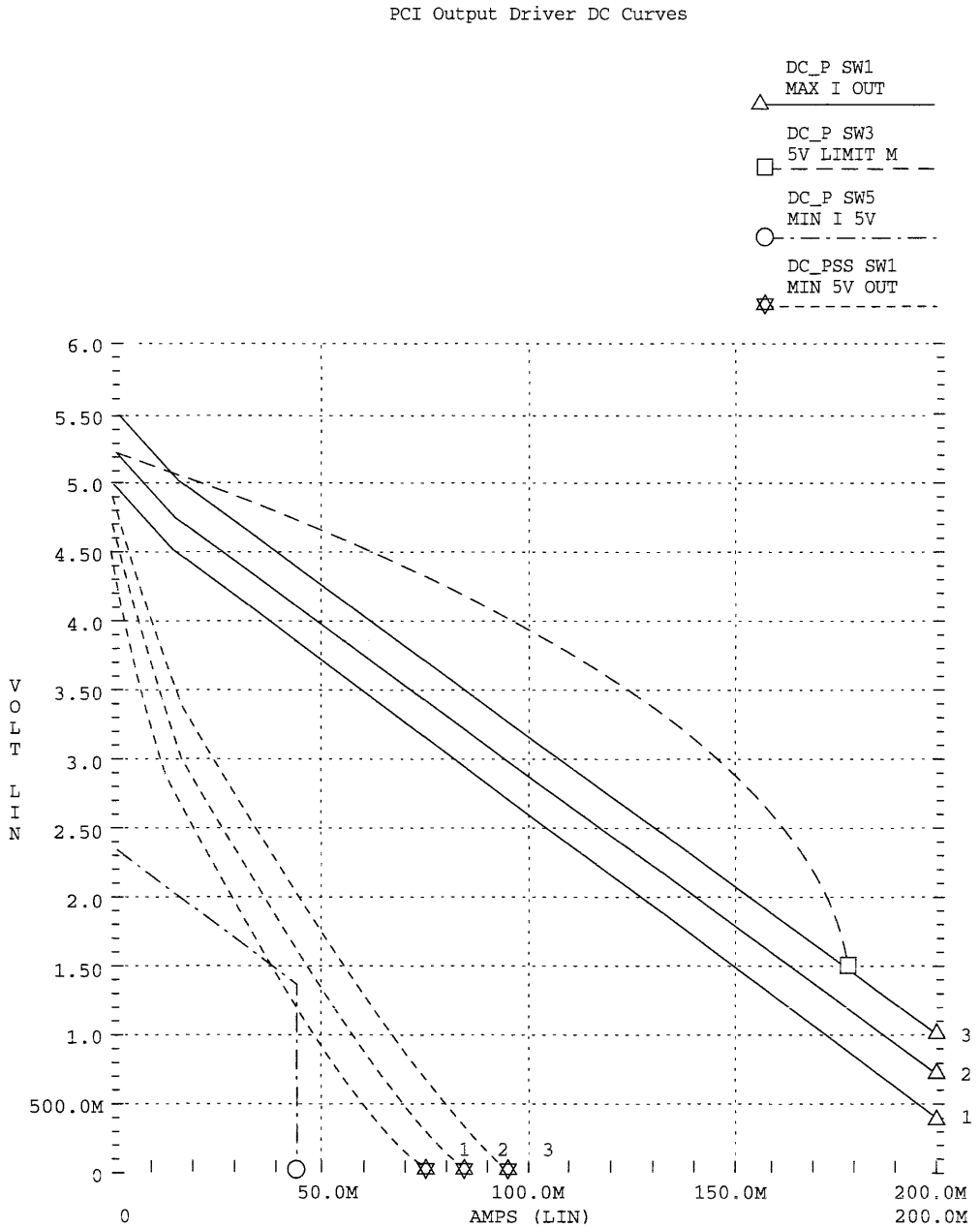


Figure 6-3. PCI Signal 5 Volt Pull-up Output V/I Curves

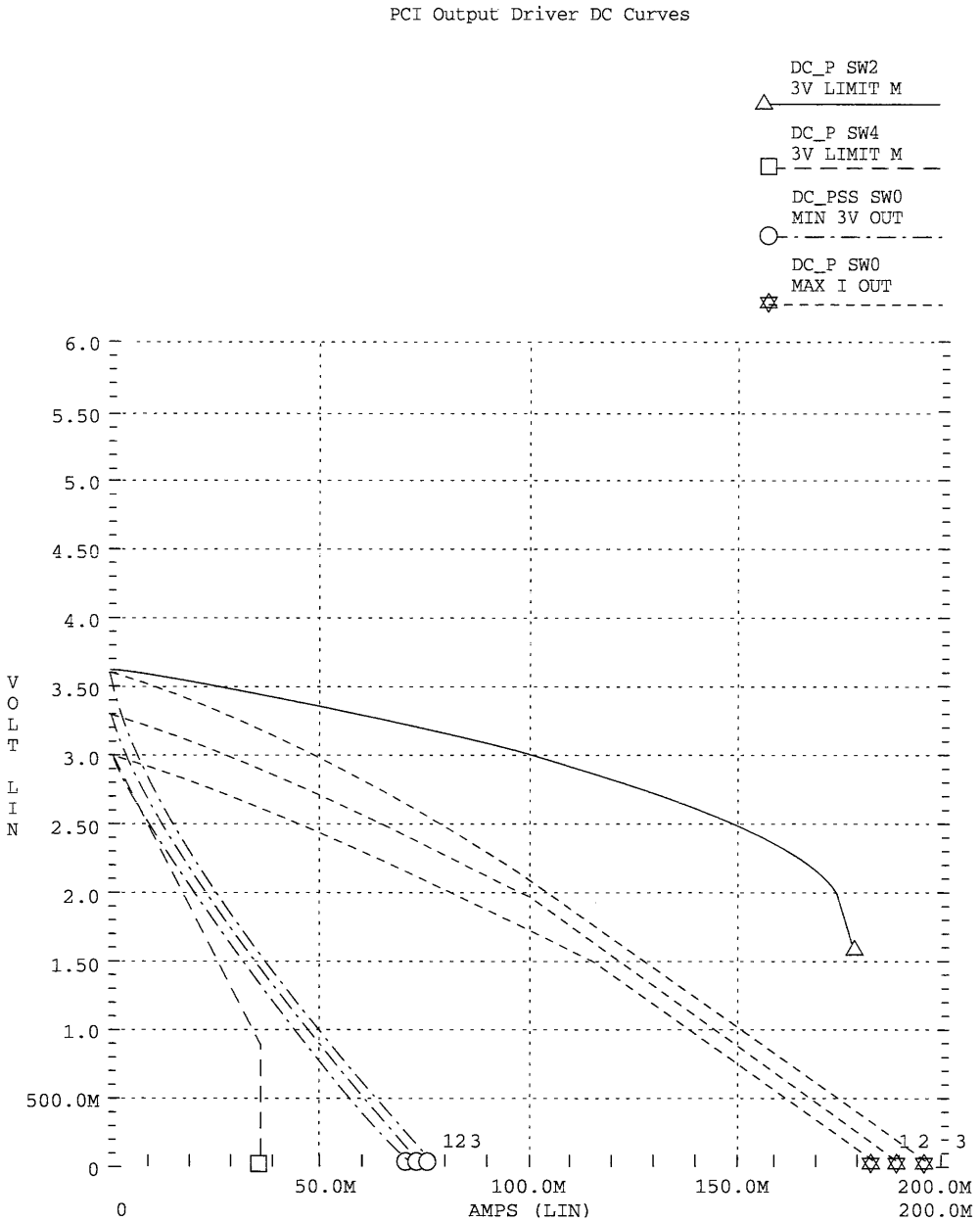


Figure 6-4. PCI Signal 3 Volt Pull-up Output V/I Curves

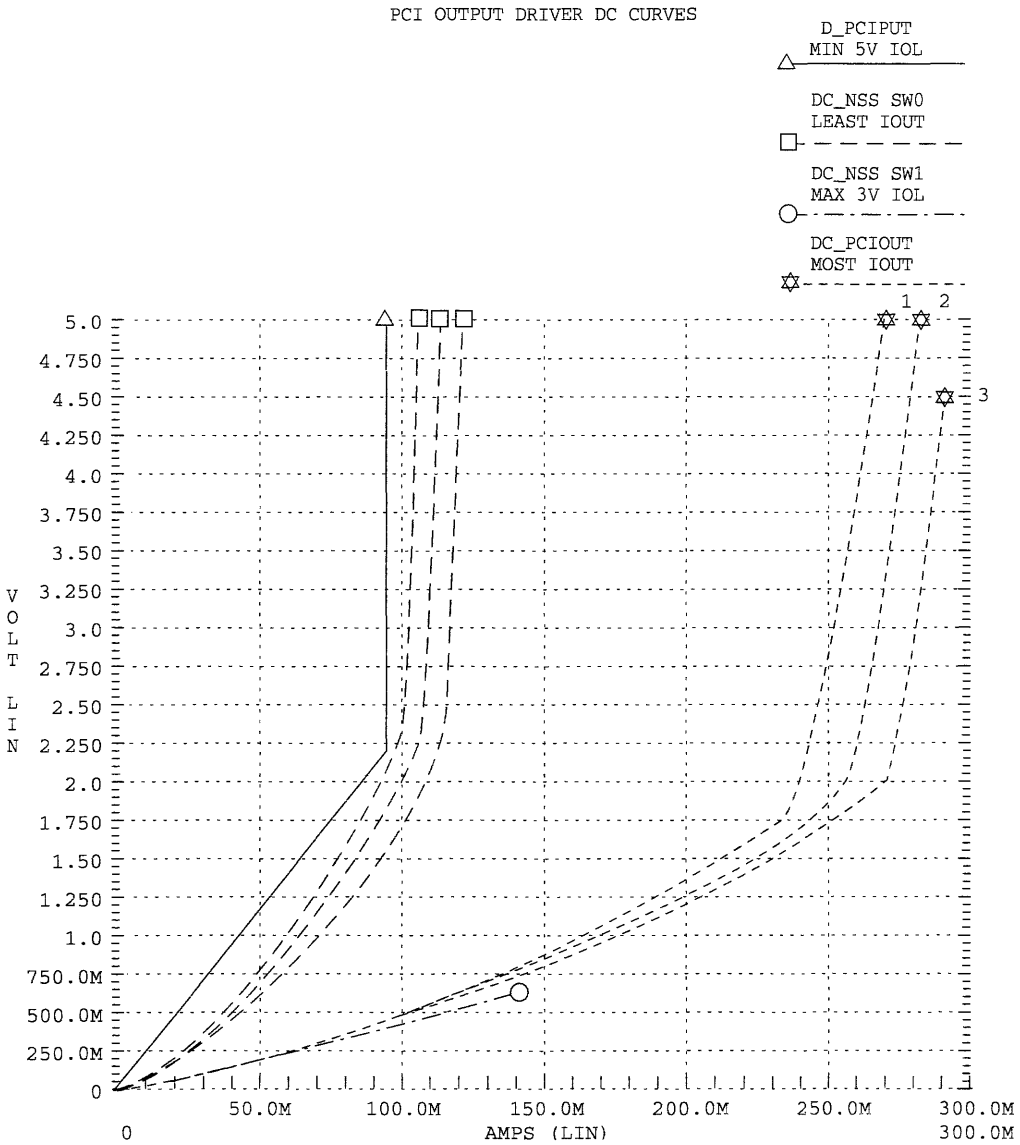


Figure 6-5. PCI Signal 3 Volt/5 Volt Pull-down Output V/I Curves

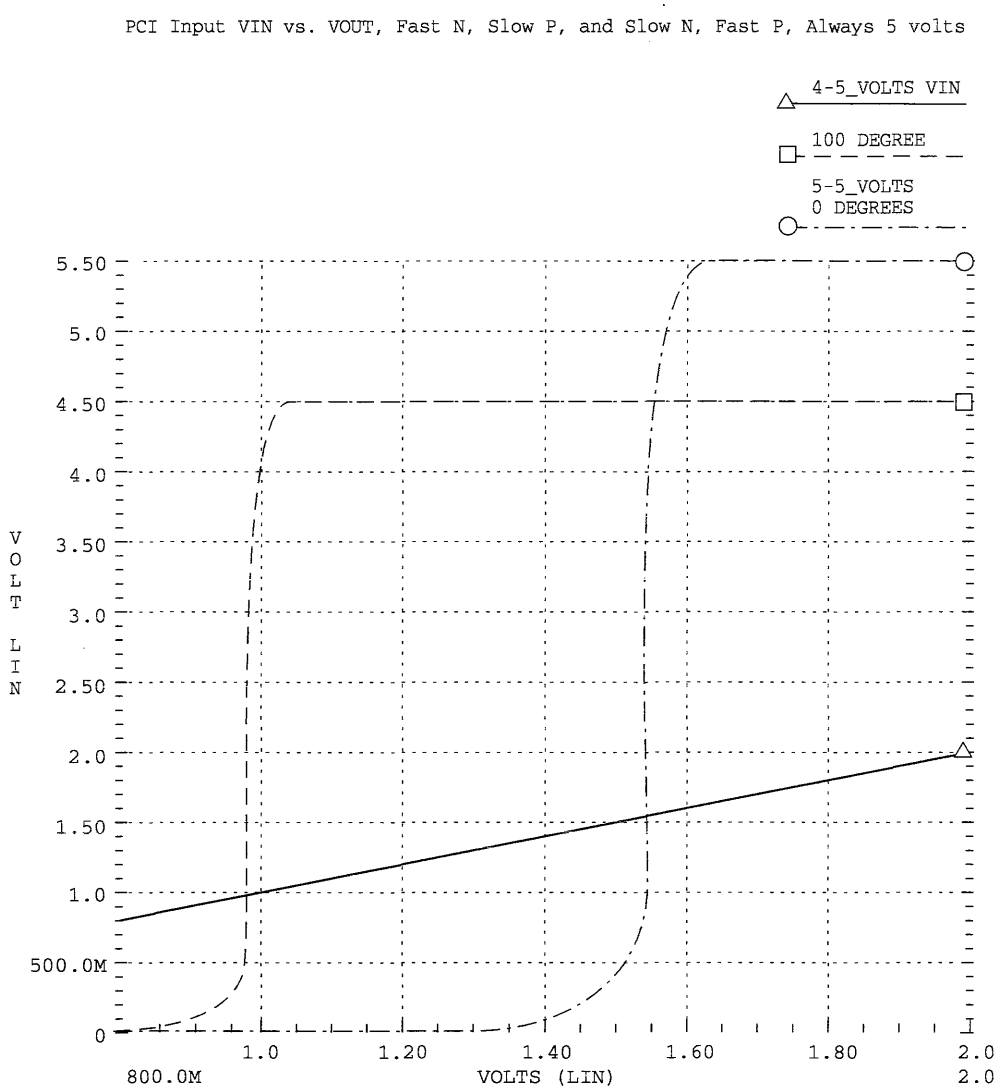


Figure 6-6. PCI Signal 5 Volt Input V/I Curves

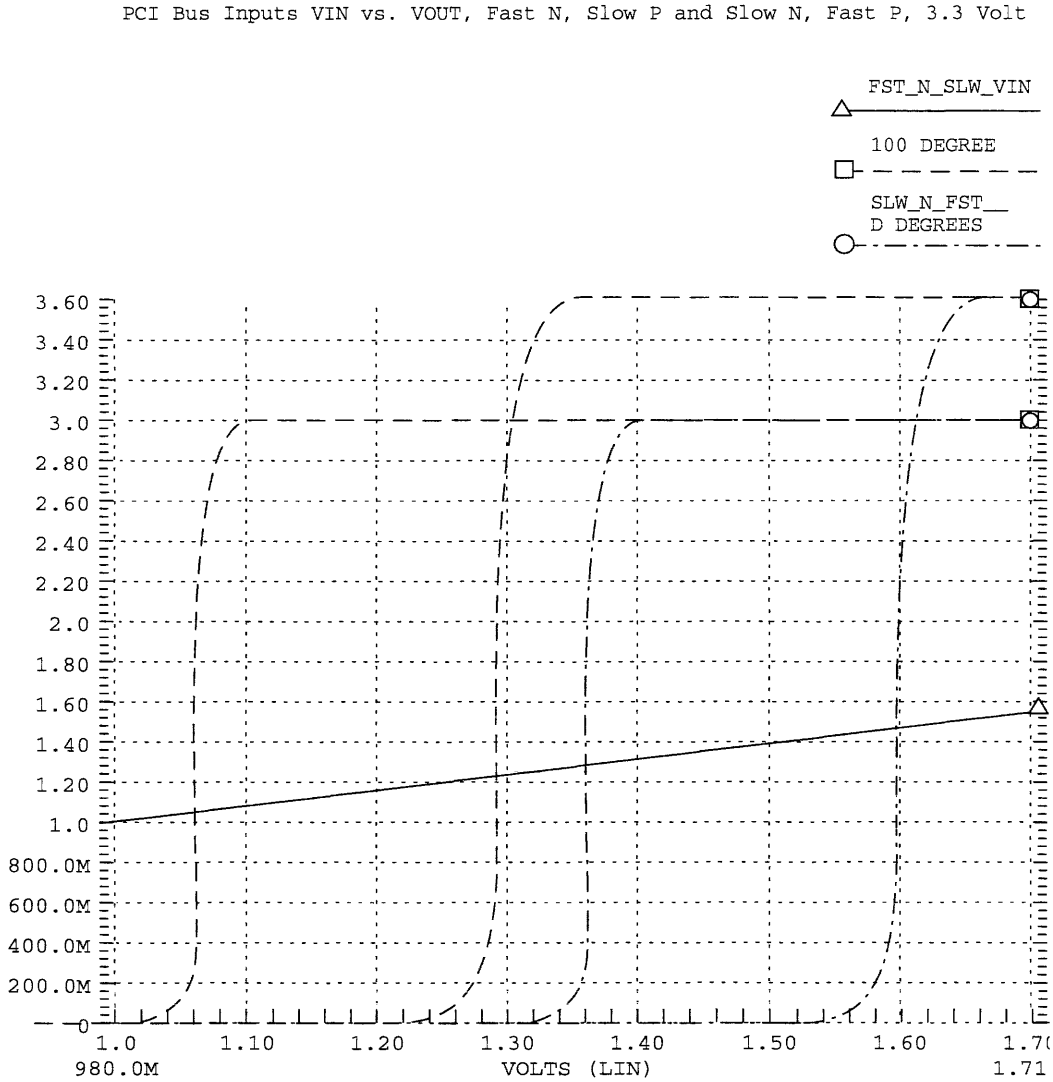


Figure 6-7. PCI Signal 3 Volt Input V/I Curves

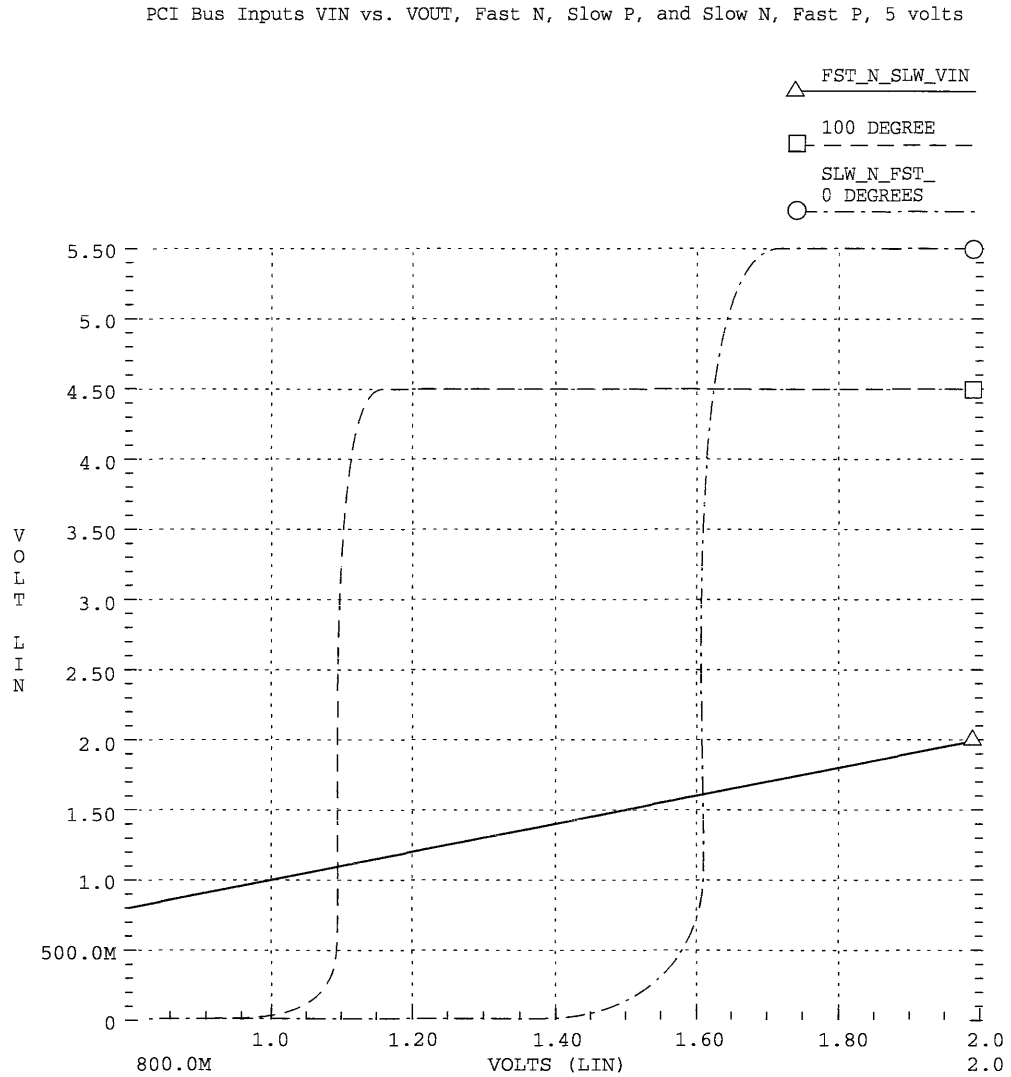


Figure 6-8. PCI Signal 3 Volt/5 Volt Input V/I Curves

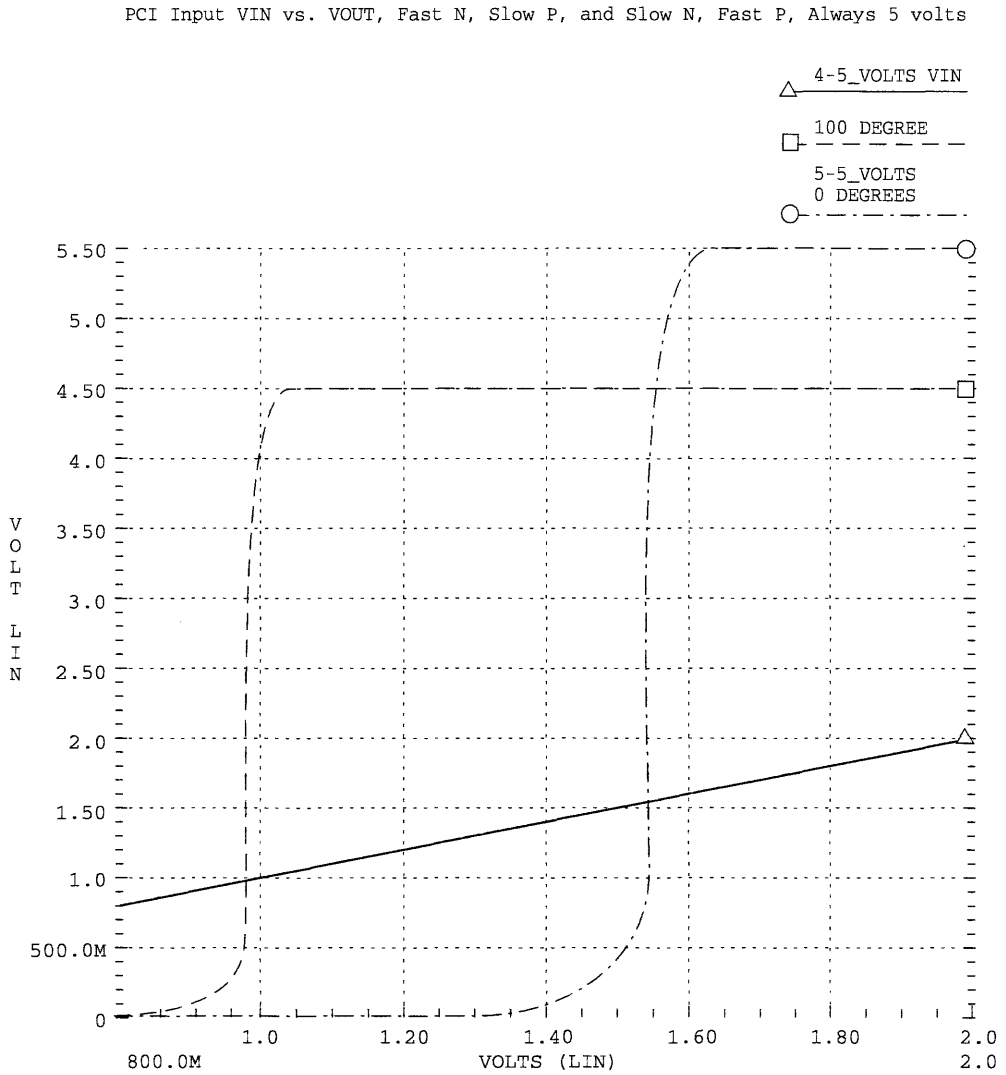


Figure 6-9. PCI Signal PCI Clock 5 Volt Input V/I Curves

Clock Timing

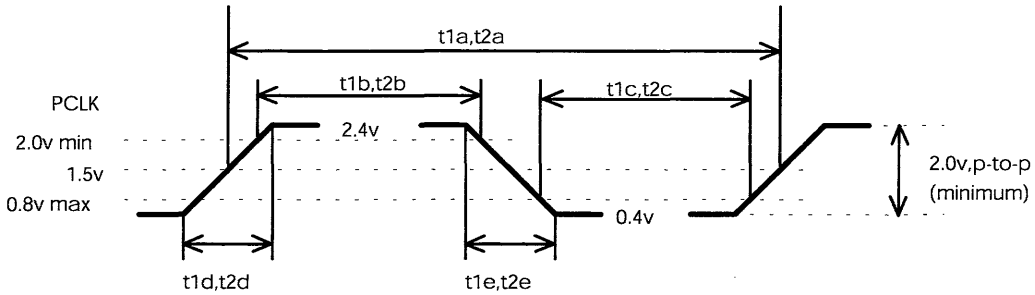


Figure 6-10. Clock Timing

Ta = 0 °to 70 °C
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Figure	Notes
t1a	PCLK Period	30		ns	6-10	1
t1b	PCLK High Time	12		ns	6-10	1
t1c	PCLK Low Time	12		ns	6-10	1
t1d	PCLK Rise Time	1	4	ns	6-10	1
t1e	PCLK Fall Time	1	4	ns	6-10	1

[1] t1a referenced to 1.5V, other times referenced to 0.8V and 2.0V.
PCLKB reference RAMPS# pin. Active from point A in Figure 9-6.

Ta = 0 °to 70 °C
VCC = 5 V ± 5%
GND = 0 V

Symbol	Definition	Min	Max	Units	Figure	Notes
t2a	CLKIN Period	25		ns	6-10	1
t2b	CLKIN High Time	7		ns	6-10	
t2c	CLKIN Low Time	8		ns	6-10	
t2d	CLKIN Rise Time		3	ns	6-10	
t2e	CLKIN Fall Time		3	ns	6-10	

[1] t2a referenced to 1.5V, other times referenced to 0.8V and 2.0V.

PCI Bus Timing

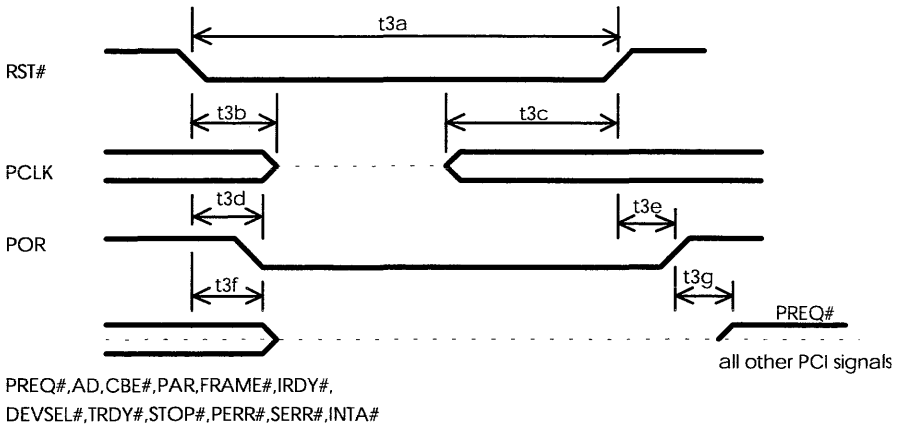
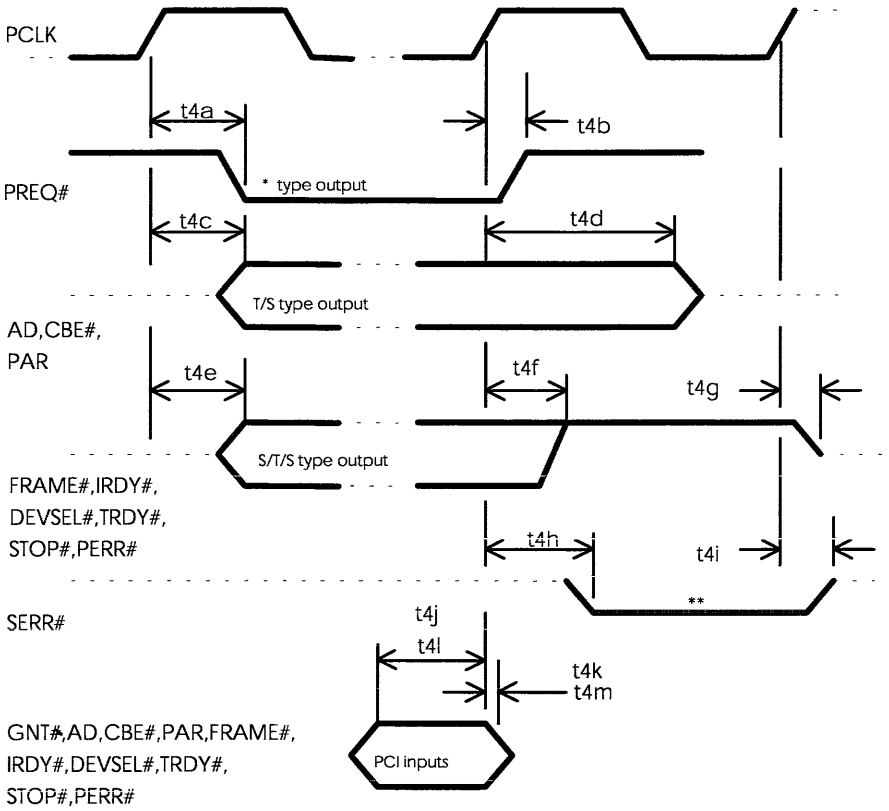


Figure 6-11. Reset Timing

Ta = 0 °to 70 °C
VCC = 5 Volts ± 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t3a	RST# Period				6-11	1
t3b	PCLK active following RST# assertion	0		ns	6-11	
t3c	PCLK active preceeding RST# deassertion				6-11	2
t3d	POR active following RST# assertion		12	ns	6-11	3
t3e	POR inactive following RST deassertion				6-11	4
t3f	PCI Outputs Float Delay	2	28	ns	6-11	
t3g	PREQ# Output Enable Delay	2	11	ns	6-11	

[1] 8 PCLK cycles minimum.
[2] 6 PCLK cycles minimum.
[3] Internal reset active (asynchronous to PCLK).
[4] Internal reset inactive (synchronous to PCLK).



* = 'T/S" type output used as "OUT" type output
(only floated when RST# is asserted).

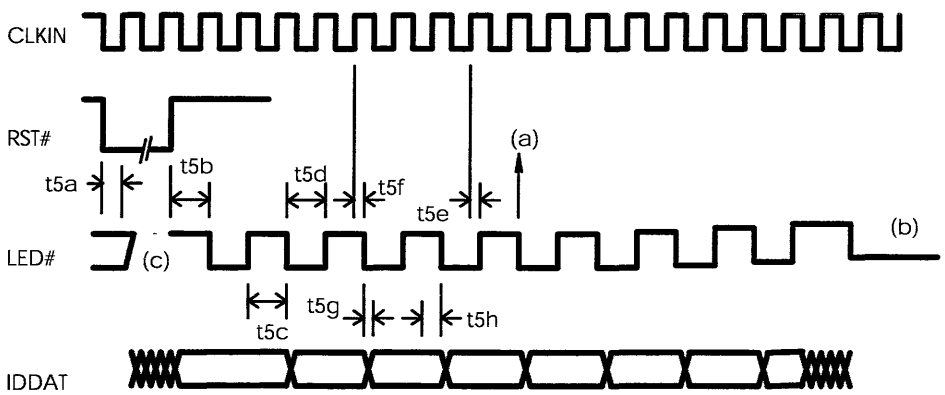
** = O/D type output

Figure 6-12. PCI Signal Input Output Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts ± 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t4a	PREQ# Assertion Delay	2	12	ns	6-12	
t4b	PREQ# Deassertion Delay	2	12	ns	6-12	
t4c	AD[31:00], CBE[3:0]#, PAR Output Valid Delay	2	11	ns	6-12	1
t4d	AD[31:00], CBE[3:0]#, PAR Output Float Delay	2	28	ns	6-12	
t4e	FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR# Output Assertion Valid Delay	2	11	ns	6-12	1
t4f	FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR# Output Deassertion Valid Delay	2	11	ns	6-12	2
t4g	FRAME#, IRDY#, DEVSEL#, TRDY#, STOP, PERR# Output Float Delay	2	28	ns	6-12	
t4h	SERR# Output Assertion Valid Delay	2	11	ns	6-12	
t4i	SERR# Output Deassertion Valid Delay	2	11	ns	6-12	
t4j	AD[31:00], CBE[3:0]#, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR# Input Valid Setup	7		ns	6-12	
t4k	AD[31:00], CBE[3:0]#, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR# Input Valid Hold	0		ns	6-12	
t4l	GNT# Input Valid Setup	10		ns	6-12	
t4m	GNT# Input Valid Hold	0		ns	6-12	

[1] Includes float to output enable delay.
[2] Starts s/t/s type output deassertion assurance period.



(a) = Note, this is the RAMPS# sample point for PCLKB output enable.

(b) = LED# is low until firmware is loaded, after which it goes high until an AIC-7890A/7891 command is busy on the SCSI bus.

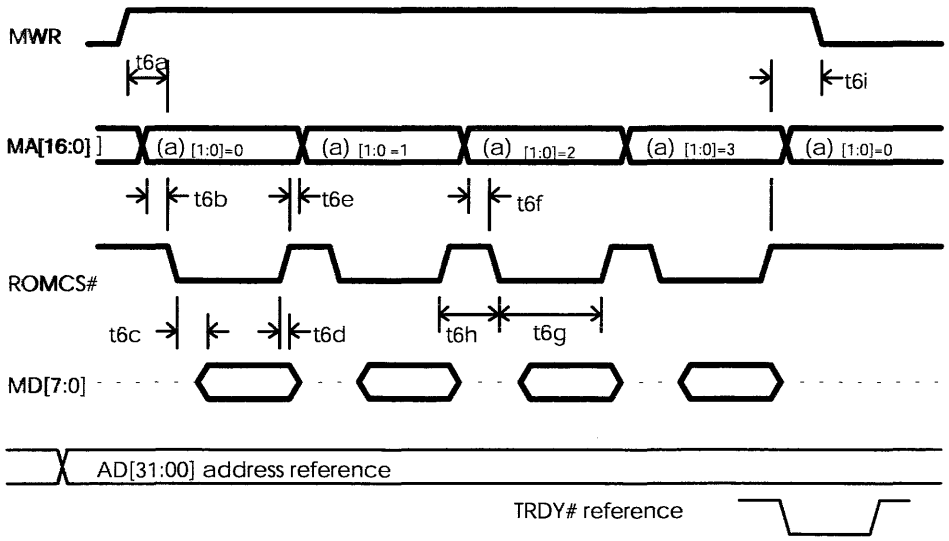
(c) = LED is in a float state.

Figure 6-13. PCI Device Identification Value Replacement Timing

Ta = 0 °to 70 °C
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t5a	RST# fall to LED# float delay		7	ns	6-13	
t5b	RST# rise to LED# first clock fall	1	3	CLKIN period	6-13	
t5c	LED# (IDDAT) clock low time	25		ns	6-13	
t5d	LED# (IDDAT) clock high time	25		ns	6-13	
t5e	CLKIN rise to LED# rise	9		ns	6-13	
t5f	CLKIN rise to LED# fall	8		ns	6-13	
t5g	IDDAT data hold from LED# rise	0		ns	6-13	
t5h	IDDAT data valid to LED# rise	5		ns	6-13	

Memory Port Timing



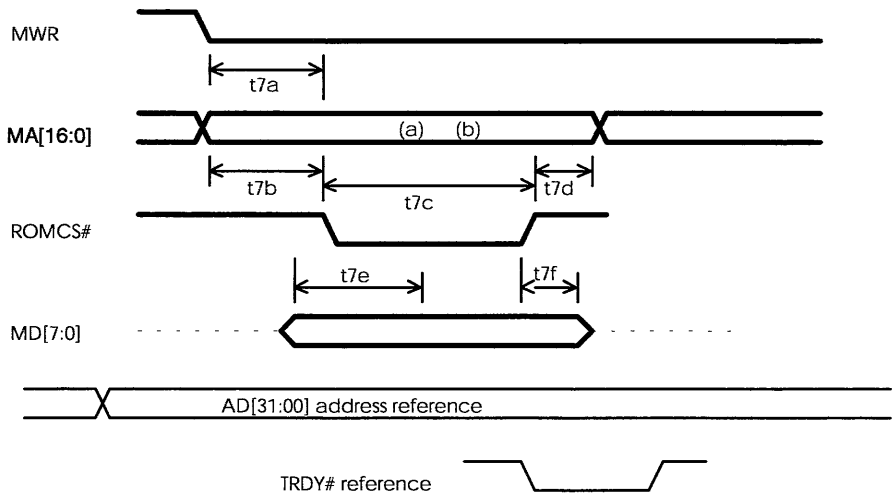
[a] = MA[16:2] = AD[16:2] address reference

Note: MA16 is provided by use of MDP during ROM read and EEPROM write cycles.

Figure 6-14. PCI ROM/EEPROM Read Memory Port Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t6a	MWR setup to ROMCS# fall	15		ns	6-14	
t6b	MA[16:0] setup to ROMCS# fall (byte 1)	60		ns	6-14	
t6c	MD[7:0] valid from ROMCS# fall		150	ns	6-14	
t6d	MD[7:0] hold from ROMCS# rise	0		ns	6-14	
t6e	MA[16:0] hold from ROMCS# rise	0		ns	6-14	
t6f	MA[16:0] setup to ROMCS# fall (bytes 2-4)	16		ns	6-14	
t6g	ROMCS# low time	150		ns	6-14	
t6h	ROMCS# high time (between bytes)	20		ns	6-14	
t6i	MWR hold from ROMCS# rise	25		ns	6-14	



[a] = MA[16:2] = AD[16:2] address reference

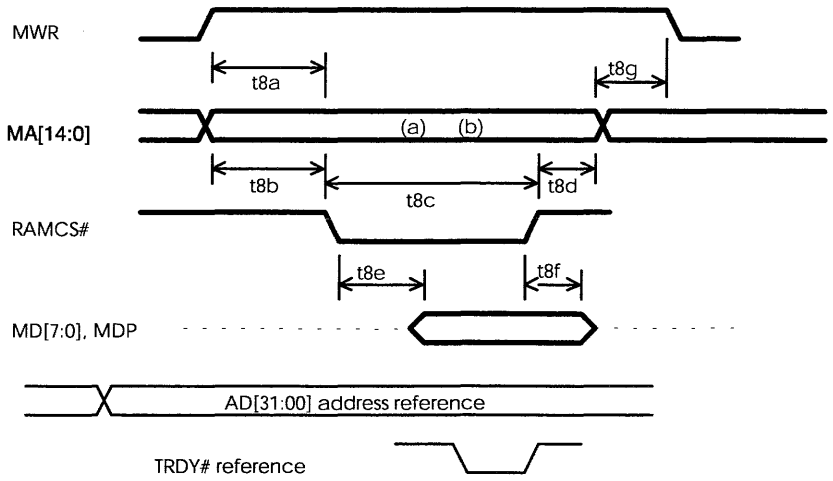
(b) = MA[1:0] = CBE[3:0] byte reference

Note: MA16 is provided by use of MDP during ROM read and EEPROM write cycles.

Figure 6-15. PCI EEPROM Write Memory Port Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t7a	MWR setup to ROMCS# fall	15		ns	6-15	
t7b	MA[16:0] setup to ROMCS# fall	60		ns	6-15	
t7c	ROMCS# low time	150		ns	6-15	
t7d	MA[16:0] hold time from ROMCS# rise	55		ns	6-15	
t7e	MD[7:0] setup time to ROMCS# fall	15		ns	6-15	
t7f	MD[7:0] hold time from ROMCS# rise	25		ns	6-15	
t7g	MWR hold time from ROMCS# rise	25		ns	6-15	



[a] = MA[14:2] = AD[14:2] address reference

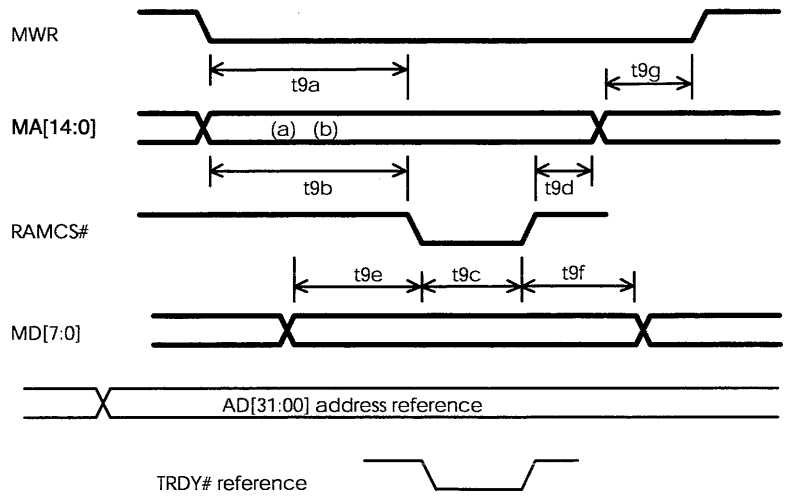
(b) = MA[1:0] = CBE[3:0] byte reference

Note: MA15 is not used.

Figure 6-16. PCI SRAM Read Memory Port Timing

Ta = 0 °to 70 °C
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t8a	MWR setup to RAMCS# fall	30		ns	6-16	
t8b	MA[14:0] setup to RAMCS# fall	20		ns	6-16	
t8c	RAMCS# low time	60		ns	6-16	
t8d	MA[14:0] hold from RAMCS# rise	30		ns	6-16	
t8e	MD[7:0], MDP valid to RAMCS# fall	20		ns	6-16	
t8f	MD[7:0], MDP hold from RAMCS# rise	0		ns	6-16	
t8g	MWR hold from RAMCS# rise	30		ns	6-16	



[a] = MA[14:2] = AD[14:2] address reference

(b) = MA[1:0] = CBE[3:0] byte reference

Figure 6-17. PCI SRAM Write Memory Port Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t9a	MWR setup to RAMCS# fall	10		ns	6-17	
t9b	MA[14:0] setup to RAMCS# fall	8		ns	6-17	
t9c	RAMCS# low time	25		ns	6-17	
t9d	MA[12:0] hold from RAMCS# rise	12		ns	6-17	
t9e	MD[7:0], MDP setup to RAMCS# fall	10		ns	6-17	
t9f	MD[7:0], MDP hold from RAMCS# rise	10		ns	6-17	
t9g	MWR hold from RAMCS# rise	0		ns	6-17	

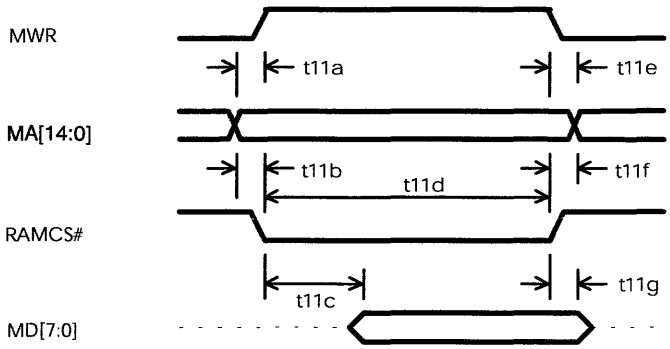


Figure 6-18. Sequencer Read Memory Port Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t11a	MWR setup to RAMCS# fall	0		ns	6-18	
t11b	MA[14:0] setup to RAMCS# fall	0		ns	6-18	
t11c	MD[7:0], MDP valid from RAMCS# fall	20		ns	6-18	
t11d	RAMCS# low time	25		ns	6-18	
t11e	MWR hold from RAMCS# rise	0		ns	6-18	
t11f	MA[14:0] hold from RAMCS# rise	0		ns	6-18	
t11g	MD[7:0], MDP hold from RAMCS# rise	0		ns	6-18	

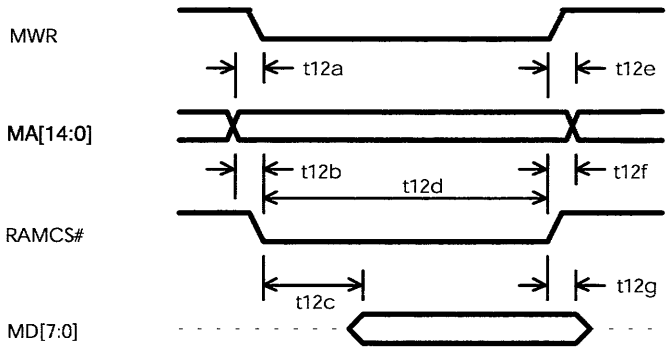


Figure 6-19. Sequencer Write Memory Port Timing

Ta = 0 °to 70 ℃
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t12a	MWR setup to RAMCS# fall	0		ns	6-19	
t12b	MA[14:0] setup to RAMCS# fall	0		ns	6-19	
t12c	MD[7:0], MDP valid from RAMCS# fall	20		ns	6-19	
t12d	RAMCS# low time	25		ns	6-19	
t12e	MWR hold from RAMCS# rise	0		ns	6-19	
t12f	MA[14:0] hold from RAMCS# rise	0		ns	6-19	
t12g	MD[7:0], MDP hold from RAMCS# rise	0		ns	6-19	

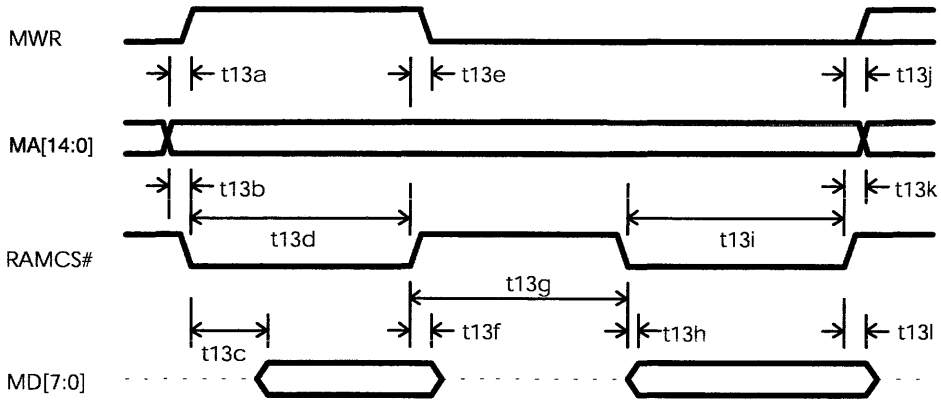


Figure 6-20. Sequencer Read-Modify-Write Memory Port Timing

Ta = 0 °to 70 °C
VCC = 5 Volts +/- 5%
GND = 0 Volts

Symbol	Definition	Min	Max	Units	Figure	Notes
t13a	MWR setup to RAMCS# fall	0		ns	6-20	
t13b	MA[14:0] setup to RAMCS# fall	0		ns	6-20	
t13c	MD[7:0], MDP valid from RAMCS# fall	20		ns	6-20	
t13d	RAMCS# low time	25		ns	6-20	
t13e	MWR hold from RAMCS# rise	0		ns	6-20	
t13f	MD[7:0], MDP hold from RAMCS# rise	0	10	ns	6-20	
t13g	RAMCS# rise (read) to RAMCS# fall (write)	25		ns	6-20	
t13h	MD[7:0], MDP valid from RAMCS# fall	0	5	ns	6-20	
t13i	RAMCS# low time	25		ns	6-20	
t13j	MWR hold from RAMCS# rise	0		ns	6-20	
t13k	MA[14:0] hold from RAMCS# rise	0		ns	6-20	
t13l	MD[7:0], MDP hold from RAMCS# rise	0		ns	6-20	

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System Cycles

PCI Master Bus Cycles

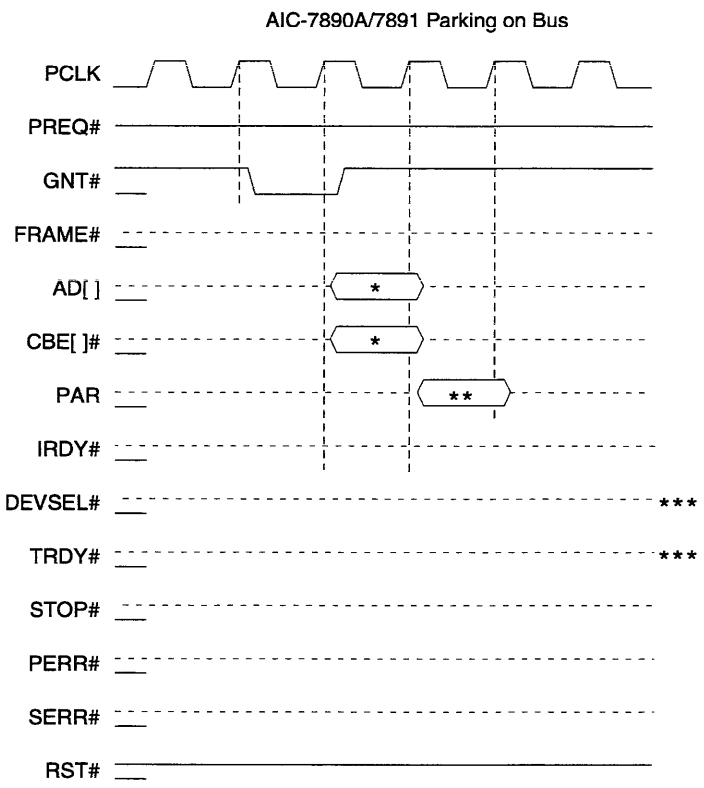


Figure 7-1. Master Parking on Bus

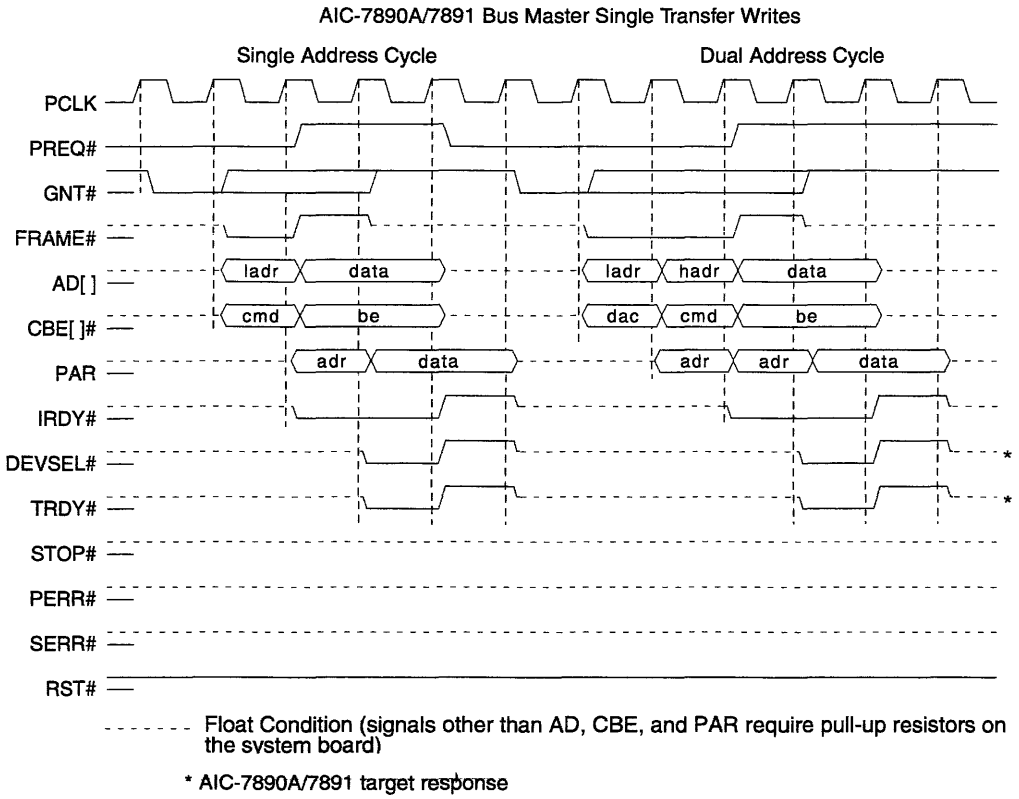


Figure 7-2. Master Single Transfer Write

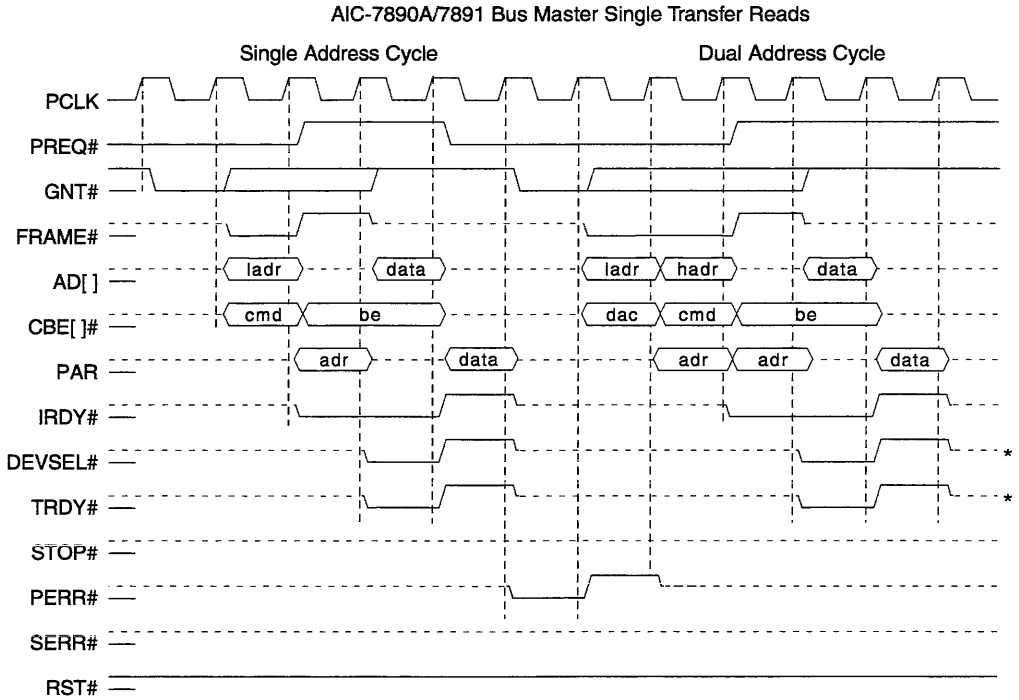
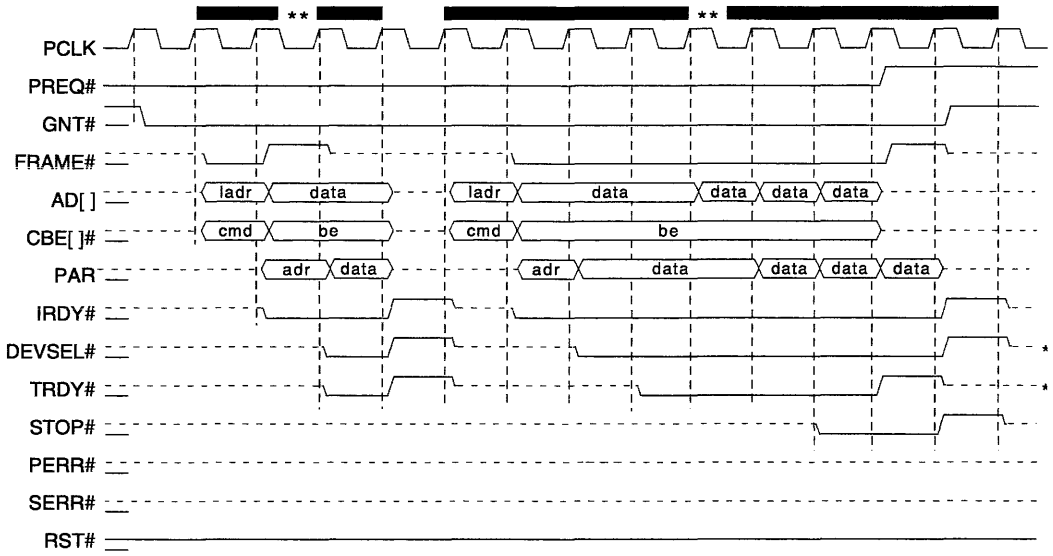


Figure 7-3. Master Single Transfer Read

AIC-7890A/7891 Parking on Bus



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

* AIC-7890A/7891 target response

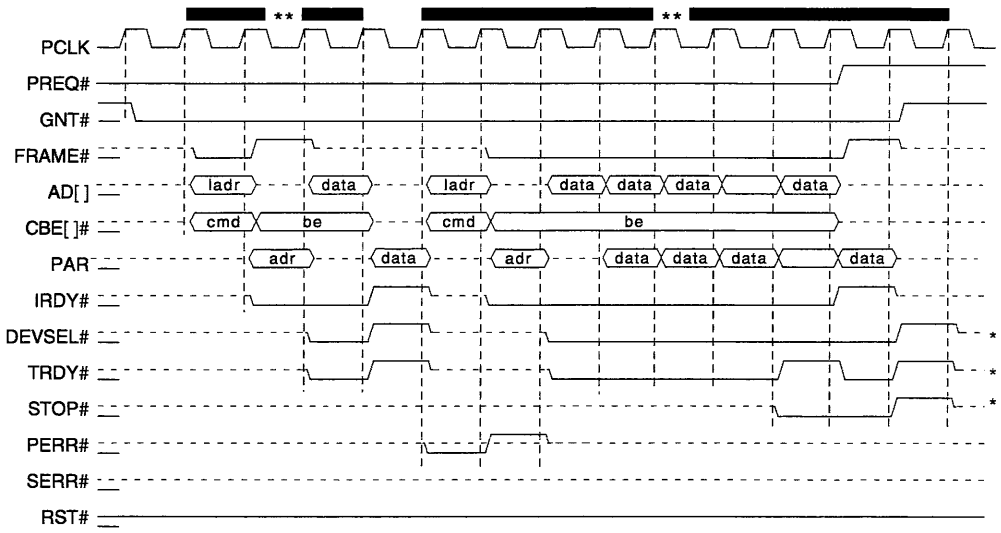
** AIC-7890A/7891 MRDC burst to cache line boundary

*** AIC-7890A/7891 MRDC burst for 16-byte cache line

The AIC-7890A/7891 is capable of cache line streaming, with no wait states. However, the target disconnects at end of cache line.

Figure 7-4. Master Burst Transfer Write

AIC-7890A/7891 Bus Master Burst Read



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

* AIC-7890A/7891 target response

** AIC-7890A/7891 MRDC burst to cache line boundary

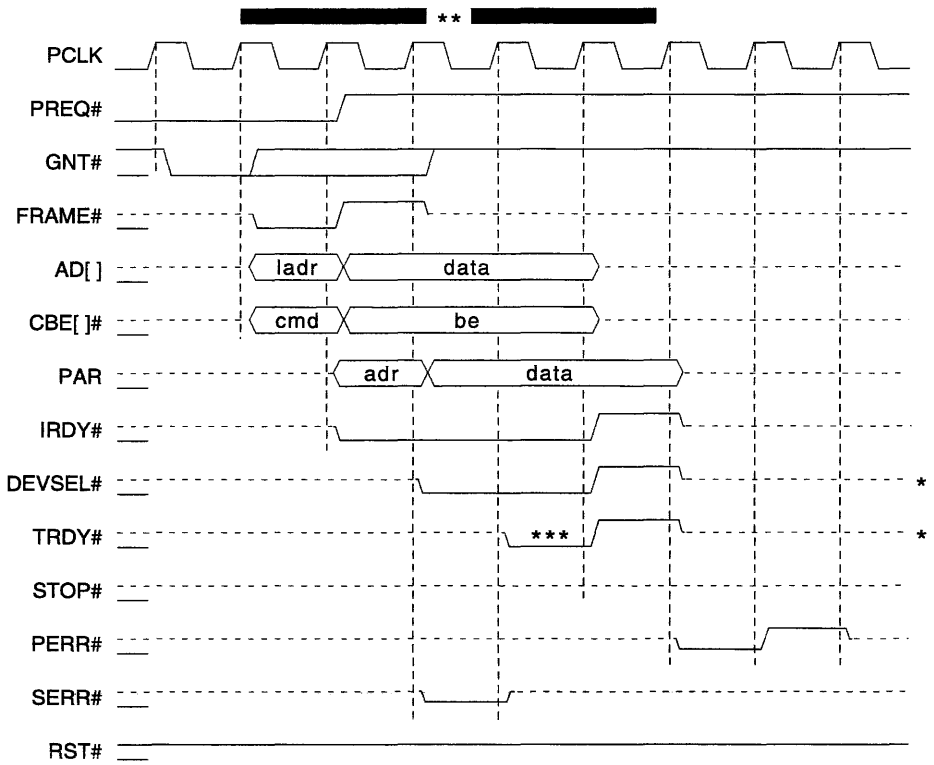
*** AIC-7890A/7891 MRDC burst for 16-byte cache line

The AIC-7890A/7891 is capable of cache line streaming, with no wait states. However, the target disconnects at end of cache line.

Figure 7-5. Master Burst Transfer Read

PCI Slave Bus Cycles

AIC-7890A/7891 Bus Slave Write Cycle



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

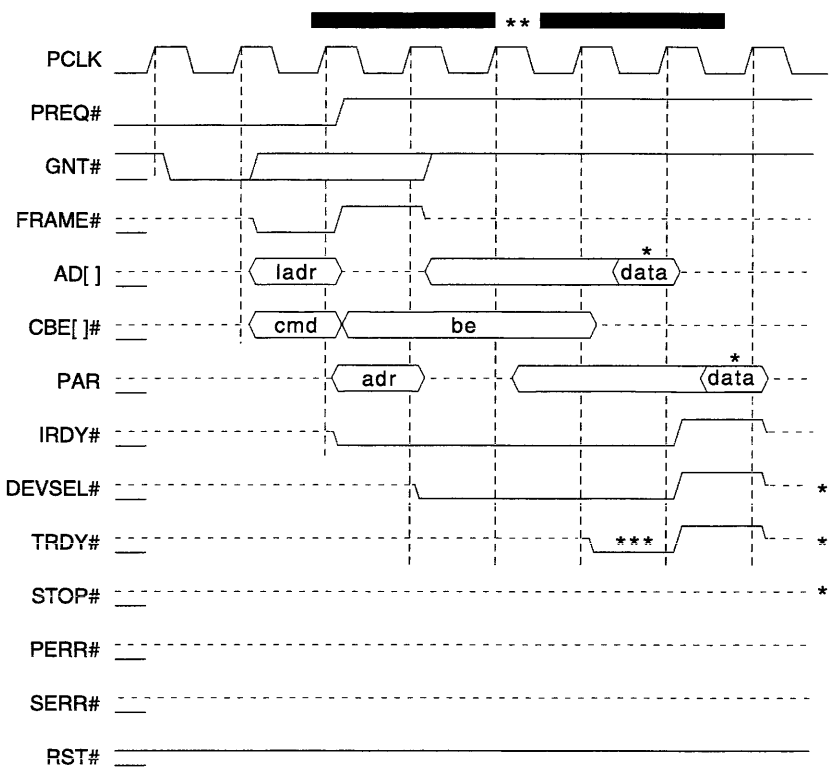
* AIC-7890A/7891 target response

** AIC-7890A/7891 register access cycle

*** May be delayed one of more clocks for some addresses.

Figure 7-6. Slave Single Transfer Write

AIC-7890A/7891 Bus Slave Read Cycle



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

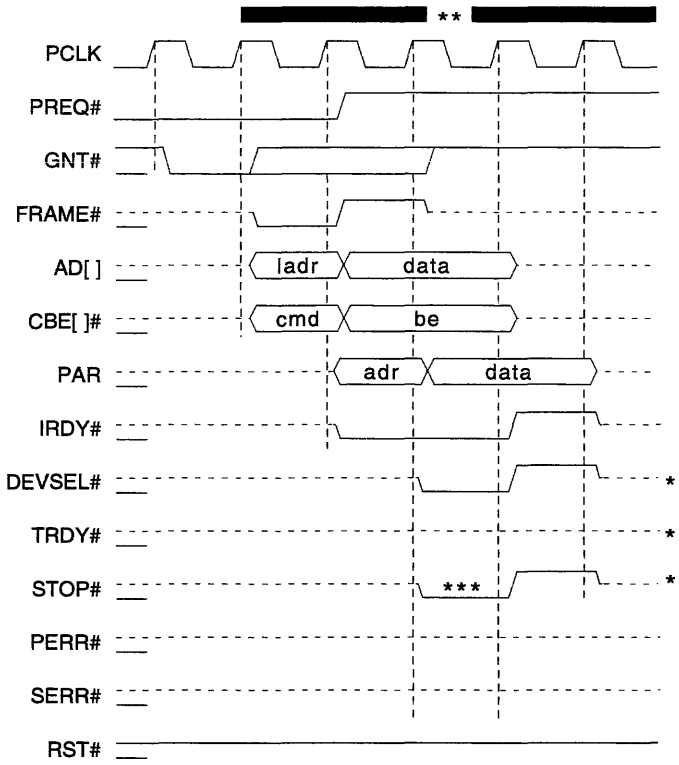
* AIC-7890A/7891 target response

** AIC-7890A/7891 register access cycle

*** May be delayed one of more clocks for some addresses.

Figure 7-7. Slave Single Transfer Read

AIC-7890A/7891 Bus Slave Retry Cycle



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

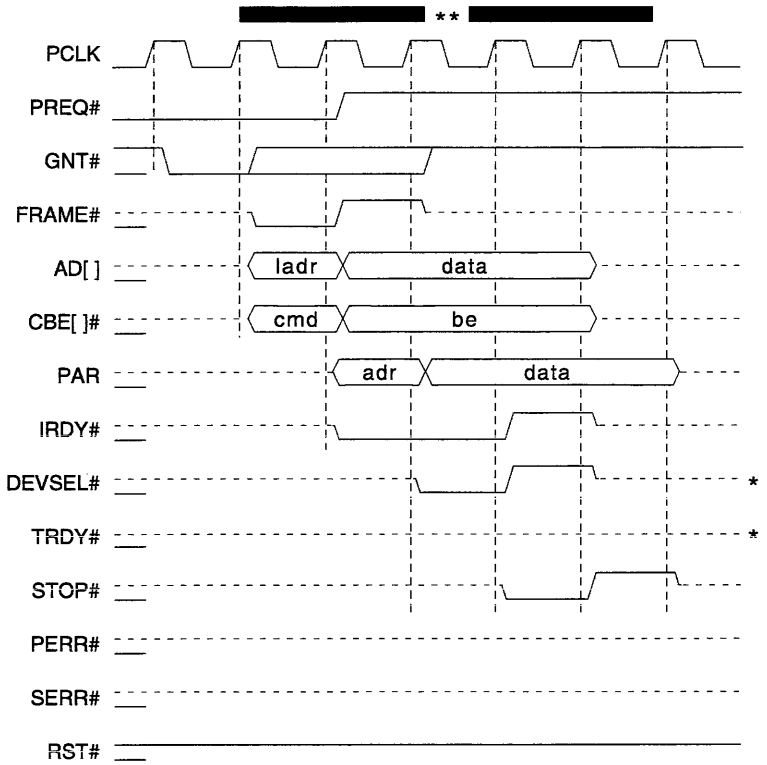
* AIC-7890A7891 target response

** AIC-7890A/7891 register access cycle

*** May be delayed one of more clocks for some addresses.

Figure 7-8. Slave Retry

AIC-7890A/7891 Bus Slave Target Abort Cycle



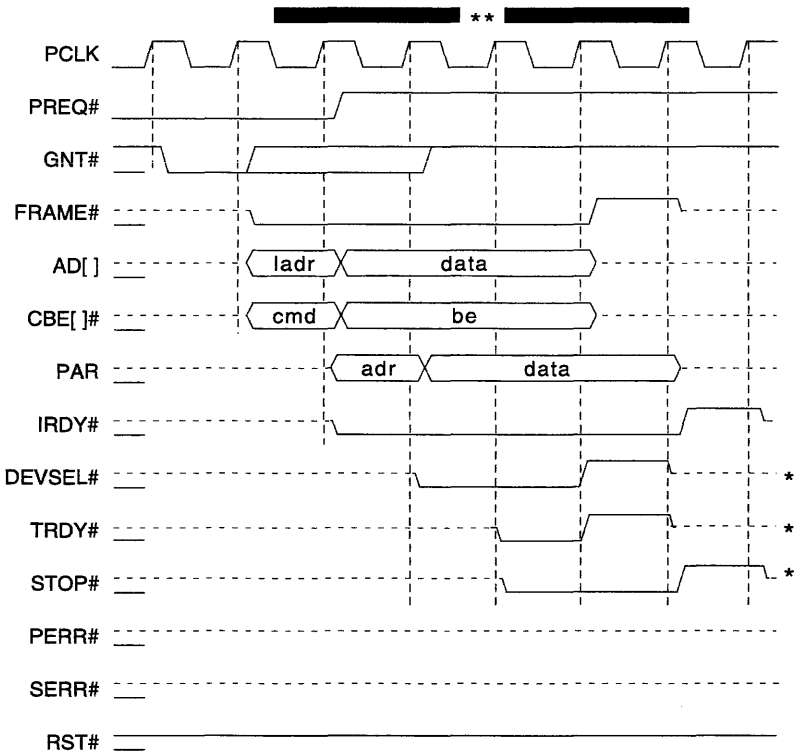
--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

* AIC-7890A/7891 target response

** AIC-7890A/7891 register access cycle with data wide error

Figure 7-9. Slave Target Abort (width error)

AIC-7890A/7891 Bus Slave Burst Disconnect Cycle



--------Float Condition (signals other than AD, CBE, and PAR require pull-up resistors on the system board.)

* AIC-7890A/7891 target response

** AIC-7890A/7891 register access cycle with unsupported burst attempt

Figure 7-10. Slave Burst Disconnect

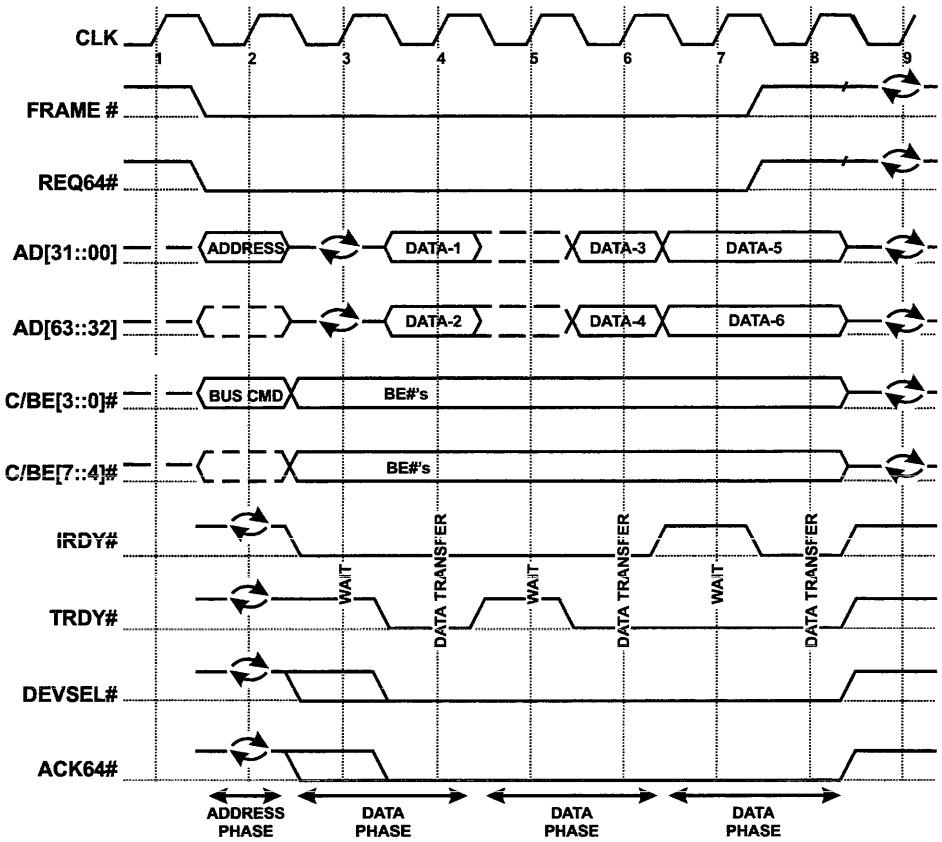


Figure 7-11. 64-Bit Read Request with 64-Bit Transfer (AIC-7891 only)

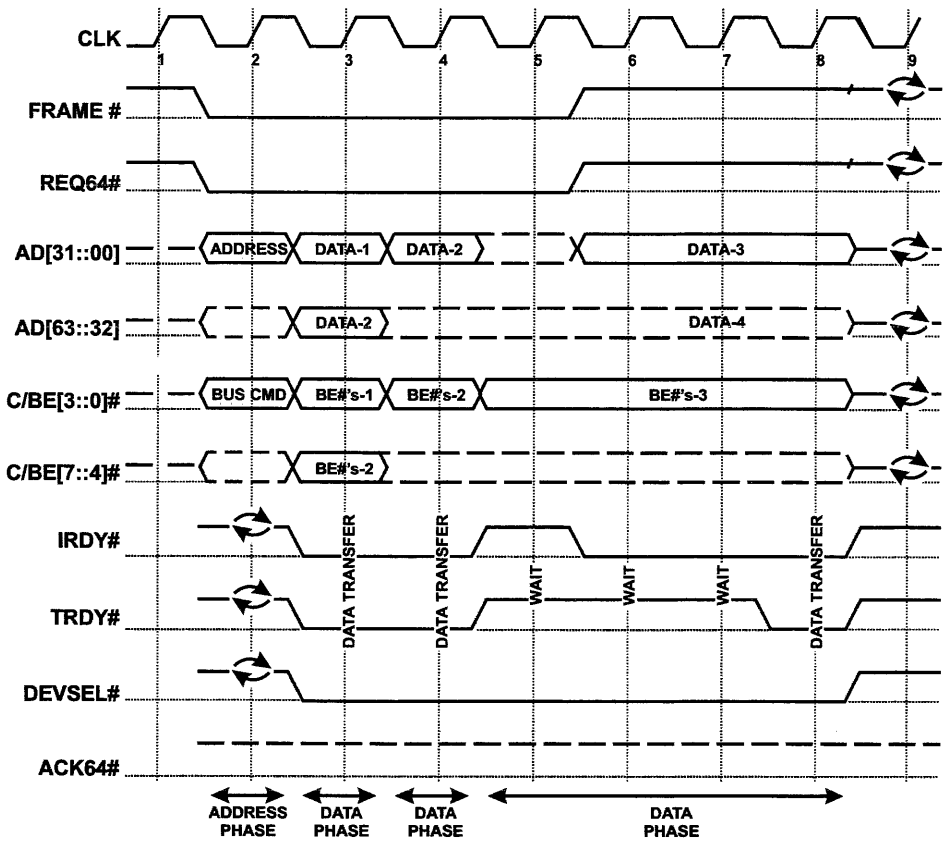


Figure 7-12. 64-Bit Write Request with 32-Bit Transfer (AIC-7891 only)

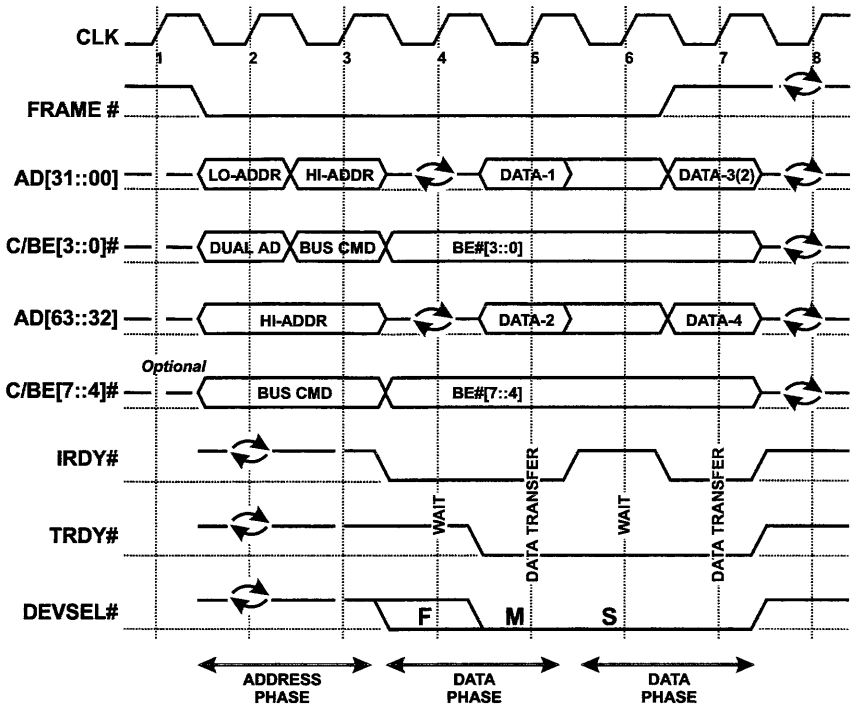


Figure 7-13. 64-Bit Dual Address Read Cycle (AIC-7891 only)

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