Ordering number: EN 3591A

NMOS LS

No.3591A

LM7001, LM7001M

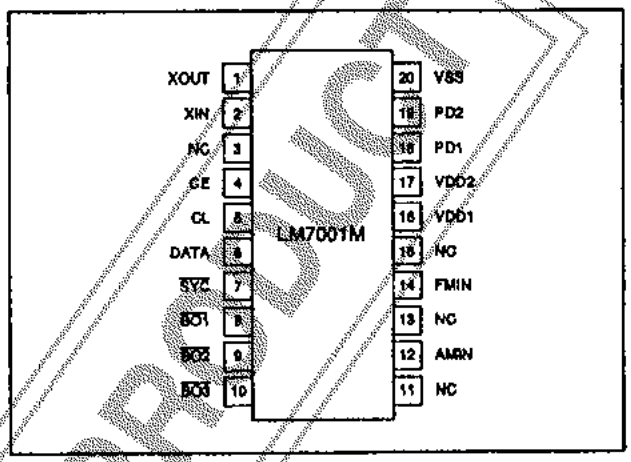
Direct PLL Frequency Synthesizers

OVERVIEW

The LM7001 and LM7001M are direct PLL frequency synthesizers that provide accurate reference frequencies for long-wave and medium-wave AM and FM tuners. They incorporate a 24-bit shift register and latch, programmable divider, reference divider and phase detector charge pump.

The LM7001 and LM7001M feature an AM frequency range of 500 kHz to 10 MHz and FM ranges of 5 to 30 MHz and 45 to 130 MHz. Seven software-selectable reference frequencies are available in the range 1 to 100 kHz. A 400 kHz microcontroller clock output and an 8 Hz real-time clock output are also provided.

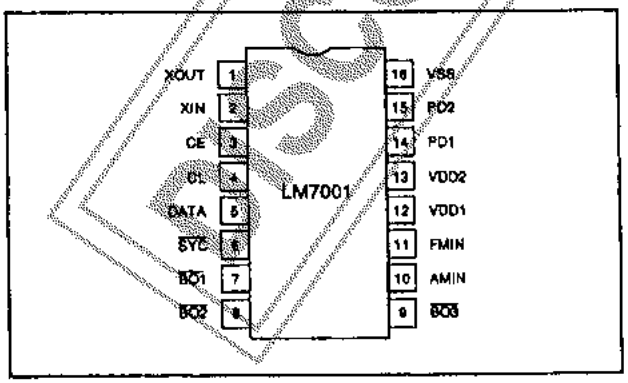
The LM7001 and LM7001M operate from a 5 V supply and are available in 16-pin DIPs and 20-pin MFPs, respectively.



FEATURES

- High-speed AM/FM programmable divider
- Seven software-selectable reference frequencies in the range 1 to 100 kHz
- Three on-chip, open-drain bandswitching output drivers
- 400 kHz clock output for microcontroller system clock
- 8 Hz timebase output for real-time clock
- Three-wire serial control
- 5 V supply
- 16-pin DIP (LM7001) and 20-pin MFP (LM7001M)

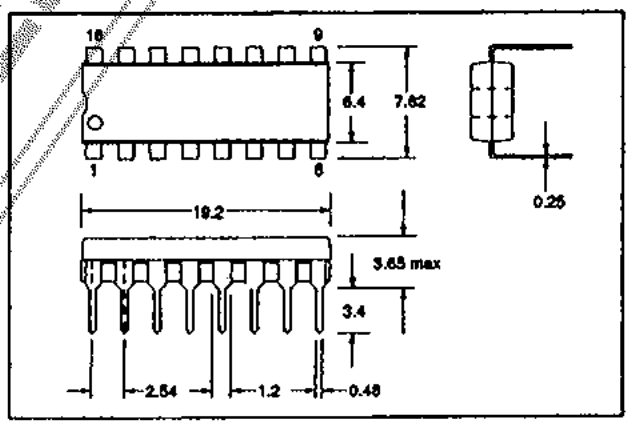
PINOUTS



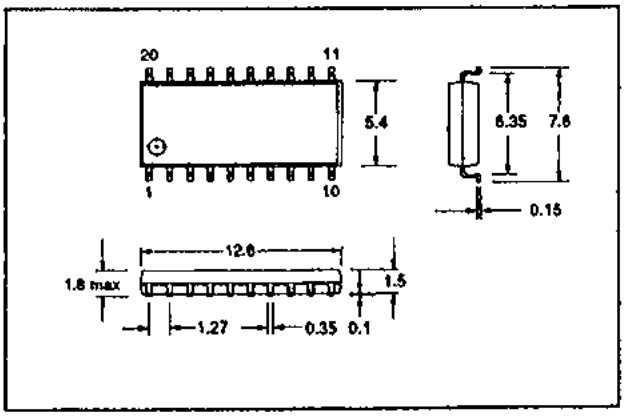
PACKAGE DIMENSIONS

Unit: mm

3006B-DIP16



3036B-MFP20



Specifications and information herein are subject to change without notice.

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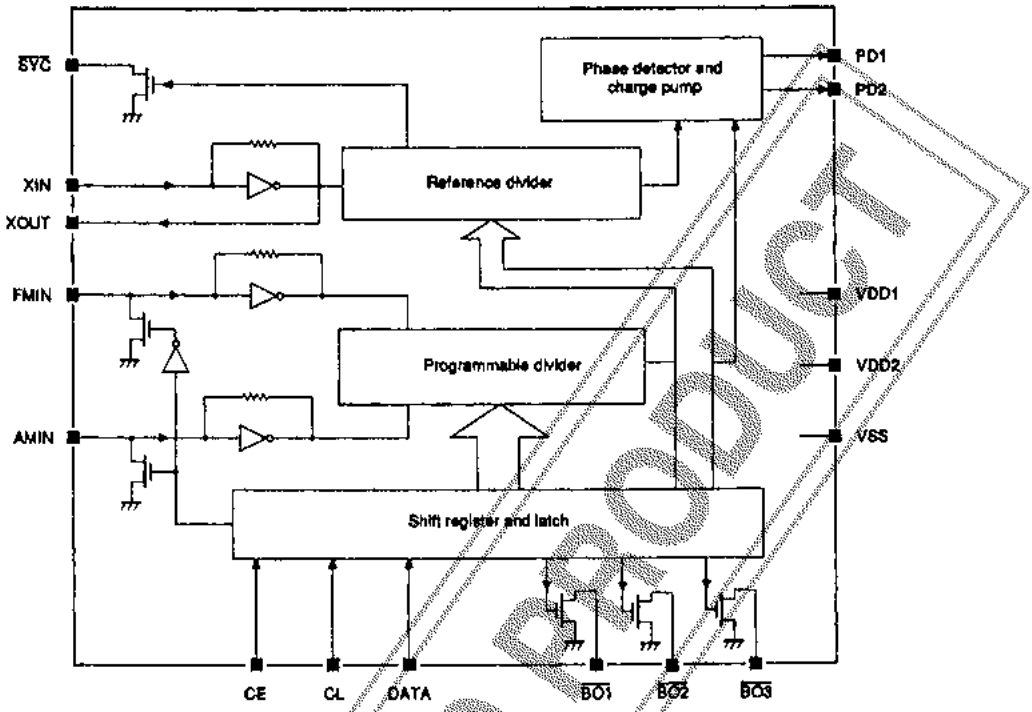
BLOCK DIAGRAM



PIN DESCRIPTION

Number		Name	Description
LM7001	LM7001M		
1	1	XOUT	7.2 MHz crystal oscillator output
2	2	XIN	7.2 MHz crystal oscillator input
–	3	NC	No connection
3	4	CE	Chip enable
4	5	CL	Clock input
5	6	DATA	Serial data input
6	7	$\overline{SYC}$	400 kHz controller clock output
7	8	$\overline{BO1}$	Bandswitching output 1. Can be used for an 8 Hz timebase output
8	9	$\overline{BO2}$	Bandswitching output 2
9	10	$\overline{BO3}$	Bandswitching output 3
–	11	NC	No connection
10	12	AMIN	AM local oscillator input
–	13	NC	No connection
11	14	FMIN	FM local oscillator input
–	15	NC	No connection
12	16	VDD1	5 V supply
13	17	VDD2	5 V backup supply

Number		Name	Description
LM7001	LM7001M		
14	18	PD1	Phase detector charge pump output 1
15	19	PD2	Phase detector charge pump output 2
16	20	VSS	Ground

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD} max	−0.3 to 7.0	V
Logic-level input voltage range	V_{IN1} max	−0.3 to 7.0	V
Analog input voltage range	V_{IN2} max	−0.3 to V_{DD} + 0.3	V
$\overline{SYC}$ output voltage range	V_{OUT1} max	−0.3 to 7.0	V
$\overline{BO1}$, $\overline{BO2}$ and $\overline{BO3}$ output voltage range	V_{OUT2} max	−0.3 to 13	V
PD1, PD2 and XOUT output voltage range	V_{OUT3} max	−0.3 to V_{DD} + 0.3	V
$\overline{BO1}$, $\overline{BO2}$ and $\overline{BO3}$ output current range	I_{OUT} max	0 to 3	mA
Power dissipation	P_D	300	mW
Operating temperature range	T_{opg}	−40 to 85	deg. C
Storage temperature range	T_{stg}	−55 to 125	deg. C

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}	5	V
	V_{DD2}	5	V
Supply voltage range	V_{DD1}	4.5 to 6.5	V
	V_{DD2}	3.5 to 6.5	V

Electrical Characteristics

T_a = −40 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CE, CL, DATA HIGH-level input voltage	V_{IH}		2.2	–	6.5	V
CE, CL, DATA LOW-level input voltage	V_{IL}		0	–	0.7	V
$\overline{SYC}$ output voltage	V_{OUT1}		0	–	6.5	V
$\overline{BO1}$, $\overline{BO2}$ and $\overline{BO3}$ output voltage	V_{OUT2}		0	–	13	V
XIN input frequency	f_{IN1}	Sine wave, capacitive coupling	1.0	7.2	8.0	MHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
FMIN input frequency	f_{IN2}	Sine wave, capacitive coupling, S = 1. See notes 1 and 5.	45	–	130	MHz
		Sine wave, capacitive coupling, S = 1. See notes 2 and 5.	5	–	30	MHz
AMIN input frequency	f_{IN3}	Sine wave, capacitive coupling, S = 0	0.5	–	10	MHz
Crystal oscillator frequency	f_{XTAL}	Crystal impedance ≤ 30 Ω	5.0	7.2	8.0	MHz
XIN input voltage	V_{IN1}	Sine wave, capacitive coupling	0.5	–	1.5	V
FMIN input voltage	V_{IN2}	Sine wave, capacitive coupling	0.1	–	1.5	V
AMIN input voltage	V_{IN3}	Sine wave, capacitive coupling	0.1	–	1.5	V
XIN internal feedback resistance	R_{f1}		–	1.0	–	MΩ
FMIN internal feedback resistance	R_{f2}		–	500	–	kΩ
AMIN internal feedback resistance	R_{f3}		–	500	–	kΩ
CE, CL, DATA HIGH-level input current	I_{IH}	V_{IN} = 6.5 V	–	–	5.0	μA
CE, CL, DATA LOW-level input current	I_{IL}	V_{IN} = 0 V	–	–	5.0	μA
FMIN, AMIN LOW-level output voltage	V_{OL1}	I_{OUT} = 0.5 mA	–	–	3.5	V
$\overline{SYC}$ LOW-level output voltage	V_{OL2}	I_{OUT} = 0.1 mA. See note 3.	0.02	–	0.3	V
$\overline{BO1}$ to $\overline{BO3}$ LOW-level output voltage	V_{OL3}	I_{OUT} = 2.0 mA	–	–	1.0	V
$\overline{SYC}$ output leakage current	I_{OFF1}	V_{OUT} = 6.5 V	–	–	5.0	μA
$\overline{BO1}$ to $\overline{BO3}$ output leakage current	I_{OFF2}	V_{OUT} = 13 V	–	–	3.0	μA
PD1 to PD2 HIGH-level output voltage	V_{OH}	I_{OUT} = –0.1 mA	0.5V_{DD}	–	–	V
PD1 to PD2 LOW-level output voltage	V_{OL4}	I_{OUT} = 0.1 mA	–	–	0.3	V
PD1 to PD2 HIGH-level leakage current	I_{OFFH}	V_{OUT} = V_{DD}	–	0.01	10.0	nA
PD1 to PD2 LOW-level leakage current	I_{OFFL}	V_{OUT} = 0 V	–	0.01	10.0	nA
Supply current	I_{DD1}	See note 4.	–	25	40	mA
	I_{DD2}	PLL inhibited	–	2.0	3.5	mA
FMIN input capacitance	C_{IN}		1	2	3	pF

Notes

1. f_{ref} = 25, 50 or 100 kHz
2. f_{ref} ≠ 25, 50 or 100 kHz
3. V_{DD} = 3.5 to 6.5 V
4. f_{IN2} = 130 MHz, V_{IN2} = 100 mV. XIN and XOUT are connected to a 7.2 MHz crystal. All other input pins are connected to V_{SS} and all output pins are open.
5. S is the divider select bit in the serial data input string.

FUNCTIONAL DESCRIPTION

Input Data Format

The LM7001 and LM7001M are controlled from a three-wire serial bus, which comprises chip-enable, clock and serial data inputs. The 24-bit serial data input comprises 14 divider select bits (D0 to D13), two test control bits (T0 and T1), three bandswitching output control bits (B0 to B2), one timebase control bit (TB), three reference frequency select bits (R0 to R2) and one divider select bit (S) as shown in figure 2.

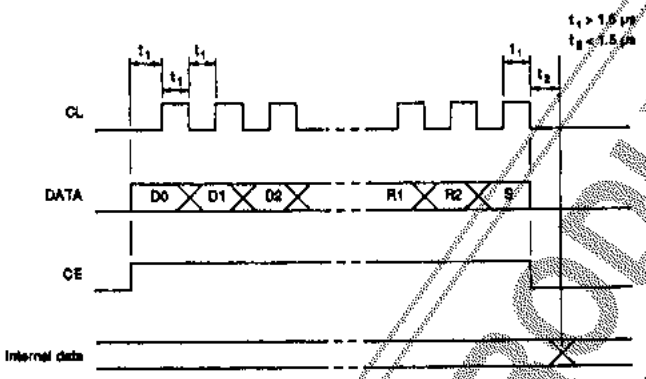


Figure 1. Input waveform diagram

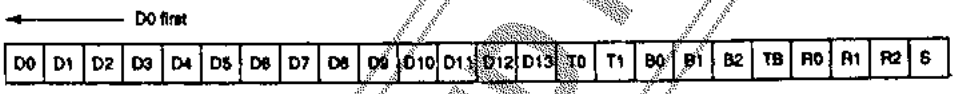


Figure 2. Input data format

Divider Ratio Select

Bits D0 to D13 select the FMIN divider ratio. Bits D4 to D13 select the AMIN divider ratio as shown in figure 3. The S bit selects the FMIN divide function when set to 1, and AMIN, when cleared to 0.

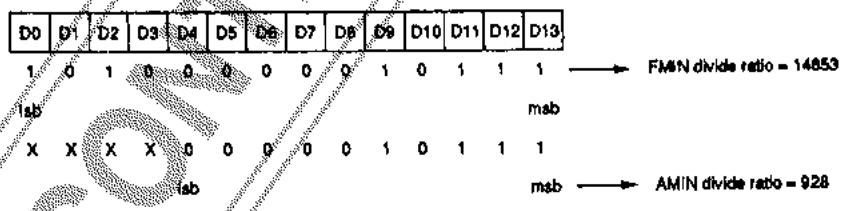


Figure 3. Divider ratio select

Test Control

Bits T0 and T1 should be cleared to 0 for normal operation.

Bandswitching and Timebase Control

Bits B0 to B2 and bit TB select the state of the bandswitching outputs $\overline{BO1}$ to $\overline{BO3}$ as shown in table 1.

Table 1. Bandswitching output select

Input				Output		
B0	B1	B2	TB	$\overline{BO1}$	$\overline{BO2}$	$\overline{BO3}$
0	0	0	0	See note 1.		
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	See note 2.	
×	1	0	1	TB	1	0
×	0	1	1	TB	0	1
×	1	1	1	TB	1	1
1	0	0	1	TB	0	0

Notes

1. Bits R0, R1 and R2 select the state of $\overline{BO1}$, $\overline{BO2}$ and $\overline{BO3}$ as shown in table 2.
2. Bits R0, R1 and R2 select the state of $\overline{BO2}$ and $\overline{BO3}$ as shown in table 2.
3. The timebase frequency is 8 Hz when TB is set to 1.
4. × = don't care

Reference Frequency Select

Bits R0 to R2 select the reference frequency as shown in table 2. In addition, bits R0 to R2 select the bandswitching outputs $\overline{BO1}$ to $\overline{BO3}$ when bits B0 to B2 are all 0.

Table 2. Reference frequency select

R0	R1	R2	f_{ref} (kHz)	$\overline{BO1}$	$\overline{BO2}$	$\overline{BO3}$
0	0	0	100	1	1	0
0	0	1	50	1	1	0
0	1	0	25	1	1	0
0	1	1	5	0	0	1
1	0	0	10	1	0	1
1	0	1	9	1	0	1
1	1	0	1	0	1	1
1	1	1	5	0	0	1