Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)

Specification Update

May 2004

Notice: The ICH2 and ICH2-M products may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 298242-027

Contents

Revision History

Revision	Description	Date
-001	Revised to be consistent with new release of combined Intel 82801BA I/O Controller Hub 2 (ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet.	November 2000
-002	Updated Errata #4, added Errata #20 and #21, added Specification Change #2, added Documentation Change #13.	November 17, 2000
-003	Added Errata #22–#25; added Specification Change #3–#5, added Specification Clarification #5–#7, added Documentation Change #14–#19. Documentation Change #1, Revision ID table, updated	April 2001
-004	Added Errata #26–32; Specification Changes #6–#7; Specification Clarifications #8; Documentation Changes #2–#5 and modified Specification Change #4 Erratum 4 fixed in ICH2X/ICH2XMC0 Stepping.	May 2001
-005	Deleted errata # 28 & 29 as they are duplicates of errata 22 & 4 respectively. Corrected errata 22 (now fixed). Added: Errata: Unexpected SMI With S1M and AC'97 Reset Race Condition, Specification Changes: AC'97 Signal DC Characteristics Change and VBIAS Specification Removed, Specification Clarifications: IDE Hot Swap, Document Change: CLK66 Power Well Change and T190 Correction. Modified: Control Bits For B-4 Stepping Specification Change (Specification Change #3).	July 2001
-006	Added: Errata: SM Bus Arbitration, Thermal Event Status Not Accurately Reported in Heartbeats and Slave Read Register, and SERIRQ and CLKRUN# Issue; Specification Changes: ARB_DIS Bit Does Not Gate PCI Arbiter From Issuing GNT#'s, I/O APIC Arbitration ID Not Set When APIC Clk Not Running; Specification Clarifications: S1M and I/O APIC Issue, Running Block Read With SECOND_TO_STS Set, SM Bus Slave I/F Access; Document Change: IDE Timing Correction. Changed: Document Change #1 (Added ICH2 B5 & ICH2X C0 steppings) and Specification Change #3 (Changed name to "New Control Bits for ICH2" and changed the scope).	August 2001
-007	Added: Errata: I2C Read Command Issue; Specification Clarifications: Parameter Clarification on PWROK and VRMPWRGD/VGATE Signals, THRM# Not Causing TCO Event Message, and C3_STAT# Is Asserted During S1-D Transitions; Document Changes: USB Timing Table, Change to Document Change #1.	September 2001
-008	Added: Specification Clarifications: Registers in Suspend Well, INTRUDER# Behavior Document Changes: Change to Package Information Deleted: Document Change #20 (PCI Device Revision ID Table) as duplicate information of Document Change #1.	October 2001
-009	Added: Errata: SE0 During Resume Causes Disconnect, PERR# Detection Issue, and PERR# Response Issue. Modified: Specification Change: Dual USB Controller Control Bit.	November 2001
-010	Added: Specification Changes: V5REF_SUS Change Documentation Changes: Change to PM1_EN Power Well Attributes, Arbiter Disable Correction.	December 2001

Revision	Description	Date
-011	Added: Specification Changes: V5REF Specification Change	January 2002
-012	Modified: Specification Changes: V5REF_SUS Change	February 2002
-013	Modified: Erratum: I2C Read Command Issue	March 2002
-014	Added: Erratum: SMI Asserted after STPCLK# Is Active and Stopgrant Received, Delayed Transaction Timeout Bit Issue, SMBus NACK and Proc_Call Issue Specification Clarifications: DMA Clarification, USB Run/Stop Bit Clarification Document Changes: Correction to GST_TCK Accuracy.	April 2002
-015	Added: Erratum: AC'97 Overrun FIFO Error Bit Not Set Specification Clarifications: RTC SET Bit Clarification, SMBus Block Transfers and TCO, End of SMI Bit, SMBus Wake	May 2002
-016	Added: Documentation Change: Table 3-4/SUS_STAT# Change	June 2002
-017	Added: Specification Clarification: 32 Clock Retry Enable Clarification. Documentation Changes: SUSCLK During RSMRST# Assertion, TCO Corrections.	July 2002
-018	Added: Specification Clarification: LPC LPCPD# Protocol Clarification	August 2002
-019	Added: Documentation Change: EEPROM Programming Application Note	September 2002
-020	Added: Specification Clarification: PCI Master Requirement	May 2003
-021	Added: Errata: PCI Non-linear Addressing Erratum Documentation Changes: Figure 2-1 (RTC Circuit) Correction	June 2003
-022	Added: Documentation Changes: PME Wake Doc Change	July 2003
-023	Added: Errata: MW DMA Mode-1 Tdh Erratum Documentation Changes: APM I/O Decode Correction, Memory Map Table Change	August 2003
-024	Added: Documentation Changes: SMBus Host_Busy Correction	September 2003
-025	Added: Documentation Change: PWRBTN_STS Note Addition	November 2003
-026	Added: Erratum: LPC Starvation Erratum	January 2004
-027	Added: Erratum: USB Buffer Overrun Erratum Specification Clarifications: Port 63/65/67 and GPI ACPI Clarifications	May 2004

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document
Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet	290687-002

Nomenclature

Errata are design defects or errors. Errata may cause the ICH2 behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® 82801BA I/O Controller Hub (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M). Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or
(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

NoFix :There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Errata No.	Steppings								Status	ERRATA
	ICH2 B0	ICH2 B1	ICH2 B1'	ICH2-M B2	ICH2X B0	ICH2 B4	ICH2 B5	ICH2X C0		
1	X								Fixed	Intermittent Resetting of Specific Resume-Well Bits
2	X	X	X	X	X	X	X	X	No Fix	Inadvertent Setting of Intel® ICH2 SMBus BYTE_DONE_STS Bit
3	X	X	X	X	X	X	X	X	No Fix	Top Block Swap and Delayed Transaction
4	X	X	X	X	X	X			Fixed	Intel® ICH2 Dual USB Controllers and Legacy USB Keyboard and Mouse Support
5	X	X	X	X	X	X	X	X	No Fix	Intel®ICH2 AC '97 "Missed Sample"
6	X	X	X	X	X	X	X	X	No Fix	Intel®ICH2 CF9 Full Reset
7	X	X	X						Fixed	RTCRST# Doesn't Reliably Reset All RTC-Well Configuration Bits
8	X	X	X						Fixed	PCI Parity Error Detection
9	X	X	X	X	X	X	X	X	No Fix	Hub Interface Parity Error Response
10	X	X	X	X	X	X	X	X	No Fix	I/O APIC and C2/C3
11	X	X	X	X	X	X	X	X	No Fix	SMBus Slave I/F Hard Reset Causes Resume
12	X	X	N/A						Fixed	Intel® SpeedStep™ Technology/Sleep State Transition Issue
13	X	X	X	X	X	X	X	X	No Fix	LPC Signaled Target Abort Generation
14	X	X	X	X	X	X	X	X	No Fix	USB Handshake
15	X	X	X	X	X	X	X	X	No Fix	Frequency Strap
16	X	X	X	X	X	X	X	X	No Fix	USB Rise Fall Matching (Trfm)
17	X	X		N/A	X				Fixed	Intel® ICH2 Data Coherency
18			X	N/A	N/A				Fixed	Intel® ICH2 B1' PCI Latency
19	X	X	X	N/A	X				Fixed	Intel® ICH2 Entry into S1/S3 (Intel® 850 and Intel® 860 Chipset Only)
20	N/A	N/A	X	N/A	N/A				Fixed	Intel® ICH2 B1' PCI Buffer Management Boundary Condition
21	X	X	X	X	X	X	X	X	No Fix	DMA Mode-0
22	X	X	X	X	X	X			Fixed	Parity Error
23	X	X	N/A	X	X	N/A	X	X	No Fix	Unexpected INTR, SMI#, or NMI on Resume from S1M
24	X	X	X	X	X	X	X	X	No Fix	Special Cycle Non-Zero Address
25	X	X	X	X	X	X	X	X	No Fix	Power-Button/CF9 Reset
26	X	X	X	X	X	X	X	X	No Fix	LPC Reset Timing
27	X	X	X	X	X	X	X	X	No Fix	S1M LDRQ# Assertion
28	X	X	X	X	X	X	X	X	No Fix	TRDY# Behavior
29	X	X	X	X					Fixed	USB VCRS
30	X	X	X	X	X	X	X	X	No Fix	LAN Microcontroller PCI Protocol Violation
31	N/A	N/A	N/A	X	X	N/A	X	X	No Fix	Unexpected SMI with S1M

Errata (Sheet 2 of 2)

Errata No.	Steppings								Status	ERRATA
	ICH2 B0	ICH2 B1	ICH2 B1'	ICH2-M B2	ICH2X B0	ICH2 B4	ICH2 B5	ICH2X C0		
32	X	X	X	X	X	X	X	X	No Fix	AC '97 Reset Race Condition
33	X	X	X	X	X	X	X	X	NoFix	SM Bus Arbitration
34	X	X	X	X	X	X	X	X	NoFix	Thermal Event Status Not Accurately Reported in Heartbeats and Slave Read Register
35	N/A	N/A	N/A	X	N/A	N/A	N/A	N/A	NoFix	SERIRQ and CLKRUN# Issue
36	X	X	X	X	X	X	X	X	NoFix	I2C Read Command Issue
37	X	X	X	X	X	X	X	X	NoFix	SE0 During Resume Causes Disconnect
38	X	X	X	X	X	X	X	X	NoFix	PERR# Detection Issue
39	X	X	X	X	X	X	X	X	NoFix	PERR# Response Issue
40	X	X	X	X	X	X	X	X	NoFix	SMI Asserted after STPCLK# Is Active and Stopgrant Received
41	X	X	X	X	X	X	X	X	NoFix	Delayed Transaction Timeout Bit Issue
42	X	X	X	X	X	X	X	X	NoFix	SMBus NACK and Proc_Call Issue
43	X	X	X	X	X	X	X	X	NoFix	AC '97 Overrun FIFO Error Bit Not Set
44	X	X	X	X	X	X	X	X	NoFix	PCI Non-linear Addressing Erratum
45	X	X	X	X	X	X	X	X	NoFix	MW DMA Mode-1 Tdh Erratum
46	X	X	X	X	X	X	X	X	NoFix	LPC Starvation Erratum
47	X	X	X	X	X	X	X	X	NoFix	USB Buffer Overrun Erratum

Specification Changes

Number	Steppings								SPECIFICATION CHANGES
	ICH2 B0	ICH2 B1	ICH2 B1'	ICH2-M B2	ICH2X B0	ICH2 B4	ICH2 B5	ICH2X C0	
1	X	X	X	X	X	X	X	X	AC '97 Integrated Pull-Down Control
2	X	X	X	X	X	X	X	X	DMA Mode-0 Not Supported
3						X	X	X	Control Bits for B-4 Stepping
4	X	X	X	X	X	X	X	X	Crystal Load Capacitance Change
5	X	X	X	X	X	X	X	X	Addition of Non-Condensing Environment Requirement
6	X	X	X	X	X	X	X	X	USBCLK PPM Change
7							X	X	Dual USB Controller Control Bit
8	X	X	X	X	X	X	X	X	AC '97 Signal DC Characteristics Change
9	X	X	X	X	X	X	X	X	VBIAS Specification Removed
10	X	X	X	X	X	X	X	X	ARB_DIS Bit Does Not Gate PCI Arbiter From Issuing GNT#s
11	X	X	X	X	X	X	X	X	I/O APIC Arbitration ID Not Set When APIC CLK Not Running
12	X	X	X	X	X	X	X	X	V5REF_SUS Change
13	X	X	X	X	X	X	X	X	V5REF Specification Change

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	Clarification of Alternate Access Mode Usage for Timer (8254)
2	AC '97 Register Access Requirements
3	GPE Event Handling under ACPI
4	Virtual Wire Mode B Usage in Intel® ICH2 DT
5	USB Handshake Errata Workaround Clarification
6	APIC Controller Behavior Clarification
7	Bus_Addr_Track and Bus_Cyc_Track Clarification
8	USB Overcurrent Detection In Sleep States
9	IDE Hot Swap
10	S1M and I/O APIC Issue
11	Running Block Read with SECOND_TO_STS Set
12	SM Bus Slave I/F Access
13	Parameter Clarification on PWROK and VRMPWRGD/VGATE Signals
14	THRM# Not Causing TCO Event Message
15	C3_STAT# Is Asserted during S1-D Transitions
16	Registers in Suspend Well
17	INTRUDER# Behavior
18	DMA Clarification
19	USB Run/Stop Bit Clarification
20	RTC SET Bit Clarification
21	SMBus Block Transfers and TCO
22	End of SMI Bit
23	SMBus Wake
24	32 Clock Retry Enable Clarification
25	LPC LPCPD# Protocol Clarification
26	PCI Master Requirement
27	Port 63/65/67 Clarification
28	GPI ACPI Clarification

Documentation Changes (Sheet 1 of 2)

No.	DOCUMENTATION CHANGES
1	PCI Device Revision ID Table Added
2	GPIO[3:4] Multiplexed with PIRQ[F:G]
3	Discard Timer Mode Bit
4	Vih9 Specifications for RTCX1
5	GPIO[28:27] Should Be on Vol6/Voh6
6	Correction to Descriptions of CPUPERF# and SSMUXSEL Signals
7	No Pull-Up Resistors Needed for PME#
8	Change in Notes for GPIO Use Select Register
9	Change to SUS_STAT# State during C3
10	Correction to Table 6-2 (Fixed IO Ranges Decoded by Intel® ICH2)
11	Correction for Table 16-2
12	Correction for PWROK min Deassertion Specification
13	Correction for Boot Block Update Scheme (6.4.1-3).
14	PME_EN Cleared Only by RTCRST#.
15	USB_Status:[HC_Halted] Is READ_ONLY.
16	Corrections to Section 5.1.4, SERR# Functionality
17	Front-Side Interrupt Delivery
18	PRD Alignment
19	Correction to Table 16-1
20	IDE PRD Alignment
21	EEPROM Control Register Correction
22	CLK66 Power Well Change
23	T190 Correction
24	IDE Timing Correction
25	Change to Control Bits for B-4 Stepping Specification Change
26	USB Timing Table
27	Change to Document Change #1
28	Change to Package Information
29	Change to PM1_EN Power Well Attributes
30	Arbiter Disable Correction
31	Correction to GST_TCK Accuracy
32	Table 3-4/SUS_STAT# Change
33	SUSCLK during RSMRST# Assertion
34	TCO Corrections
35	EEPROM Programming Application Note
36	Figure 2-1 (RTC Circuit) Correction
37	PME Wake Doc Change
38	APM I/O Decode Correction

Documentation Changes (Sheet 2 of 2)

No.	DOCUMENTATION CHANGES
39	Memory Map Table Change
40	SMBus Host_Busy Correction
41	PWRBTN_STS Note Addition

Identification Information

Markings

Intel® ICH2 Stepping	S-Spec	Top Marking	Notes
ICH2 B0	SL45HQ	FW82801BAM Q967, Q968	Production, Mobile
ICH2-M B1	SL4HN	FW82801BAM QA36, QA37	Production, Mobile
ICH2-M B2	QA56, QA57	FW82801BAM QA56, QA57	Engineering Sample, Mobile
ICH2-M B2	SL4R6	FW82801BAM	Production, Mobile
ICH2 B0	Q965, Q966, QA11	FW82801BA	Engineering Sample
ICH2 B0	SL45H	FW82801BA	Production
ICH2 B1	QA34, QA35	FW82801BA	Engineering Sample
ICH2 B1	SL4HM	FW82801BA	Production
ICH2 B1’	QB18, QB19, QB20	FW82801BA	Engineering Sample
ICH2 B1’	SL4YG	FW82801BA	Production
ICH2 B4	QB54, QB55	FW82801BA	Engineering Sample
ICH2 B4	SL59Z	FW82801BA	Production
ICH2X B0	SL5FC	FW82801BA	Production ICH2X External Fab
ICH2X B0	QB69, QB70, QB73, QB74	FW82801BA	Engineering Sample ICH2X External Fab
ICH2X C0	SL5PN	FW82801BA	Production ICH2X External Fab
ICH2X C0	QC09, QC10, QC13, QC14	FW82801BA	Engineering Sample ICH2X External Fab
ICH2 B5	SL5WK	FW82801BA	Production
ICH2 B5	QC51, QC52	FW82801BA	Engineering Sample

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Errata

1. Intermittent Resetting of Specific Resume-Well Bits

Issue: Internal signal to reset specific resume-well register bits crosses power planes. Differing voltage levels between the two power planes make this particular signal sensitive to noise caused by PCI traffic, or accesses to CMOS RAM or registers.

Implication: USB-related bits could get reset. The following issues could arise:

The Port Enable bit could get reset, which could result in the intermittent disabling of USB ports or the loss of ability to resume via USB activity or loss of USB device functionality after resume by other means.

The Global Suspend bit could also get reset, which could result in the loss of ability to resume via USB devices.

The USB Connect Status Change bit could also be reset, which may cause the connection of new devices on the USB ports to be missed by software. This will only occur if it is reset prior to End-Of-Frame. This issue has not been seen in Intel testing.

The USB Port Suspend bit could also be reset. This could cause USB devices to consume normal current after having been suspended. This feature is not used by current USB devices.

The USB Port Enable/Disable Change bit could also be reset. This could result in software missing the disconnection of devices on the USB ports. This would only occur if it is reset prior to End-Of-Frame. This issue has not been seen in Intel testing.

System Management related bits could get reset. The following issues could arise:

The first Alert on Lan* heartbeat could be missed due to the TCO watchdog timer expiring. In this case the heartbeats will begin with subsequent timeouts.

The status of CPU Power Failure Reporting bit may be inconsistent, which may result in the system management software not reliably report failing VRM.

The status of BOOT_STS bit may be inconsistent; that is, the BOOT_SYS bit may be set when the processor has not fetched the first instruction. Therefore no system traffic may occur at this time which could reset this bit.

Note: None of these system management related issues have been observed in Intel testing environments. The effects on these system management bits are based on theoretical design analysis only.

Workaround: **Hardware Workaround:**

First measure VccRTC - VccSus1_8 with an oscilloscope using a differential probe to measure the voltage delta, and then look for the lowest point in the voltage ripple. This should be done with while the system is undergoing PCI/CMOS traffic. This can be done by using a simple program that repeatedly accesses the CMOS RAM or registers to generate traffic and simulate worse-case ripple.

If the voltage differential between VccRTC - VccSus1_8 is always greater than 1.2 V, then no hardware or software workaround is needed. If, however, the voltage differential droops to less than 1.2 V, then one or more of the following steps can be implemented to get the voltage differential greater than 1.2 V. Step 1 should be tried first, and if the voltage drop is not large enough then proceed to step 2:

STEP 1:

Use a low voltage drop Schottky diode between VccSus3_3 and VccRTC. An example of this diode is a Bat 54 diode.

STEP 2:

Reduce the value of VccSus1_8 to 1.7 V by changing the resistor values at the voltage regulator. The minimum spec for VccSus1_8 has been changed to changed to 1.6 V (see Spec Change #12 in this document).

All of the implications are fixed by this hardware workaround. If these steps cannot be implemented, then use the software workaround.

Software Workaround:

Note: The software workaround is not required for the following operating systems: Microsoft Windows* 98, Windows* 2000, and Windows* Me. It is required for legacy (DOS mode) USB keyboard/mouse support. It will correct the USB Port Enable bit issue and the Global Suspend bit issue. There is no software fix for the USB Connect Status Change bit, the USB Port Suspend bit, the USB Port Enable/Disable bit, or any of the System Management implications.

To fix the USB Port Enable bit issue, periodically re-enable USB ports via SMI. To fix the Global Suspend bit issue, re-enable the USB ports and set Global Suspend bit prior to going into suspend mode. Details and sample code are provided in the latest ICH2-M BIOS Specification Update.

Status: Fixed in B-1 stepping.

2. Inadvertent Setting of Intel® ICH2 SMBus BYTE_DONE_STS Bit

Issue: The ICH2 may inadvertently set the BYTE_DONE_STS bit, in the SMBus Host Status register, when the INTR bit for the n+1 interrupt is set at the end of a block write transfer of two bytes or more.

Implication: The ICH2 will hang the next attempted transfer causing an SMBus lockup if this BYTE_DONE_STS bit is not cleared before the next attempted transfer. This can result in a system lock-up requiring an AC power-cycle to recover from.

Workaround: Ensure that a 1 is written to the BYTE_DONE_STS bit at the same time the INTR bit (both in the SMBus Host Status register) is being cleared for the “n+1” interrupt, regardless if interrupts are used or not.

Status: There are no plans to fix this erratum.

3. Top Block Swap and Delayed Transaction

Issue: The Top Block Swap feature of the ICH2 doesn't work correctly if the PCI Delayed Transaction feature is enabled.

Implication: Re-programming the Boot Block of the FWH will fail if the Top Block Swap feature is used with Delayed Transactions enabled.

Workaround: When updating BIOS, disable Delayed Transactions by clearing the DTE bit (D31:F0, offset D0h, bit 1) before setting the TOP_SWAP bit (D31:F0, offset D4h, bit 13). After the update is completed and verified, re-enable Delayed Transactions by setting DTE after clearing TOP_SWAP.

Status: There are no plans to fix this erratum.

4. Intel® ICH2 Dual USB Controllers and Legacy USB Keyboard and Mouse Support

Issue: USB Legacy Keyboard/Mouse Control (USB_LEGKEY) register is physically shared between both USB controllers, but appears to SW as two separate registers.

Implication: **Scenario #1:** When legacy USB keyboard/mouse support is enabled, control is handed off from BIOS to OS at OS boot time. The OS takes control of one controller at a time, first stopping Controller #1, then disabling USB SMI# generation and enabling interrupt generation via bits in the USB_LEGKEY register. At this point, Controller #2 is still running and can generate an interrupt, but there is no interrupt handler in place. The end result is system hang or blue screen.

This issue only affects systems in which legacy USB keyboard/mouse support is enabled for both USB controllers.

Scenario #2: When using Microsoft Windows Me, the system could reboot or hang upon wakeup from a S1 sleep state when a USB device is plugged into the first USB controller and another USB device is plugged into the second controller.

Specifically, when the system experiences a wake event from S1 sleep state, its USB status register has its Resume Detect bit set or USB Interrupt bit set or USB Error Interrupt bit set, and if USB interrupts are enabled in the USB_LEGKEY register, the host controller will generate an interrupt.

Workaround: **Scenario #1:**

Option 1: BIOS can assign a dedicated IRQ to USB Controller #2, which is not shared by any other device in the system (i.e. IRQ7).

Option 2: In the INT19 Bootstrap Loader, BIOS can execute the following steps:

- Disable interrupt generation by USB Controller #2.
- Set up 16 ms periodic SMI to poll USB Controller #2 for keyboard/mouse activity.
- Set up 8 s periodic SMI to monitor system boot activity for 4 minutes, and watch for OS taking control of USB Controller #2.
- After 4 minutes of boot activity:
  - — Disable previously enabled periodic SMIs.
  - — If OS hasn't taken control, enable interrupt generation by USB Controller #2.

Refer to the ICH2 BIOS Spec Update for complete implementation details.

Scenario #2:

To prevent the host controllers from generating interrupts during resume, BIOS code has to implement the code to clear the pending USB interrupts in the USB status registers of both USB controllers. This code should be implemented in the S1 resume sequence of the sleep SMI handler.

Refer to the ICH2 BIOS Spec Update for complete implementation details.

Status: This erratum has been fixed.

5. Intel® ICH2 AC '97 "Missed Sample"

Issue: If an incoming data overrun occurs on AC-link within a 2 clock time window of an AC '97 write completion on the hub interface, the AC '97 controller will not set the FIFOE status bit.

Implication: Possibility of missing a single sample of incoming (Modem In, Mic In or PCM In) AC '97 data. For audio data, this will be undetectable. For modem data, SW may re-try a packet transmit, resulting in a negligible performance hit (modem data packet re-tries occur frequently due to telephone line noise). Neither Audio nor Modem drivers are affected, since they do not implement overrun error handlers.

The boundary conditions required for this to occur are extremely unlikely. This issue has only been observed in artificial, highly stressed system test environments.

Workaround: Not required.

Status: There are no plans to fix this erratum

6. Intel® ICH2 CF9 Full Reset

Issue: There is a boundary condition in which a Full Reset via the CF9h register will not assert SLP_S3# and SLP_S5# for the specified 3 to 5 seconds.

When SW attempts a Full Reset via a CF9h write, ICH2 will assert SLP_S3# and SLP_S5#. If PWROK# does not de-assert within 120 µs, and the ICH2 does not see at least 5 PCICLKs after SLP_S3# and SLP_S5# are asserted, these signals will be asserted for only ~300 µs (instead of the specified 3 to 5 seconds).

Implication: Some systems will not perform the expected power cycling in response to a Full Reset via a CF9h write. This may result is some motherboard devices not being properly reset.

Only affects systems in which both of the following conditions are true:

- PWROK does not de-assert within 120 µs after SLP_S3# assertion.
- At least 5 PCICLK edges cannot be guaranteed after SLP_S3# assertion.
  - — This will be true if SLP_S3# connects to clock generator's PWRDOWN# pin.

Workaround: Option 1: For systems that connect SLP_S3# to the clock generator's PWRDOWN pin, use an RC delay on SLP_S3# to ensure > 5 PCICLKs after ICH2 asserts SLP_S3#.

Option 2: Use SLP_S3# to gate PWROK assertion to ICH2.

Status: There are no plans to fix this erratum.

7. RTCRST# Doesn't Reliably Reset All RTC-Well Configuration Bits

Issue: Assertion of the ICH2's RTCRST# signal does not reliably reset all RTC-well register bits to their default states as documented.

Implication: Some RTC-well configuration bits may not be restored to their expected default states when booting after RTCRST# assertion (See Document Change #36 for the affected bits).

Workaround: BIOS should already be checking the RTC_PWR_STS bit during POST (this bit is not affected by the issue). If this bit is set, BIOS should explicitly reset all RTC-well register bits to the desired default states.

An alternate workaround, requiring board changes, would force VBAT to ground at its source, ensuring that all signals powered by the coin cell battery are forced to 0 V.

Status: Fixed in B-2 stepping of ICH2.

8. PCI Parity Error Detection

Issue: ICH2, as target of a PCI Write transaction, calculates parity and may improperly signal a parity error during Master-initiated wait state cycles.

Implication: Can't support Parity Error Response on the ICH2's PCI bus.

Workaround: Disable Parity Error Response in the Bridge Control Register (D30:F0:3Eh) by setting bit 0 to a value of 0.

Status: Fixed in B-2 stepping of ICH2.

9. Hub Interface Parity Error Response

Problem: ICH2 does not generate a valid Hub Interface Parity message when Parity Error Response is disabled for the Hub/PCI Bridge function.

Implication: System hang if Hub Interface Parity Error Response is enabled in the MCH when it is disabled in the ICH2. This issue only affects platforms in which the MCH supports Hub Interface Parity checking (840, 850, 860, 870). The issue has only been observed with the Linux* OS.

Workaround: Software must not disable Hub Interface Parity Error Response in the ICH while it is enabled in the MCH.

Status: There are no plans to fix this erratum. A patch for Linux will be posted to the "Kernel Web Site."

10. I/O APIC and C2/C3

Problem: A boundary condition exists in which completion of delivery of an interrupt by the I/O APIC coincides with completion of a LVL2 or LVL3 read by the CPU (to enter C2 or C3 state).

Implication: Interrupts that hit this boundary condition will not break the system out of C2/C3. The interrupt will not be processed until another break event occurs. In the case of IRQ8 (RTC interrupt), the ISR will not have cleared the RTC Alarm Flag bit, and no further RTC interrupts will be generated until a subsequent break event allows the ISR to complete. The result of this is time loss from the perspective of the SW clocks that depend on RTC interrupts (the HW RTC clock does not lose time).

Workaround: Systems that support the I/O APIC cannot support C2/C3 states. The C2/C3 states are not necessary for desktop systems. Systems that must support C2/C3 states (mobile systems) cannot support the I/O APIC.

Status: There are no plans to fix this erratum.

11. SMBus Slave I/F Hard Reset Causes Resume

Problem: An SM Bus Slave Hard Reset command received via the SMLINK I/F when the system is in S5 will wake the system, even if the S5 state was entered due to Power Button Override.

Implication: If for some reason a system hangs, the watchdog timer will expire and ICH2 will start sending heartbeat messages to the LAN management console. A user may recognize that the system is hung, and shut it down by a Power Button Override. Meanwhile, a network administrator may have been alerted to the hang by the heartbeat messages, and attempt to reset the system remotely. The user would see the system wake up unexpectedly when the remote reset message is received.

Workaround: None identified.

Status: There are no plans to fix this erratum.

12. Intel® SpeedStep™ Technology/Sleep State Transition Issue

Issue: Some Intel® SpeedStep™ signals are affected by PCI reset. This causes problems when entering S3~S5 with the processor in Maximum Performance mode.

Implication: System reset causes immediate auto-resume and system hang.

Workaround: BIOS workaround is to set the Low Power state before setting SLP_EN and set it back to Max performance state after system resume.

Status: Fixed in B-2 stepping of ICH2-M.

13. LPC Signaled Target Abort Generation

Problem: If there is a downstream I/O cycle followed by posted memory writes, both targeted towards PCI with different BE#s and with Delayed Transaction enabled (D31:F0;GEN_CNTL(D0-D3h):[1]), the ICH2-M can erroneously set the STA bit (bit-11) in D31:F0;PCISTS configuration space even though there is no Target Abort on the PCI bus. This has only been observed on DP systems.

Implication: The STA bit in D31:F0;PCISTS is incorrectly set. No NMI or SERR# will be generated due to the STA bit being set. Software which polls this STA bit may incorrectly indicate a Target Abort has occurred.

Workaround: There are two possible workarounds:

1) Ignore the STA bit (bit-11) in D31:F0;PCISTS(06-07h) when Delayed Transaction is enabled. The D30:F0;SECSTS(1E-1Fh):[RTA (bit-12)] bit remains an accurate reflection of downstream cycles towards PCI that get Target Aborted.

2) Disable Delayed Transaction (which may induce a performance penalty on PCI)

Status: There are no plans to fix this erratum.

14. USB Handshake

Problem: The ICH2 UHCI will fail to provide a handshake if it receives an incoming data packet where CRC has five consecutive ones in the least significant bit of CRC and is immediately followed by an EOP for Bulk, Interrupt, and Isoc transfers ONLY IF a K-state is being signalled on the other port at the time of this EOP. This behavior, to date, has only been observed during artificial testing procedures.

Implication: USB devices may stall. The OS will attempt to recover, but if it fails to do, an error message will be displayed. The user may have to unplug then re-install the USB device that has stalled.

Workaround: There are two possible workarounds to choose from:

1. Do not use the specific selective suspend feature of the ICH2 when there can be activity on the other bus. Global Suspend must be employed.

2. Do not allow USB peripherals to use remote wake feature (form selective suspend).

Status: There are no plans to fix this erratum.

15. Frequency Strap

Problem: The ICH2 will not drive the CPU frequency straps signal (A20M#, INTR, NMI, IGNNE#) to ones as VCC comes up prior to PWROK assertion(t184). The ICH2 drives these signals to zero instead.

Implication: No implication to qualification and productions processors as they drive their own “start” straps internally. Implication to pre-qual processors is that the “start ratio” may be set to an illegal value and the system may not boot.

Workaround: (Not required for systems using qualification or production processors)

1. Re-implement Legacy mux that drives ones prior to PWROK.
2. PLace a 1.2 ms RC delay on CPUPWRGD so that it asserts when ICH2 Run ration Freq Strap values are present.

Status: There are no plans to fix this erratum.

16. USB Rise Fall Matching (Trfm)

Problem: The USB Specification defines a rise/fall time matching (Trfm) which is calculated by dividing rise time by fall time (Tr/Tf). The ICH2 does not meet this specification.

Implication: This erratum will result in a lower crossover voltage which is still within the specification (Vcrs)

Workaround: None

Status: There are no plans to fix this erratum.

17. Intel® ICH2 Data Coherency

Problem: During a PCI Memory Read Line or Memory Read Line Multiple command from a PCI master, the ICH2 will pre-fetch up to three, 32-byte cache lines from main memory and store the data in its internal pre-fetch buffers. During this pre-fetch process, the pre-fetched data may become invalid either during transit to the ICH2 or while residing in the ICH2 pre-fetch buffers, due to CPU activity. In this case, the ICH2 should invalidate its pre-fetch buffer and request new data prior to delivering data to the requesting PCI master. However, in some cases, this does not occur, thus allowing "invalid" data to reach the requesting PCI master.

Implication: "Invalid" data may be delivered to a PCI master. This issue only occurs in 850/860 chipset-based systems due to the unique architectural interactions between the MCH and the ICH2. Intel® Pentium® III processor-based systems (with 810/E2, 820/E, 840/E chipsets) are based on a different architecture and are not affected by this erratum.

Workaround: None.

Status: Fixed in B-1' stepping of the ICH2.

18. Intel® ICH2 B1' PCI Latency

Problem: The ICH2 B1' may delay time sensitive, isochronous data from reaching the targeted PCI device when running certain applications that require high bandwidth CPU writes directly to a PCI device operating in non-bus mastering mode. Components within the ICH2, such as IDE, USB, LAN, and AC '97 are not affected by this erratum. This erratum only affects devices residing on the ICH2's PCI bus.

Implication: When running an application that executes a large number of CPU writes to a non-PCI bus master device, the performance of some time sensitive, isochronous-class PCI components may be reduced.

Workaround: Don't use time sensitive, isochronous PCI devices together with an application that writes a large amount of data to a non-bus mastering PCI device.

Status: Fixed in B-4 stepping of the ICH2.

19. Intel® ICH2 Entry into S1/S3 (Intel® 850 and Intel® 860 Chipsets Only)

Problem: Entry into S1 or S3 state may result in a delayed entry or possible system hang when running a compute intensive application that does not perform a blocking operation (e.g., system call for I/O, faults for needing I/O, relinquishing time quantum) while executing at high OS priority within an ACPI and APIC enabled OS. This is a boundary condition where the OS powers down PCI devices required to generate system bus interrupt messages to end a processor compute intensive application that does not perform a block operation before software has relinquished control to the OS.

Note: This erratum only affects platforms based on the Intel® 850 and Intel® 860 chipsets.

Implication: Effects the use of the I/O APIC feature in the ICH2 when running compute intensive, high priority application under an ACPI and APIC enabled OS resulting in a system hang or delayed entry into S1 and/or S3.

Workaround: Use 8259 interrupt mode.

Status: Fixed in B-4 stepping of the ICH2.

20. Intel® ICH2 B1' PCI Buffer Management Boundary Condition

Problem: A rare PCI bus boundary condition exists that may cause ICH2 B1' abnormal behavior if a very specific set of data transfers occur at a precise time. Below are the specific conditions and sequence list that must happen in order to see this boundary condition to occur.

1) PCI bus master requests multiple or line read data from main memory.

2) MCH returns some of the read data to the ICH2, but the PCI bus is stalled causing the data to be buffered in the ICH2.

3) A combination of interleaved writes and reads fills the ICH2 Hub Interface buffer and the data backs up into the MCH buffer.

4) ICH2 PCI bus frees up beginning to empty ICH2 Hub Interface FIFO allowing data to begin bursting across the Hub Interface from MCH to the ICH2.

Burst sequence must match the following

5) Burst processor writes to PCI (must be 1 or 2 DWords only).

6) Burst read data to PCI bus master (Hub Interface FIFO must be filled with at least 24 DWords before this begins).

7) Burst processor write to the PCI bus.

8) Burst read data to PCI bus master.

Conditions which are necessary for this erratum to be seen

9) The first read from the above Burst Cycle sequence (step #6) must occur at the same time (within 4 PCI clocks) as the PCI bus becomes unstalled.

Either of the following conditions must then occur

10) The last read from the above Burst Cycle sequence (Step #8) must occur on the same clock edge as the ICH2 buffer is flushed (due to write at step #5).

-OR-

10) Another write to PCI must occur after the burst read data (Step #8)

11) The last write in the burst sequence (above) must occur on the same clock that the write (Step #7) completes on PCI.

Implication: During a very specific set of data transfers to the PCI bus, with a specific set of stall conditions, when two independent events occur on the same clock edge, the ICH2 B1' may operate incorrectly which will cause a platform lock-up. A hard-reset has to be performed in order to regain system functionality.

This errata has not been seen in a real life system environment. This erratum has only been seen in simulation and controlled test environments.

PCI cards placed in the system which cause a high amount of CPU to PCI traffic may increase exposure to this erratum.

Workaround: None.

Status: Fixed in B-4 stepping of the ICH2.

21. DMA Mode-0

Problem: If a device on one of the IDE interfaces, such as the secondary channel, is operating in Multi-Word DMA Mode with compatible timings where the cycle time is 600 ns, while a device on the other interface (primary channel), is running in PIO mode, the IDE PIO prefetch buffer will inadvertently provide an extra piece of secondary channel data to the primary device, resulting in data corruption. This happens when DMAREQ is deasserted and a DMA transaction is running while a PIO transaction is outstanding on the other channel. Note that DMA Mode-0 is an unsupported mode of the ICH2.

Implication: Systems configured in this manner may experience a situation in which the DMA IDE controller transfers incorrect data from the PIO configured device. Exactly how this manifests itself in a system is dependent on the system activity at that time.

Workaround: When BIOS is determining which mode(s) an IDE device is capable of, it must not set the DMA capable bits in the ICH2 if that device only supports Mode-0 DMA or slower. That device should be configured for PIO instead.

Status: This will not be fixed in the ICH2.

22. Parity Error

Problem: When enabled, a Parity Error will not be signaled or detected, via either D30:F0;1Eh bit-8 or D31:F0;06h bit-8 (SECSTS:[DPD] or PCISTS:[DPED]), if 2 Double-Word up-bound writes are followed by a down-bound read. Neither PERR# will be asserted, nor the indicated status bits will be set, resulting in failure to generate NMI or SMI. Note that the Hub I/F Parity Error detect mechanism remains fully functional with regards to this erratum.

Implication: This results in loss of indication to PCI target and system software when bad PCI data is received. This could result in data corruption to either memory or hard drive data.

Workaround: None.

Status: This was fixed in the ICH2X C0.

23. Unexpected INTR, SMI#, or NMI on Resume from S1M

Problem: When entering S1M, peripheral PCI clocks including PCI clock to the Super IO will be stopped earlier (one clock after STP_PCI# is asserted) compared to PCI clock to the ICH2 which is stopped later after SLP_S1# is asserted. If a SERIRQ agent is driving an active low on the SERIRQ on the last PCI clock before it is stopped, the active low will be maintained on the SERIRQ line. Since PCI clocks to the ICH2 are still running for some time, the ICH2 may misinterpret this as a request for INTR, SMI#, or NMI (depending on which SERIRQ slot is being sampled).

Implication: Unexpected INTR, SMI#, or NMI may occur when resuming from S1-Mobile suspend state.

Workaround: Disable SERIRQ before entering S1-M state and re-enable after exiting from S1-M. This will prevent generation of unexpected interrupts. SERIRQ can be disabled by writing a ‘0’ to D31:F0;64h bit-7. Refer to the ICH2 BIOS Spec Update for additional details.

Status: This will not be fixed in the ICH2/ICH2-M.

24. Special Cycle Non-Zero Address

Problem: Special Cycles immediately followed by any cycle(s) (within 3 Hub I/F clocks) may result in the ICH2 driving non-zero data during the address phase of the special cycle The PCI specification only requires that stable data be driven during the address phase, which happens, it does not require that it be 0x0h data.

Implication: Non-PCI compliant devices may attempt to claim this special cycle and it may not function properly. This has only been seen on one PCI graphics card, which is no longer produced.

Workaround: None.

Status: There are no plans to fix this erratum.

25. Power-Button/CF9 Reset

Problem: If the power-button is pressed (PWRBTN# is asserted) during a CF9 hard reset event (an IO write of 06h to CF9h), the ICH2/ICH2-M will behave as if a power-button override event has occurred and transition the system to the S5 state (off).

Implication: If a CF9 hard reset sequence is initiated while the power-button is depressed, the system may unexpectedly transition to the S5 state (turn off). The user will have to awaken the system by pressing the power-button.

Workaround: Software must test the PWRBTN# status bit before attempting a CF9 hard reset sequence to reduce the boundary of this failure.

Status: There are no plans to fix this erratum.

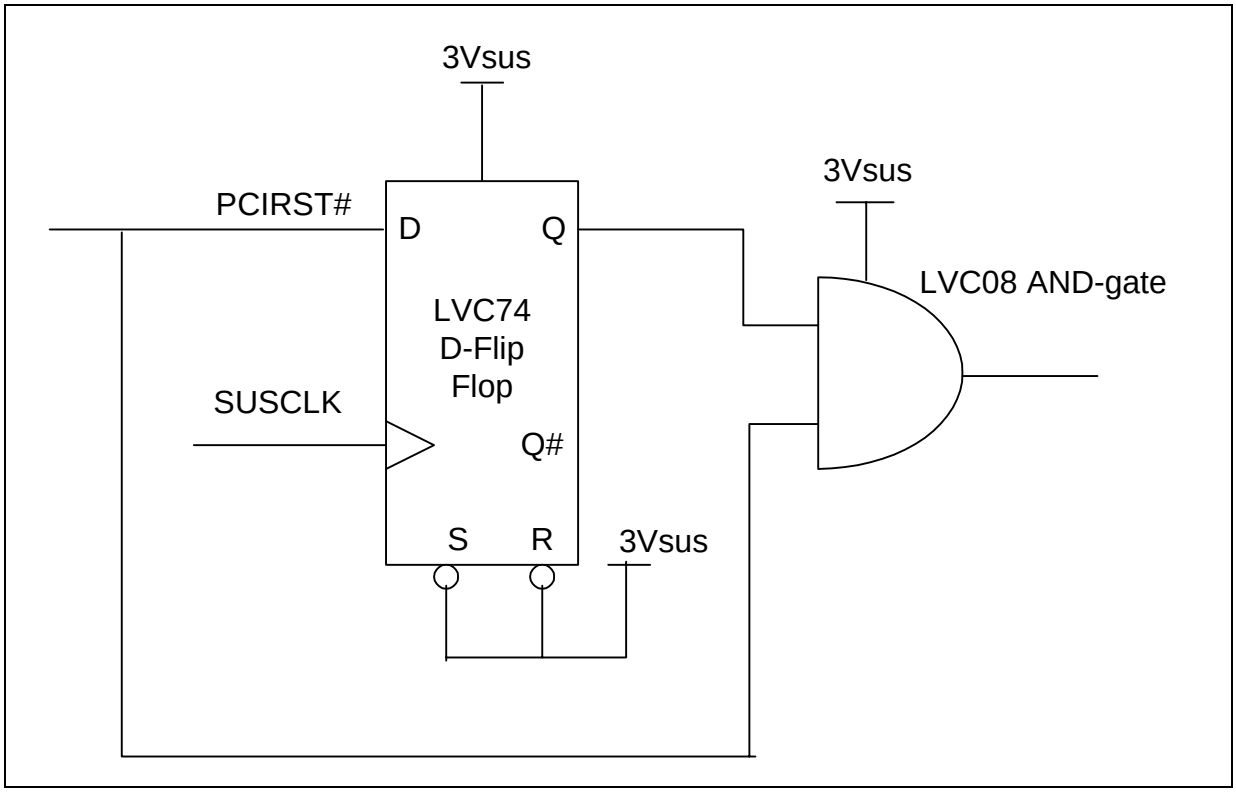
26. LPC Reset Timing

Problem: The ICH2/ICH2-M specified 1-3 RTC clock timing of SUS_STAT# inactive to PCIRST# inactive violates the LPC specification (Rev 1.0) of “at least 60 µs.”

Implication: Some LPC devices may not properly reset resulting in failure of the system to boot or resume from a sleep state.

Workaround: Use any one of these three workarounds:

1) Delay PCIRST# by 1 susclk using a D-flop and an AND gate to the LPC devices.



2) Do a CF9 Hard Reset (06h) within the first 100 ms of POST.

3) Do not connect the ICH2/ICH2-M SUS_STAT# to the SIO PD input, instead implement an external pull-up resistor on the PD input of the SIO device.

Status: There are no plans to fix this erratum.

27. S1M LDRQ# Assertion

Problem: During a transition to S1M, the ICH2-M will assert SUS_STAT#. Some SIOs have been found to drive the LDRQ# low in response to SUS_STAT# going low, which is compliant to the LPC specification. Accordingly, the ICH2-M should shut off the LDRQ# input buffer when SUS_STAT# is driven low. However, the ICH2-M does not do this, and consequently sends an erroneous DMA transfer, which may cause a system hang.

Implication: 1) A hang may result if DMA cycles are not suppressed upon entry/exit from S1M.

2) After resuming from S1M, once the DMA unit is enabled to operate, an erroneous DMA transfer may occur which could cause a variety of different failures in the system depending on the attributes of the transfer.

Workaround: Details of the ICH2-M software workaround is available in the *Intel® ICH2 BIOS Specification Update*.

Status: There are no plans to fix this erratum.

28. TRDY# Behavior

Problem: The ICH2/ICH2-M may not assert TRDY# for more than 16 PCI clocks (up-to 32 clocks) after a bus master asserts FRAME# if there are no other masters requesting the bus. This behavior is inconsistent with its Sub-class code of a PCI-to-PCI Bridge device.

Implication: The ICH2/ICH2-M may not respond with a data phase within 16 PCI clocks, as required by the *PCI Specification*. This has not been found to cause any functional problems. Since prior generations of chipsets were required to meet 32 clock requirements for a Host-to-PCI Bridge, PCI adapters that worked in these systems should also work in an ICH2/ICH2-M based system.

Workaround: None.

Status: There are no plans to fix this erratum.

29. USB V_{CRS}

Problem: The USB buffer V_{CRS} (crossover voltage) may be below the USB specified 1.3 V on some devices.

Implication: USB devices may not enumerate, may drop off or may experience other forms of inoperability if the peripheral itself violates the T_{FST}/T_{LST} SE0 rejection specification of the *USB Specification*.

Workaround: Increase the 3.3 V Standby (VccSUS3_3) to 3.45V to provide increased V_{CRS} margin. This workaround will not guarantee that all parts will meet this 1.3 V specification.

Status: This was fixed in the ICH2X and ICH2 B4 steppings.

30. LAN Microcontroller PCI Protocol Violation

Problem: When the ICH2/ICH2-M (using the 82562ET PLC) is receiving large files from a peer LAN device using the 10 Mbps data rate, the ICH2/ICH2-M can cause a system lock-up. Specifically, if the LAN controller has Standby Enable set (EEPROM Word 0Ah bit-1 = 1), while receiving large files using the 10 Mbps data rate and receives a CU_RESUME command when it is just entering IDLE state, the ICH2/ICH2-M will cause a PCI protocol violation (typically by asserting FRAME# and IRDY# together) within the next few PCI cycles. This will cause the PCI bus to lock-up, further resulting in system lock-up.

Implication: Large file transfers to the ICH2/ICH2-M using 10 Mpbs can cause the receiving system to lock-up.

Workaround: Clear EEPROM Word 0Ah bit-1 to 0. This will result in an increase power consumption of the ICH2/ICH2-M of ~ 40 mW.

Status: There are no plans to fix this erratum.

31. Unexpected SMI with S1M

Problem: When entering S1M, peripheral PCI clocks including the PCI clock to the Super IO will be stopped one clock after STP_PCI# is asserted. In the S1M transition SUS_STAT# is asserted, and in response some SERIRQ agents may drive active low on SERIRQ. The active low may be maintained on the SERIRQ line, as the SERIRQ agents observes SUS_STAT# assertion. The PCI clock to the ICH2-M is stopped later after SLP_S1# is asserted. Since PCI clocks to the ICH2-M are still running for some time, the ICH2-M may misintrepret this as a request for an SMI, INTR, or NMI (depending on which SERIRQ slot it being sampled). Upon exit from S1M an SMI, INTR, or NMI may occur in response to this misintrepreretation.

Implication: Unexpected INTR, SMI, or NMI may occur when resuming from S1M suspend state. System implications will be BIOS/OS dependent. Based on the type of interrupt detected this may result in a system hang.

Workaround: A BIOS workaround has been validated in which SERIRQ must be disabled before entering S1M state and re-enabled after exiting from S1M. This will prevent generation of unexpected interrupts. SERIRQ can be disabled by writing a ‘0’ to D31:F0;64h bit-7.

Status: This will not be fixed in the ICH2-M.

32. AC ’97 Reset Race Condition

Problem: If an AC’97 reset is initiated (via GLB_CNT:[1]) just as a new frame is starting, a race condition between AC_RST# asserting and AC_SDIN transitioning from “Ready=1” to ground, due to the reset, may cause an unexpected wake event (SMI), if AC’97 wake events are enabled (via GPE0_EN).

Implication: This will result in an unexpected wake event (SMI) that may not be comprehended by the SMI handler resulting in repeated SMI’s.

Workaround: Early in enumeration disable AC ’97 wake events and re-enable it after enumeration. BIOS must disable SMI & PME generation when doing a reset to or powering down the codecs. BIOS should clear the related status registers and then re-enable SMI & PME generation.

Status: This will not be fixed in the ICH2/ICH2-M.

33. SM Bus Arbitration

Problem: The ICH2/ICH2-M will not detect a bus collision when attempting to STOP at the end of a SMBus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, the ICH2/ICH2-M may not set the Bus Error bit.

Implication: A master attempting a transfer that had actually "lost" may think that its transaction was completed.

Workaround: None.

Status: This will not be fixed in the ICH2/ICH2-M.

34. Thermal Event Status Not Accurately Reported in Heartbeats and Slave Read Register

Problem: The ICH2/ICH2-M Temp Event Status in heartbeat messages and Slave Read Register 4 may not accurately reflect the status of the THRM# pin in S1M, S3, and S4 sleep states.

Implication: While in S1M, S3, or S4 sleep states, in the unlikely event that a thermal situation is reached, it will not be detected by an external controller for purposes of thermal throttling.

Workaround: None.

Status: This will not be fixed in the ICH2/ICH2-M.

35. SERIRQ and CLKRUN# Issue

Problem: If Dynamic PCI Clock control is enabled (CLKRUN_EN - Dev31, Func 0, Offset A0, bit-2 set to '1'), STP_PCI# may be asserted while ICH2-M is driving SERIRQ Start Frame, causing a boundary condition during which ICH2-M may continue to drive a SERIRQ Start Frame for up to two clocks while the external PCICLK to the Super I/O Controller (SIO) may be stopped. If SERIRQ Start Frame is set to 4 clocks (Start Frame Pulse Width - Dev31, Func 0, Offset 64, bits 1:0 = '00'), the SIO may misintrepret the Start Frame driven from the ICH2-M.

Implication: System may hang.

Workaround: BIOS should program SERIRQ Start Frame to either 6 or 8 clocks.

Status: This will not be fixed in the ICH2-M.

36. I2C Read Command Issue

Problem: The ICH2 uses the HST_D0 register (Dev31, Func 3, Offset 05h) as the byte count register instead of depending on the LAST_BYTE bit in the Host Control register (Dev 31, Func 3, Offset 02h:[bit-5]) to end the transaction.

Implication: The transaction will stop pre-maturely if HST_D0 contains a number smaller than the intended transaction.

Workaround: No workaround for 10-bit addressing I^2C devices. Can use the SM Bus read command for 7-bit addressing of I^2C devices.

Status: This will not be fixed in the ICH2/ICH2-M. The I2C Read command is de-featured.

37. SE0 during Resume Causes Disconnect

Problem: A transient SE0 during an upstream resume signal from the USB peripheral to the ICH2/ICH2-M while the system is in the S3/S4 sleep states will cause the ICH2/ICH2-M to register a disconnect for that port. This violates the USB Rev 1.1 specification.

Implication: The implication is operating system dependent. It can range from additional latency on a resume before the USB device is functional (after the resume), to the USB device no longer working (after the resume) - in which case a system reboot must be done to obtain functionality for that USB device. In all cases the rest of the system does resume normally.

Workaround: None.

Status: This will not be fixed.

38. PERR# Detection Issue

Problem: The ICH2/ICH2-M's Detected Parity Error (DPE) bit in SECSTS register (D30:F0, offset 1Eh: bit-15) and PCISTA register (D31:F0, offset 06h: bit-15) will get set when PERR# is asserted by external PCI devices. This issue was found during ongoing validation using a synthetic test environment and there have been no failures reported by customers.

Implication: DPE bit of SECSTS and PCISTA may erroneously get set.

Workaround: BIOS needs to clear DPE of SECSTS and PCISTA when those bits are set.

Status: This will not be fixed.

39. PERR# Response Issue

Problem: If ICH2/ICH2-M's Parity Error Response Enable (PER) bit in Bridge_CNT register (D30:F0, offset 3Eh: bit-0) is disabled (default), it will block PERR# from being asserted when data parity error is detected on PCI bus during LPC or legacy DMA master read cycles, or when ICH2/ICH2-M is the target for write cycles to Device 31 Functions 0 and 3. This bit should only block PERR# from being asserted when a PCI data parity error is detected during PCI-to-memory writes or CPU-to-PCI read cycles. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

Implication: PERR# will not be asserted when PCI Parity Error detected during LPC or legacy DMA master read cycles, or when ICH2/ICH2-M is the target for write cycles to Device 31 Functions 0 and 3.

Workaround: BIOS needs to set PER of Bridge_CNT when the parity error detection is supported on LPC or legacy DMA.

Status: This will not be fixed.

40. SMI Asserted after STPCLK# Is Active and Stopgrant Received

Problem: ICH2/ICH2-M should latch SMI when STPCLK# is active. When USB UHCI is active and an SMI is generated by the UHCI, logic does not latch the interrupt with STPCLK#, thus SMI goes low when CPU is in sleep mode.

Implication: SMI could be lost if CPU is in sleep state.

Workaround: None.

Status: This will not be fixed in the ICH2/ICH2-M.

41. Delayed Transaction Timeout Bit Issue

Problem: After a delayed transaction has been serviced the discard timer is not reset, which incorrectly times out. This timeout sets the SERR# Due to Delayed Transaction Timeout bit (D30:F0;92h:bit-1). This may result in generation of SERR# based NMIs if the SERR# enable on Delayed Transaction Timeout bit (D30:F0;90h:bit-1) is set to a '1' by software or system BIOS.

Implication: This erratum may cause excessive NMIs to occur which impacts system performance.

Workaround: System BIOS must clear D30:F0;90h:bit-1 to '0' if the delayed transaction based SERR#'s should not be generated on the platform.

Status: This will not be fixed in the ICH2/ICH2-M.

42. SMBus NACK and Proc_Call Issue

Problem: ICH2/ICH2-M SMBus controller fails to respond after being NACKed on the 4th data phase when using the SMBus command Process Call (with or without I^2C enabled).

Implication: This issue may lockup the SMBus controller and cause the system to stop responding. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by known commercial applications.

Workaround: None.

Status: This will not be fixed in the ICH2/ICH2-M.

43. AC '97 Overrun FIFO Error Bit Not Set

Problem: The ICH2/ICH2-M may not set the FIFO Error Bit in the Input Status register after an overrun error occurs on a highly stressed system in the vicinity of the end of an AC'97 input stream. The bit affected depends on what stream causes the error:

- PCM IN - PISR(D31:F5;NABMBAR+06h:[bit-4])
- Mic IN - MCSR(D31:F5;NABMBAR+26h:[bit-4])
- Modem IN - MISR(D31:F6;MBAR+06h:[bit-4])

Implication: Driver vendors typically do not use this status bit in their production drivers.

Workaround: None.

Status: This erratum will not be fixed.

44. PCI Non-linear Addressing Erratum

Problem: If a PCI Memory Read Multiple or Memory Read Line transaction falls at the last DW of a 32 byte cache line boundary and non-linear addressing (cache-line wrap mode) is used, the ICH2/ICH2-M will prefetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent CPU cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

Implication: None known.

- System hang only seen in a synthetic test environment.

- No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line.

Workaround: None.

Status: No Fix.

45. MW DMA Mode-1 Tdh Erratum

Problem: Data hold time of MW DMA Mode-1 writes may not meet ATA specification.

Implication: None known.

Workaround: Program the controller to PIO Mode-4 instead.

Status: NoFix.

46. LPC Starvation Erratum

Problem: Latency issues on LPC may occur if a PCI bus master is performing large upstream bursts to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may bet delayed until the PCI device completes its transaction and de-asserts its REQ#.

Implication: Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

Workaround: None.

Status: No fix.

47. USB Buffer Overrum Erratum

Problem: If a full-speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20 µs of system latency) and the USB FIFO begins to empty during a 20 ns window immediately prior to teh overrun event actually occuring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

Implication: Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behavior. There is no known exposure with real world applications.

Workaround: None.

Status: No Fix.

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Specification Changes

1. AC ’97 Integrated Pull-Down Control

The integrated pull-down resistors on AC_BITCLK, AC_SDIN:[1:0], and AC_SDOUT can be enabled when either the ACLINK Shut Off bit in the AC ’97 Global Control Register is set or when both function 5 and function 6 are hidden (disabled.) Note 6 below Table 3-2 of page 3-2 will be changed accordingly.

2. DMA Mode-0 Not Supported

DMA Mode-0 is not supported by the ICH2/ICH2-M.

3. New Control Bits for Intel® ICH2

New control bits have been added to the ICH2 Configuration Space for use with Intel® 845/850/860/870 chipsets.

TMR - Test Mode Register (D31:F0)

Offset:	FC-FFh	Attribute:	Read/Write
Default:	00000000h	Size:	32-bit
Lockable:	NO	Power Well:	Core

Bit	Description
31:26	Reserved
25	**BME_Override - (BMEO) - R/W.** This bit enables the delivery of APIC interrupts to the processor when this bit is set to 1. This bit must be set to 1 for 845/850/860/870 systems and be 0 for all other systems.
24:0	Reserved.

D30_Policy - Device 30 Policy Register (D30:F0)

Offset:	B4h	Attribute:	Read/Write
Default:	00h	Size:	16-bits

Bit	Description
15:2	Reserved
1:0	**Prefetch Flush Enable: - R/W.** When set to 11b, this bit causes North PCI logic to deliver “Demand” data for a delayed transaction if a Hub I/F-to-PCI write has occurred since the delayed transaction was initiated These bits must be set to 11b for operation with MCHs that allow CPU-to-Hub I/F writes to pass previously-snooped Hub I/F read completions Bits 1 and 0 must be written with the same value in order for bit-0’s value to change. These bits must be set to 11b for 845/850/860/870 systems and be 00b (default) for all other systems.

4. Crystal Load Capacitance Change

Table 16-6, *Other DC Characteristics*, lists the CL (Crystal Load Capacitance) as between 7.5 pF to 15 pF. This is being changed as follows:

CL (XTAL1) 2.5 - 6 pF Typical

CL (XTAL2) 2.5 - 6 pF Typical

5. Addition of Non-Condensing Environment Requirement

Added to Section 16.1, *Absolute Maximum Ratings*, the following Note is added,

Note: A non-condensing environment is required to maintain RTC accuracy.

6. USBCLK PPM Change

Table 16-7, *Clock Timings*, lists the USB Clock frequency tolerance. This parameter is being changed from 2500 ppm to 500 ppm. The Note 1 associated with this parameter will have the following sentence appended, “The source of this ppm is external to this component.”

7. Dual USB Controller Control Bit

A control bit has been added to the ICH2X C-0 and ICH2 B5 steppings to enable the fix for the ICH2 Dual USB Controllers and Legacy Keyboard and Mouse Support erratum.

TMR - Test Mode Register (D31:F0)

Offset:	FC-FFh	Attribute:	Read/Write
Default:	00000000h	Size:	32-bit
Lockable:	NO	Power Well:	Core

Bit	Description
31:26	Reserved
25	**BME_Override - (BMEO) - R/W.** This bit enables the delivery of APIC interrupts to the processor when this bit is set to 1. This bit must be set to 1 for 850/860 systems and be 0 for all other systems.
24:10	Reserved.
9	**Dual_USB_Register_Enable - (DURE) - R/W.** This bit must be set to make the second USB register visible. If this bit is set, the BIOS workarounds for the related erratum should be removed from the BIOS.
8:0	Reserved.

8. AC ’97 Signal DC Characteristics Change

The DC Characteristics of the AC ’97 signals are being modified to match the AC ’97 specification. Specific changes are:

1) AC ’97 Signals (AC_BITCLK, SDIN[1:0], AC_SYNC) in Table 16-2 are removed from the VIH3/VIL3 specification. These signals are added to a new group “VIH10/VIL10” in Table 16-2.

2) VIH10/VIL10 is added to Table 16-3 as indicated below:

Symbol	Parameter	Min	Max	Unit	Notes
VIL10	Input Low Voltage	-0.5	0.35*Vcc3_3	V	
VIH10	Input High Voltage	0.65*Vcc3_3	Vcc3_3+0.5	V	

9. VBIAS Specification Removed

The DC Characteristic for the VBIAS symbol in Table 16-6 is removed.

10. ARB_DIS Bit Does Not Gate PCI Arbiter from Issuing GNT#s

In Section 9.8.3.8, *PM2_CNT - Power Management 2 Control*, replace the description of ARB_DIS (bit-0) with the following:

ARB_DIS: Arbiter Disable R/W

0 = Enable Hub Interface arbiter.

1 = Disable Hub Interface arbiter. ARB_DIS will only disable the arbiter at the Hub Interface to prevent up-bound traffic. Consequently, the PCI arbiter will continue to issue GNT#'s even when ARB_DIS is set. Note that after the arbiter is disabled, the processor must not initiate any down-bound reads to PCI devices that may have up-bound posted data, as this will result in system deadlock.

11. I/O APIC Arbitration ID Not Set When APIC Clk Not Running

In Section 9.5.8, *ARBID - Arbitration ID Register*, the second sentence of the first paragraph was: "This register is loaded whenever the APIC ID register is loaded." It is changed to "If APIC clock is running, this register is loaded whenever the APIC ID register is loaded."

12. V5REF_SUS Change

Section 2.19, *Signal Description - Power and Ground*, indicate for the V5REF_SUS that this signal only affects 5 V tolerance for USB OC:[3:0]# pins and can be connected to VccSUS3_3 if 5 V tolerance on these signals in not required. If 5 V tolerance is required, it can be connected to the 5V_Always or 5V_AUX rail which remains powered except in S5 state.

V5REF_SUS affects 5V tolerance for all USB signals, both over-current and data pins. Because of this and due to USB specification compliance, the V5REF_SUS pin must be connected to 5VSUS (5V Aux) if USB is implemented. If USB is not implemented then V5REF_SUS can be connected to VCCSus3_3.

New Description:

Name	Description
V5REF_SUS	Reference for 5 V tolerance on USB OC:[3:0]# signals. This power is not expected to be shut off unless power is removed.

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Specification Clarifications

1. Clarification of Alternate Access Mode Usage for Timer (8254)

If the ALT Access Mode is entered and exited after reading the registers of the ICH2 timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1) BIOS enters ALT Access Mode for reading the ICH2 timer related registers.

2) BIOS exits ALT Access Mode.

3) BIOS continues through the execution of other needed steps and passes control to the OS.

After getting control in step #3, if the OS does not reprogram the system timer again the timer ticks may be happening faster than expected. For example DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the timeouts in the software may be happening faster than expected.

Operating systems such as Microsoft Windows 98, Windows 2000 and Windows NT* reprogram the system timer and hence will not run into this problem.

For some other operataing systems, such as MS-DOS, the BIOS should restore the timer back to 54.6 ms before passing control to the OS. If the BIOS is entering ALT Access Mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT Access Mode.

2. AC ’97 Register Access Requirements

Sections 13 and 14 address AC ’97 Audio and Modem Controller Registers. Access to some of these registers is restricted accordingly (all are Read/Modify/Write);

AC’97 Audio Registers

NAMBAR - must align to 256-byte boundary
MABMBAR - must align to 64-byte boundary
x_BDBAR - accessed as 32-bit access only
x_SR - accessed as 16-bit access only
x_PICB - accessed as 16-bit access only
CLOB_CNT - accessed as 32-bit access only
GLOB_STA - accessed as 32-bit access only

AC’97 Modem Registers

MMBAR - must align to 256-byte boundary
MBAR - must align to 128-byte bounder
x_BDBAR - accessed as 32-bit access only
x_SR - accessed as 16-bit access only
x_PICB - accessed as 16-bit access only
GLOB_CNT - accessed as 32-bit access only
GLOB_STA - accessed as 32-bit access only

3. GPE Event Handling under ACPI

The ICH2 uses the same GPE1_EN register (I/O address: PMBase+2EH) to enable/disable both SMI and ACPI SCI general purpose input events. APCI OS assumes that it owns the entire GPE1_EN register per ACPI spec. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case, ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states.

4. Virtual Wire Mode B Usage on Intel® ICH2

When an I/O APIC based system is configured in Virtual Wire Mode B with edge triggered interrupt delivery on the I/O APIC input pin INITIN_0 (INTR output from the 8259), a high-priority interrupt occurring just as the ICH2 receives INTACK for a preceding low-priority interrupt can cause an unusually small interrupt de-assertion on INTR signal which can be missed at either the I/O APIC or the processor, depending on the configuration, and most likely cause a system hang.

The unusually small interrupt de-assertion time does not meet the input min specifications for the device receiving this signal. This may result in a system lockup.

When using Virtual Wire Mode B, where the INTR output of the 8259 is routed to the I/O APIC INTIN_0, software must program the I/O APIC redirection table entry 0, Trigger Mode (bit-15 of redirection table) to Level Sensitive, rather than Edge Sensitive. This may result in infrequent spurious interrupts which should have minimal adverse impact on system performance.

Another consideration is to use Virtual Wire Mode A with the local APICs set to Level Trigger.

5. USB Handshake Errata Workaround Clarification

The USB Handshake Errata identifies a workaround that should allow system software to still be able to use selective suspend. The steps and requirements needed to do this safely are outlined below.

1) Arm all applicable devices for remote wake (prior to suspending),

2) Terminate all transactions on the bus for all ports (to ensure that there are no active data structures reachable by the Host Controller),

3) Places all applicable ports in selective suspend (PORTSCx:[Suspend]=1),

4) Stop the Host Controller (USB.Command:[Run/Stop]=0),

5) Wait for the Host Controller to halt (USB.Status:[HC_Halted]=1),

6) Place the Host Controller in Global Suspend (USB.Command:[Enter Global Suspend Mode]=1).

Note Another requirement is that the time from both ports being suspended (step 3) to the Run/Stop bit being cleared (step 4) must be less than 1 ms, and when the system resumes, software must resume (unsuspend) all suspended ports before initiating traffic on the ports as this will prevent the conditions that cause the stated errata (problem).

6. APIC Controller Behavior Clarification

Section 5.8, *APIC*, describes the APIC controller behavior.

The local APIC (in the processor) has a delivery mode option to interpret Front Side Bus (FSB) messages as an SMI in which case the processor treats the incoming interrupt as an SMI instead of as an interrupt. This does not mean that the ICH2 has any way to have an SMI source from ICH2 power management logic cause the I/O APIC to send an SMI message - there is no way to do this. The ICH2's I/O APIC can only send interrupts due to interrupts which do not include SMI, NMI or INIT. This means that in IA32/IA64 based platforms, FSB interrupt message format delivery modes 010 (SMI/PMI), 100 (NMI), and 101 (INIT) as indicated in Section 5.8.5.5, must not be used and is not supported. Only the hardware pin connection is supported by ICH2.

7. Bus_Addr_Track and Bus_Cyc_Track Clarification

Sections 9.8.3.18 and 9.8.3.19 describe the Bus_Addr_Track and Bus_Cyc_Track registers. The value stored in these registers are based on an SMI event, which can include an asynchronous SMI, not just synchronous SMIs such as an SMI_Trap.

8. USB Overcurrent Detection in Sleep States

The ICH2/ICH2-M will not wake from a USB overcurrent condition when the system is in S1M, S3, S4, and S5 sleep states. In these sleep states neither of the overcurrent status bits in the PORTSC[1:0] register will set. If an overcurrent still exists when the system is in S0 or S1 - then the overcurrent can be detected. This will be added as a note to the PORTSC:[1:0] register.

9. IDE Hot Swap

In an IDE Hot Swap Operation an IDE device is removed and a new one inserted while the IDE interface is powered down and the rest of the system is in a fully powered-on state (S0). During an IDE Hot Swap, if the OS executes cycles to the IDE interface after it has been powered down, which causes the ICH2/ICH2-M to hang the sytem waiting for IORDY to be asserted from the drive.

To correct this issue, the following BIOS procedures are required prior to performing an IDE Hot Swap

1) Program IDE SIG_MODE (config register 54h) to 10b (Drive Low mode).

2) Clear IORDY Sample Point Enable (bits 1 or 5 of IDE Timing register).

This will prevent the ICH2/ICH2-M from not waiting for IORDY assertion when the OS accesses an IDE device after the IDE drive powers down, and ensure that zeros will always be returned for read cycles that occur during a hot swap operation.

10. S1M and I/O APIC Issue

In Section 5.12.7.1, *Initiating Sleep State*, Table 5-41, *Sleep Types*, the following note is added to the comment of S1-M.

Note: ICH2-M requires that the I/O APIC interrupts be masked before entering S1-M. If software does not mask all interrupts in the I/O APIC prior to entering S1-M, the system may hang during resume from S1-M.

11. Running Block Read with SECOND_TO_STS Set

In Section 12.2.2, *HST_CNT - Host Control Register*, the following note is added to the description for LAST_BYTE (bit-5).

Note: Once the SECOND_TO_STS bit in TCO2_STS register (Dev31, Func 0, TCOBase+06h:[1]) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the ICH2/ICH2-M from running some of the SM Bus commands (Block Read/Write, I2C Read, Block I2C Write).

12. SM Bus Slave I/F Access

When an external micro-controller accesses the SM Bus slave interface over the SM Link a translation in the address is needed to accommodate the leaset significant bit used for read/write control. For example, if the ICH2 slave address (RCV_SLVA) is left at 44h (default), the external micro-controller would use an address of 88h/89h (write/read).

13. Parameter Clarification on PWROK and VRMPWRGD/VGATE Signals

The parameter of t177 in Table 16-18 is changed to “PWROK and VRMPWRGD(ICH2)/ VGATE(ICH2-M) both active to SUS_STAT# inactive.

14. THRM# Not Causing TCO Event Message

In Section 5.12.8.1, *THRM# Signal*, the following note is added at the end of the section:

Note: THRM# assertion will not cause TCO event message in S1-M, S3, or S4. The level of the signal will not be reported in the heartbeat message.

15. C3_STAT# Is Asserted during S1-D Transition

In Section 3.10, *Power Management Interface*, Table 2-10, *Power Management Interface Signals*, the following note is added to the description of C3_STAT#.

Note: This signal will be asserted in S1-D, and S1-M on the ICH2-M.

16. Registers in Suspend Well

The following registers/bits are in the suspend well.

USB PORTSC, USB USBCMD:[3], GP_LVL(GPIOBase+0Ch):[28:27, 25:24], GPO_BLINK(GPIOBase+18h):[28:27, 25], and GPI_INV(GPIOBase+2Ch):[13:11, 8].

17. INTRUDER# Behavior

Section 5.13.1 describes INTRUDER# Theory of Operation. The following note is added to the two existing notes on “Handling an Intruder”.

Note: If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written a 1, then INTRD_DET will go to a 0 when INTRUDER# input signal goes inactive.

18. DMA Clarification

Section 9.2.1, *DMABASE_CA*, is being replaced with the following:

Bit	Description
15:0	**Base and Current Address - R/W.:** This register determines the address for the transfers to be performed. The address specified points to two seperate registers. On writes, the value stored in the *Base Address* register and copied to the *Current Address* register. On reads, the value is returned from the *Current Address* register. The address increments/decrements in the Current Address register after each transfer, depending on the mode of the transfer. If the channel is in auto-initialize mode, the Current Address register will be reloaded from the Base Address register after a terminal count is generated. For transfers to/from a 16-bit slave (channels 5-7), the address is shifted left one bit location. Bit 15 will be shifted into Bit 16. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flop/flop. Before accessing an address register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

Section 9.2.3, *DMAMEM_LP*, is being replaced with the following:

Bit	Description
7:0	**DMA Low Page (ISA Address bits [23:16]) - R/W.:** This register works in conjunction with the DMA controller's Current Base Address register to define the complete 24-bit address for the DMA channel. This register remains static throughout the DMA transfer. Bit 16 of this register is ignored when in 16 bit I/O count by words mode as it is replaced by the bit 15 shifted out from the current address register.

Section 5.4.2, *Address Compatibility Mode*, is being replaced with the following:

Whenever the DMA is operating, the addresses do not increment or decrement through the High and Low Page registers. Therefore, if a 24-bit address is 01FFFFh and increments, the next address will be 010000h, not 020000h. Similarly, if a 24-bit address is 020000h and decrements, the next address will be 02FFFFh, not 01FFFFh. However, when the DMA is operating in 16 bit mode, the addresses still do not increment or decrement through the High and Low Page registers but the page boundary is now 128K. Therefore, if a 24 bit address is 01FFFEh and increments, the next address will be 000000h, not 010000h. Similarly, if a 24 bit address is 020000h and decrements, the next address will be 03FFFEh, not 02FFFEh. This is compatible with the 82C37 and Page Register implementation used in the PC-AT. This mode is set after CPURST is valid.

19. USB Run/Stop Bit Clarification

Note: The USB Run/Stop bit should be cleared only under one of the following conditions:

1) There are no active Transaction Descriptiors in the schedule.

2) A reset of the USB host controller is guaranteed prior to a subsequent Run/Stop bit assertion.

20. RTC SET Bit Clarification

The SET bit (bit-7) in RTC_REGB should be set then cleared early in BIOS POST after each powerup directly after coin-cell battery insertion.

21. SMBus Block Transfers and TCO

The BIOS should always clear the SECOND_TO_STS bit (TCO2_STS register, PMBase+06h, bit-1) before executing any SMBus Block Reads or Writes.

22. End of SMI Bit

In Section 9.8.3.13, *SMI_EN*, the following note is added to bit-1:

Note: ICH2/ICH2-M is able to generate the first SMI after reset even though the EOS bit is not set. Subsequent SMI's require EOS bit is set.

23. SMBus Wake

In table 5-42, *Causes of Wake Events* replace the SMBALERT# with the following row:

SMBALERT#	S1-S5	Always enabled as a wake event

In Section 5.17.4, first paragraph, S4 is changed to S5.

In Section 6.8.3.9, *GPE0_STS*, add the following note to bit-7:

Note: The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit-5) should be cleared by software before this bit is cleared.

24. 32 Clock Retry Enable Clarification

The description for the 32 Clock Retry Enable bit (bit-1) in the Device 30 Function 0:CNF(50h) register is incorrect. There is no relationship to PCI locked cycles. The description is changed as indicated below:

32 Clock Retry Enable - R/W System BIOS must set this bit for PCI compliance.

1=The ICH2/ICH2-M will retry a PCI to memory cycle (reads or writes) if the ICH2/ICH2-M is not able to complete the transfer in 32 PCI clocks.

0=The ICH2/ICH2-M will insert as many wait states as needed to complete the PCI to memory cycle.

25. LPC LPCPD# Protocol Clarification

The LPC specification defines the LPCPD# protocol where there is at least 30uS from LPCPD# assertion and LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The ICH2/ICH2-M will assert both SUS_STAT# (connects to LPCPD#) and PCIRST# (connects to LRST#) at the same time when the core logic is reset (via CF9, PWROK, etc). This is not inconsistent with the LPC LPCPD# protocol.

26. PCI Master Clarification

Add Note to 5.1.1 (PCI Bus Interface). Note: PCI Bus masters should not use memory area locations as a target if that area is programmed to be anything but Read/Write.

27. Port 63/65/67 Clarification

Table 6-2 (Fixed I/O Ranges Decoded by the ICH2) incorrectly lists ports 63, 65 and 67 as addresses decoded by the processor I/F. These addresses are entirely removed from this table.

28. GPI ACPI Clarification

Section 5.12.7.2 incorrectly indicates that some GPIs, specifically GPI[7:0], GPI[23:16] are not ACPI compliant when they actually are. The paragraph above Table 5-43 and Table 5-43 are changed as indicated:

“It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from an S1 state. Table 5-43 summarizes the use of GPIs as wake events.”

GPI	Power Well	Wake From	Notes
GPI[7:0], GPI[23:16]	Core	S1	ACPI Compliant
GPI[15:8]	Suspend	S1 - S5	ACPI Compliant

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Documentation Changes

1. PCI Device Revision ID Table Added

PCI Revision ID Register Values (PCI Offset 08h) for all ICH2 functions are shown below.

This information is not listed in the datasheet. This is the standard reference document.

Table 1. Revision ID Table

Function	ICH2 B-0	ICH2 B-1	ICH2 B1'	ICH2 B2	ICH2 B4	ICH2 B5	ICH2X B0	ICH2X C0
D8:F0[1]	1	1	1	3	3	3	3	3
D30:F0	1	2	2	3	4	5	11	12
D31:F1	1	2	2	3	4	5	11	12
D31:F2	1	2	2	3	4	5	11	12
D31:F3	1	2	2	3	4	5	11	12
D31:F4	1	2	2	3	4	5	11	12
D31:F5	1	2	2	3	4	5	11	12
D31:F6	1	2	2	3	4	5	11	12

Note: From a software perspective, the integrated LAN Controller (D8:F0) appears to reside on the secondary side of the ICH2's virtual PCI-to-PCI Bridge. This is typically Bus 1, but may be assigned a different number, depending upon system configuration.

Note: The ICH2's integrated LAN Controller (D8:F0) provides support for configurable Subsystem ID and Subsystem Vendor ID fields. After reset, the LAN Controller automatically reads addresses Ah through Ch of the EEPROM. The LAN Controller checks bits 15:13 in the EEPROM word Ah. ~~For additional information refer to Application Note AP-409 *I/O Controller Hub EEPROM Map and Programming Information*.~~

2. GPIO[3:4] Multiplexed with PIRQ[F:G]

In Table 9-12 of Section 9.10, *General Purpose I/O Registers (D31:F0)*, the column of alternate function for GPIO[3:4] should be PIRQ[F:G] not PIRQ [E:H].

3. Discard Timer Mode Bit

Section 8.1.26 describes the functions of various bits in the ICH2 configuration Register D30:F0 bits is ICH2-M only which is not correct. It should be applied to both ICH2 Desk-Top and Mobile.

4. Vih9 Specification for RTCX1

In Table 16-3 of Section 16.3 *DC Characteristics* Vih10 on the symbol column is not correct, it should beVih9.

5. GPIO [28:27] Should Be on Vol6/Voh6

In Table 16-4, *DC Characteristic Output Signal Association*, the GPIO[28:27] signals should be on Vol6/Voh6.

6. Correction to Descriptions of CPUPERF# and SSMUXSEL Signals

In Table 2-10, within Section 2-10, *Power Management Interface*, the descriptions of both signals CPUPERF# and SSMUXSEL# include the sentence "*If this functionality is not needed this signal can be configured as a GPO*." This sentence (in both places) should be removed.

7. No Pull-Up Resistors Needed for PME#

In Table 16-5 on page 16-5, the note 1 states PME# must have an external pull-up resistor, which is incorrect.

8. Change to Notes for GPIO Use Select Register

In Section 4.10.2, *GPIO_USE_SEL--GPIO Use Select Register*, the first note incorrectly states that GPIO7 is not implemented. GPIO7 should be listed in the second note instead. The two notes should now read as follows:

Note: Bits 31:29, 26, 15:14 and 10:9 are not implemented because there is no corresponding GPIO.

Note: Bits 28:27, 25:22, 20:18, 13:12 and 8:6 are not implemented because the corresponding GPIOs are not multiplexed.

9. Change to SUS_STAT# State during C3

In Table 3-4, within Section 3.4, *Output and I/O Signal Planes and States*, the state of SUS_STAT# is not currently specified in C3. It should be specified as **High**.

10. Correction to Table 6-2 (Fixed IO Ranges Decoded by Intel® ICH2)

The notes 1 and 2 associated with Table 6-2 are incorrectly applied. Note 1 should apply to I/O Address 1F0-1F7 and 3F6 (primary IDE controller), and Note 2 should apply to I/O Address 170-177 and 376 (secondary IDE controller) on the write target column.

11. Correction for Table 16-2

The signal AC_SYNC is listed in Table 16-2, *DC Characteristic Input Signal Association*, and should not be since this signal is an output signal only. This signal AC_SYNC will be removed from this table.

12. Correction for PWROK min Deassertion Specification

The PWROK minimum deassertion requirement at Table 16-9, Figure 16-25, and Figure 16-26 within Section 16.4 *AC Characteristics* are incorrect. Below is a list of changes required for datasheet.

1. In Table 16-19, the description for t196 on the parameter should be changed to "SLP_S3# active to PWROK and VRMPWRGD (VRMPWRGD/VGATRE for ICH2-M) inactive".

2. In Table 16-19, the description for t196a on the parameter should be changed to "PWROK Minimum Deassertion".

3. In Figure 16-25, t196a should be changed to indicate the deassertion width of PWROK. Parameter t196 for VRMPWRGD is also applied to PWROK.

4. In Figure 16-26, t196a should be changed to indicate the deassertion width of PWROK. Parameter t196 for VGATE is also applied to PWROK.

13. Correction for Boot Block Update Scheme (6.4.1 - 3)

In Section 6.4.1, step 3, the third sentence will be changed to read “Processor access to FFFF_0000 through FFFF_FFFF are directed to FFFE_0000 through FFFE_FFFF in the FWH.”

14. PME_EN Cleared Only by RTCRST#

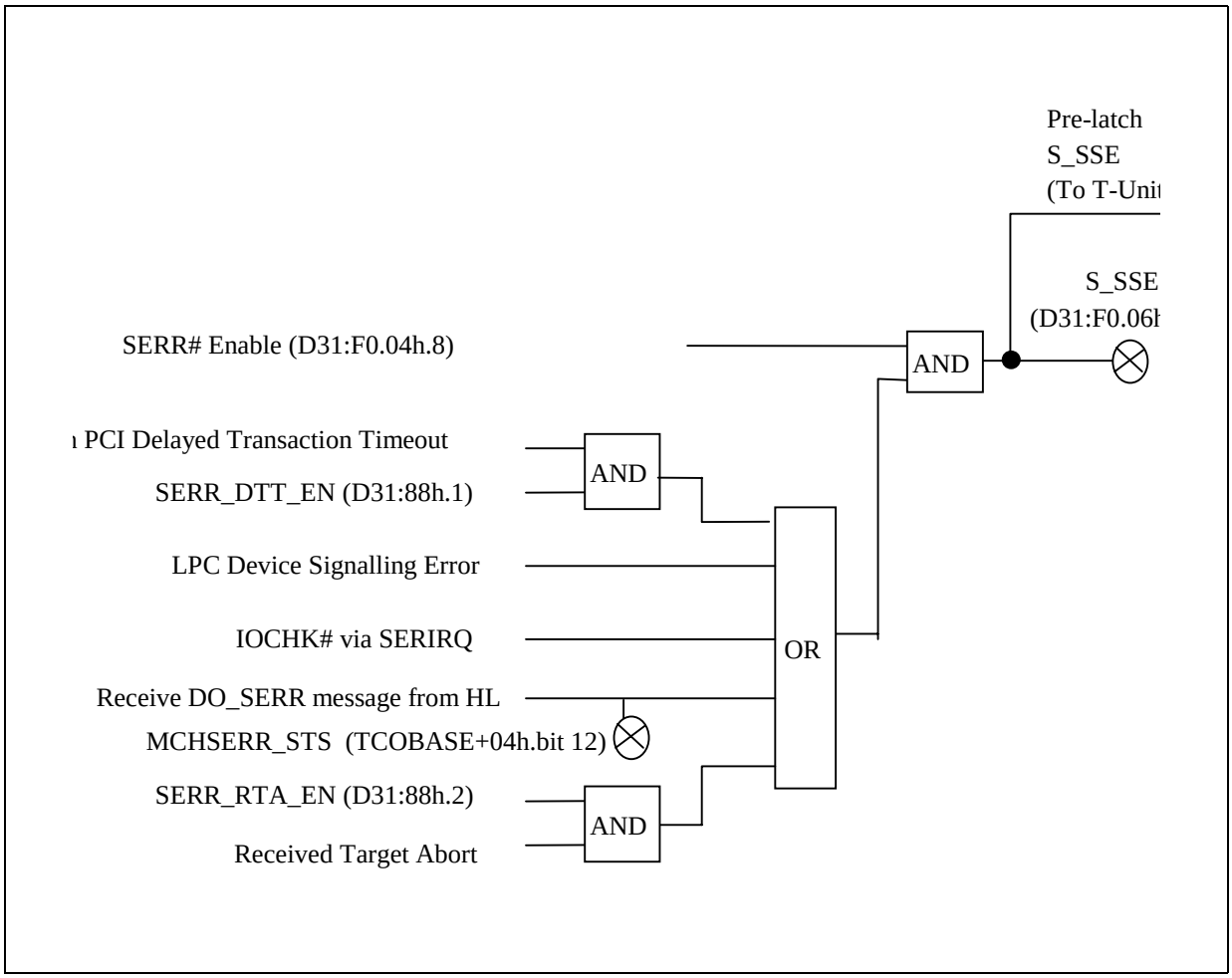
The “Note” at the end of Section 5.12.7.3 incorrectly indicates that PME_EN and PME_STS are cleared by RSMRST#. This note will be changed to indicate that only PME_STS is cleared by RSMRST#. PME_EN is cleared by RTCRST#.

15. USB_Status:[HC_Halted] Is READ_ONLY

Section 11.2.2 of the datasheet indicates that the HC_Halted bit (bit-5) of USB_Status is R/WC. Bit-5 is not R/WC but is READ_ONLY. The statement “0 = Software resets this bit to 0 by writing a 1 to the bit position” will be removed. The other bits remain R/WC.

16. Corrections to Section 5.1.4 SERR# Functionality

The following note is added just below Figure 5-3: “D30:F0;1Eh:[14] (SEC_STS:[SSE]) is only set when SERR# is detected asserted. Additionally, Figure 5-2, *Secondary Status Register Error Reporting Logic*, is replaced with the figure below:



17. Front-Side Interrupt Delivery

The sentence “If the interrupt was active but goes inactive before the EOI is received, the ‘Deassert Message’ is sent.” in Section 5.8.5.3 is removed.

18. PRD Alignment

In Section 5.15.2, the PRD is incorrectly listed as being required to be aligned to 64-KB boundaries. It must be D-Word aligned. It still must not cross a 64-KB boundary.

19. Correction to Table 16-1

The title for Table 16-1 is incorrectly listed as ICH2-M specific, it is for both ICH2 and ICH2-M. This table is being replaced with the one below.

Power Plane	Maximum Sustain Supply Current I_{CC} (max) ICH2-M					
	S0	S1	S3	S4	S5	G3
1.8VCore	300 mA	100 mA	0	0	0	
3.3VI/O	410 mA	5 mA	0	0	0	
1.8VLAN	30 mA	23 mA	6 mA	6 mA	6 mA	
3.3VLAN (LAN+PLC)	186 mA	180 mA	180 mA; 50 mA when LAN PLC placed in reduced power mode (50 MHz ->5 MHz			
1.8VSUS	5 mA	1.8 mA	1.8 mA	1.8 mA	1.8 mA	
3.3VSUS	15 mA	1.4 mA	1.4 mA	1.4 mA	1.4 mA	
V_{CC}RTC						4 µA
Power Plane	**Maximum Sustain Supply Current I_{CC} (max) ICH2-Desktop**					
	S0	**S1**	**S3**	**S4**	**S5**	**G3**
1.8VCore	300 mA	100 mA	0	0	0	
3.3VI/O	410 mA	5 mA	0	0	0	
1.8VSUS	35 mA	25 mA	7.8 mA	7.8 mA	7.8 mA	
3.3VSUS	201 mA	181.4 mA	181.4 mA; 51.4 mA when LAN PLC placed in reduced power mode (50 MHz ->5 MHz			
V_{CC}RTC						4 µA

20. IDE PRD Alignment

Section 5.15.2, *Physical Region Descriptor Format*, second paragraph, describes requirements for the Physical Region Descriptor (PRD). This section incorrectly indicates that the PRD must be aligned to 64-KB boundaries. This paragraph will be changed to indicate that the PRD must be DWord aligned and must not cross a 64-KB boundary.

21. EEPROM Control Register Correction

The EEPROM Control bits are listed in the datasheet in the reverse order. The correct order is indicated below.

EEPROM Control Register (B1:D8:F0)

Offset:	0Eh	Attribute:	RO/R/W
Default:	00h	Size:	8-bits

Bit	Description
7:4	Reserved
3	**EEPROM Serial Data Out (EEDO) - RO.** Note that this bit represents “Data Out” from the perspective of the EEPROM device. This bit contains the value read from the EEPROM when performing read operations.
2	**EEPROM Serial Data In (EEDI) - WO.** Note that this bit represents “Data In” from the perspective of the EEPROM device. The value of this bit is written to the EEPROM when performing write operations.
1	**EEPROM Chip Select (EECS) - R/W.** 0 = Drives the ICH2’s EE_CS signal low, to disable the EEPROM. This bit must be set to 0 for a minimum of 1uS between consecutive instruction cycles. 1 = Drives the ICH2’s EE_CS signal high, to enable the EEPROM.
0	**EEPROM Serial Clock (EESK) - R/W.** Toggling this bit clocks data into or out of the EEPROM. Software must ensure that this bit is toggled at a rate that meets the EEPROM component’s minimum clock frequency specification. 0 = Drives the ICH2’s EE_SHCLK signal low. 1 = Drives the ICH2’s EE_SHCLK signal high.

22. CLK66 Power Well Change

Table 3-5 lists the CLK66 as being in the Main Logic power well. This signal is in the Main I/O power well.

23. T190 Correction

In Table 16-19 (*Power-Management Timings*) t190 is incorrectly listed. It is changed to be 48uS (min) and 58 µs (max).

24. IDE Timing Correction

In Table 16-11 Ultra ATA Timing (Mode 3, Mode 4, Mode 5), t85 and t86 (for Mode 5) is changed from 3.3 ns to 6.0 ns.

25. Change to Control Bits for B-4 Stepping Specification Change

The name of the Specification Change “Control Bits for B-4 Stepping” is changed to “New Control Bits for ICH2.”

The sentence associated with this change is also changed to read: “New control bits have been added to the ICH2 Configuration Space for use with Intel® 845/850/860/870 chipsets.

This Specification Change applies to ICH2 B4, B5 and ICH2X C0 steppings.

26. USB Timing Table

Section 16.4, *AC Characteristics*, Table 16-12 is replaced with the following table.

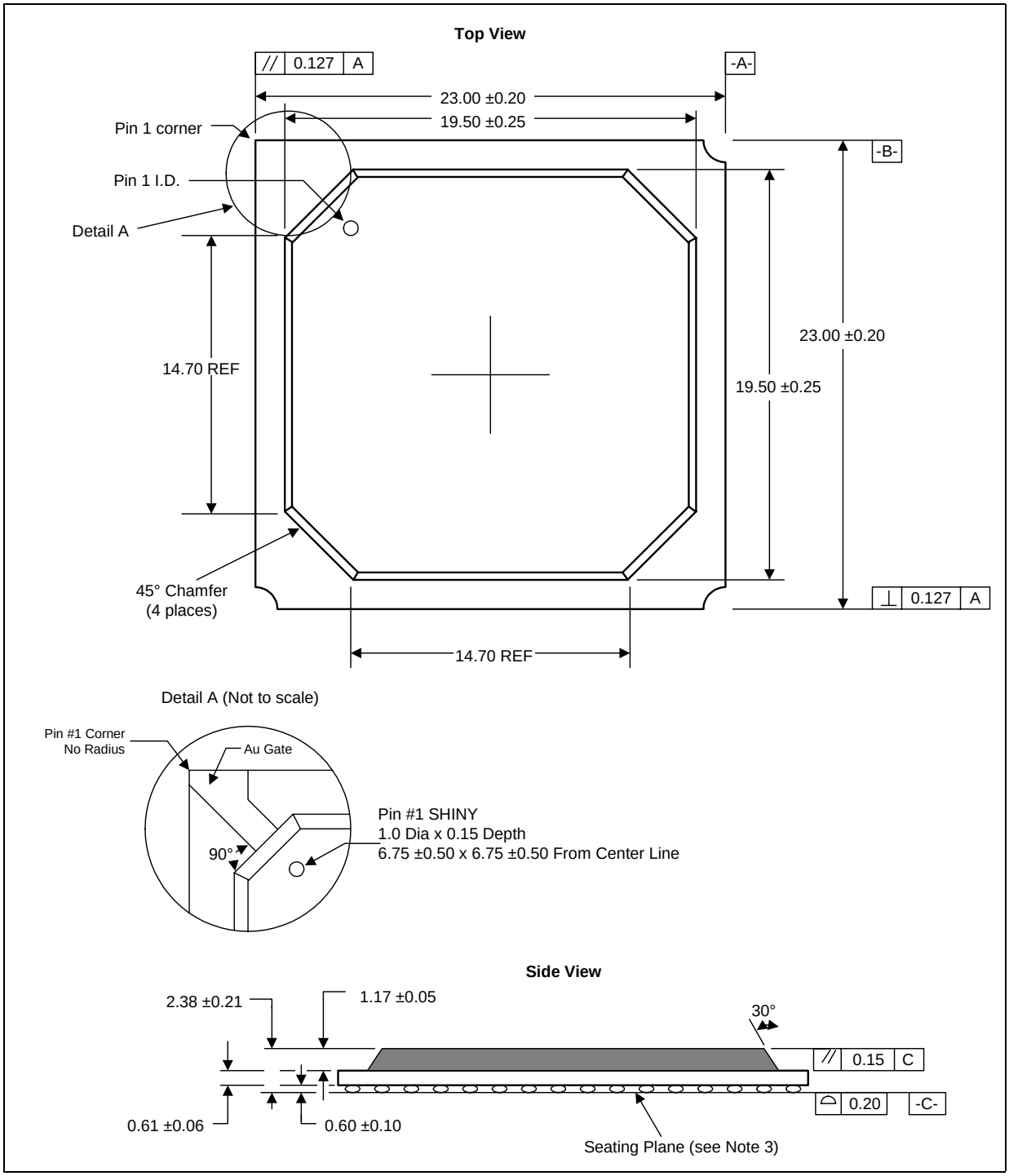
Sym	Parameter	Min	Max	Units	Notes	Fig
Full Speed Source (Note 7)						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	17-13
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	17-13
t102	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -3.5 -4	 3.5 4	 ns ns	2, 3	17-14
t103	Source SE0 interval of EOP	160	175	ns	4	17-15
t104	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns	5	
t105	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -18.5 -9	 18.5 9	 ns ns	3	17-14
t106	EOP Width: Must accept as EOP	82		ns	4	17-15
t107	Width of SE0 interval during differential transition		14	ns		
Low Speed Source (Note 8)						
t108	USBPx+, USBPx- Driver Rise Time	75	300	ns ns	1, 6 C_L = 50 pF C_L = 350 pF	17-13
t109	USBPx+, USBPx- Driver Fall Time	75	300	ns ns	1,6 C_L = 50 pF C_L = 350 pF	17-13
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -25 -14	 25 14	 ns ns	2, 3	17-14
t111	Source SE0 interval of EOP	1.25	1.50	µs	4	17-15
t112	Source Jitter for Differential Transition to SE0 Transition	-40	100	ns	5	
t113	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -152 -200	 152 200	 ns ns	3	17-14
t114	EOP Width: Must accept as EOP	670		ns	4	17-15
t115	Width of SE0 interval during differential transition		210	ns		

27. Change to Document Change #1

The last sentence of the second note associated with Document Change #1 and #20 is removed.

28. Change to Package Information

Figure 15-3 is replaced with the figure below.



NOTES:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M - 1982.
3. Primary Datum (-C-) and seating plane are defined by the sperical crowns of the solder balls.

29. Change to PM1_EN Power Well Attributes

Section 9.8.3.2 Describes the PM1_EN - Power Management 1 Enable Register. The attributes above the bit descriptions indicate that bit-10 (RTC_EN) is in the Resume Power Well when it is actually in the RTC Power Well, as the description for that bit correctly indicates. The Power Well attribute for PM1_EN is being changed to:

Power Well: Bits 0-7: Core, Bits 8-9, 11-15: Resume, Bits 10: RTC.

30. Arbiter Disable Correction

Section 9.8.3.8 describes the PM2_CNT - Power Management 2 Control register. The description for Arbiter Disable (ARB_DIS) is being change to:

Bit	Description
0	**Arbiter Disable (ARB_DIS)-R/W** 0 = Enable system arbiter. The arbiter can grant the bus to bus masters (internal devices or external PCI devices), other than the processor. 1 = Disable system arbiter (default). Processor has ownership of the system bus and memory. No bus masters (internal or external) are granted the bus. Note that after the arbiter is disabled, the processor must not initiate and down-bound reads to PCI devices that may have up-bound posted data, as this will result in system deadlock. Note: In general, software should not attempt any non-posted accesses during arbiter disable except to the ICH2's power management registers. This implies that interrupt handlers for any unmasked hardware interrupts and SMI/NMI should check ARB_DIS status before reading from ICH devices.

31. Correction to GST_TICK Accuracy

Section 9.8.1.1 is being corrected, specifically for bit-11 (GST_TICK) as indicated below.

Bit	Description
11	**ICH2 (82801BA):** Reserved **ICH2-M (82801BAAM):** **Global Standby Timer Tick Rate (GST_TICK)-R/W** 0 = Counts by 65.536 seconds (1.0921 minute). This yields a GST timeout range of 1 to 17.476. 1 = Counts by 2097.152 seconds (34.952 minutes). This yields a GST timeout range of 0.58 hours to 8 hours 45 minutes 22.816 seconds.

32. Table 3-4/SUS_STAT# Change

The SUS_STAT# row in Table 3-4 is changed as follows:

Signal Name	Power Plane	Reset Signal	During Reset	Immediately After Reset	C3 (ICH2-M)	S1	S3	S4/S5
SUS_STAT#	Resume I/O	RSMRST#	High	High		Low (ICH2-M) High (ICH2)	Low	Low

33. SUSCLK during RSMRST# Assertion

Table 3-4 incorrectly indicates that SUSCLK is “Running” during Reset. SUSCLK is low when RSMRST# is asserted, but will be “Running” when PCIRST# is deasserted.

34. TCO Corrections

Section 9.9.2 incorrectly lists TCO1_RLD as the register name for TCOBase+00h. This register is correctly named TCO_RLD - “TCO Timer Reload and Current Value Register”. This is an 8-bit register, thus the correct default value of this register is 00h.

Section 9.9.3 incorrectly lists TCO1_TMR as the register name for TCOBase+01h. This register is correctly named TCO_TMR - “TCO Timer Initial Value Register”. This is an 8-bit register, thus the correct default value of this register is 04h. The description of bits 5:0 incorrectly indicates that “Values of 0-3 are ignorred and should not be attempted”. Only values of 0-1 are actually ignorred.

Section 9.9.4 incorrectly lists TCO1_DAT_IN as the register name for TCOBase+02h. This register is correctly named TCO_DAT_IN - “TCO Data In Register”. This is an 8-bit register, thus the correct default value of this register is 00h. The last sentence of the description of this register is changed to: “Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register.”

Section 9.9.5 incorrectly lists TCO1_DAT_OUT as the register name for TCOBase+03h. This register is correctly named TCO_DAT_OUT - “TCO Data Out Register”. This is an 8-bit register, thus the correct default value is 00h.

35. EEPROM Programming Application Note

Section 5.2.4, *Serial EEPROM Interface*, refers to *Application Note AP-409, I/O Controller Hub EEPROM Map and Programming Information.* This reference is removed.Figure 2-1 (RTC Circuit) Correction

36. Figure 2-1 (RTC Circuit) Correction

The following note is added to Figure 2-1; Note: Diodes are Schottky.

37. PME Wake Doc Change

The following changes are made to Section 5.12.7.2, Table 5-42:

Note 1 is changed to “This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software or from a power failure.”

Note 2is added: “This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software.”

The note associated with GPI:[0:n] is changed from Note 1 to Note 2.

The following changes are made to Section 5.12.7.3:

The last sentence of the 4th paragraph is changed to read: “There are only four possible events that will wake the system after a power failure.”

Add a 4th item: PME: PME_STS, if enabled, will wake the system from S5 if S5 is entered from an AC power failure or if entered by a write to the SLP_TYP and SLP_EN registers.

The following changes are made to Section 9.8.3.9:

The 3rd sentence of the description for PME_STS is changed to: “If the PME_STS bit is set, and the system is in an S1-S4 state (or S5 state due to setting SLP_TYP and SLP_EN or due to a return from AC power failure), then the setting of the PME_STS will generate a wake event, and an SCI will be generated.”

The following changes are made to Section 9.8.3.10:

The 2nd sentence of the description for PME_EN is changed to: “PME# can be a wake event from the S1-S4 state or from S5 (if entered via SLP_EN or from AC power recovery, but not power button override).

38. APM I/O Decode Correction

The second sentence of Section 9.8.2 (APM I/O Decode) is changed to read “This register space cannot be moded (fixed I/O location).”

39. Memory Map Table Change

The last row of Table 6-4 of Section 6.4 (Memory Map) is changed as indicated:

Memory Range	Target	Dependency/Comments
All other	PCI	Any memory range access that makes it to the ICH2’s PCI bus and is not specified in one of the D31:F0;0xE0-0xEF registers or below 16MB will be master aborted.

40. SMBus Host Busy Correction

Section 12.2.1 HST_STS - Host Status Register is being corrected. Specifically, bit-0 Host_Busy is corrected to read as follows:

0 = Cleared by the ICH2 when the current transaction is completed.

1 = Indicates that the ICH2 is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE or LAST BYTE registers. The BLOCK DATA BYTE and LAST BYTE registers can be accessed when this bit is set only when the SMB_CMD bit in the Host Control register are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

41. PWRBTN_STS Note Addition

Section 9.9.3.1 PM1_STS - Power Management 1 Status Register is being corrected. Specifically, bit-8 Power Button Status will additionally contain the following note:

In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI if SCI_EN is not set) will be generated.

§