Intel 430HX PCIset Design Guide

June 1997

297467-002

TABLE OF CONTENTS

1

Overview

CHAPTER 1
OVERVIEW

1. Overview

Today's technology does not meet tomorrow's needs. With new applications such as multimedia, video conferencing, and on-line services; market requirements for the volume desktop computer will be higher performance, increased ease of use, and more features—all at a lower system price. The Intel 430HX PCIset (430HX) redefines the mainstream PC by providing new performance, features, and support for emerging technologies. 430HX architecture maximizes PCI performance which allows for new performance levels, optimized multimedia support, and Plug and Play (PnP) support. A design based on a Pentium® processor Flexible Motherboard reduces time to market and minimizes cost to support upgradability and flexibility.

The information provided in this design guide is based on a reference platform developed around the 430HX and the latest members of the Pentium processor family. Section 6.0 shows the schematics, jumper settings, component placement, and bill of materials.

A block diagram of the motherboard design is shown in Figure 1-1. A list of the motherboard design features is shown below.

- **CPUs Supported**
  - **— Pentium® Processors at iCOMP® Index 1308\166 MHz through iCOMP Index 610\75 MHz**
  - **— Future Pentium Overdrive® Processors**
  - **— Future High Performance Pentium Processors**
- **PCIset**
  - **— 82439HX System Controller (TXC)**
  - **— 82371SB PCI ISA/IDE Xcelerator (PIIX3)**
- **DRAM Main Memory**
  - **— 4 DRAM SIMM sockets for support for 4 MB to 256 MB at 60 ns or 70 ns (3V or 5V)**
  - **— EDO DRAM or Fast Page Mode DRAM**
- **L2 Cache SRAM**
  - **— 3.3V Pipelined Burst SRAMs**
  - **— Supports 512 KB of direct-mapped, writeback second level cache**
- **PCI ISA/IDE Xcelerator**
  - **— Integrated fast IDE interface**
  - **— Support for up to four devices**
  - **— PIO Mode 4 transfers up to 16 MB/s**
  - **— Integrated 8x32 bit buffer for PCI IDE bus master burst transfers**
- **USB Ready**
- **Slots**
  - **— 4 PCI**
  - **— 3 ISA**
- **3.3V Clock Driver**
- **Form Factor**
  - **— 2/3 Baby AT**
- **Number of Board Layers**
  - **— 4 (2 signal layers)**
- **Socket 7**
- **Flash Device**
  - **— 1 Mbit Flash implementation**
  - **— Provides upgrade to 2 Mbit Flash**

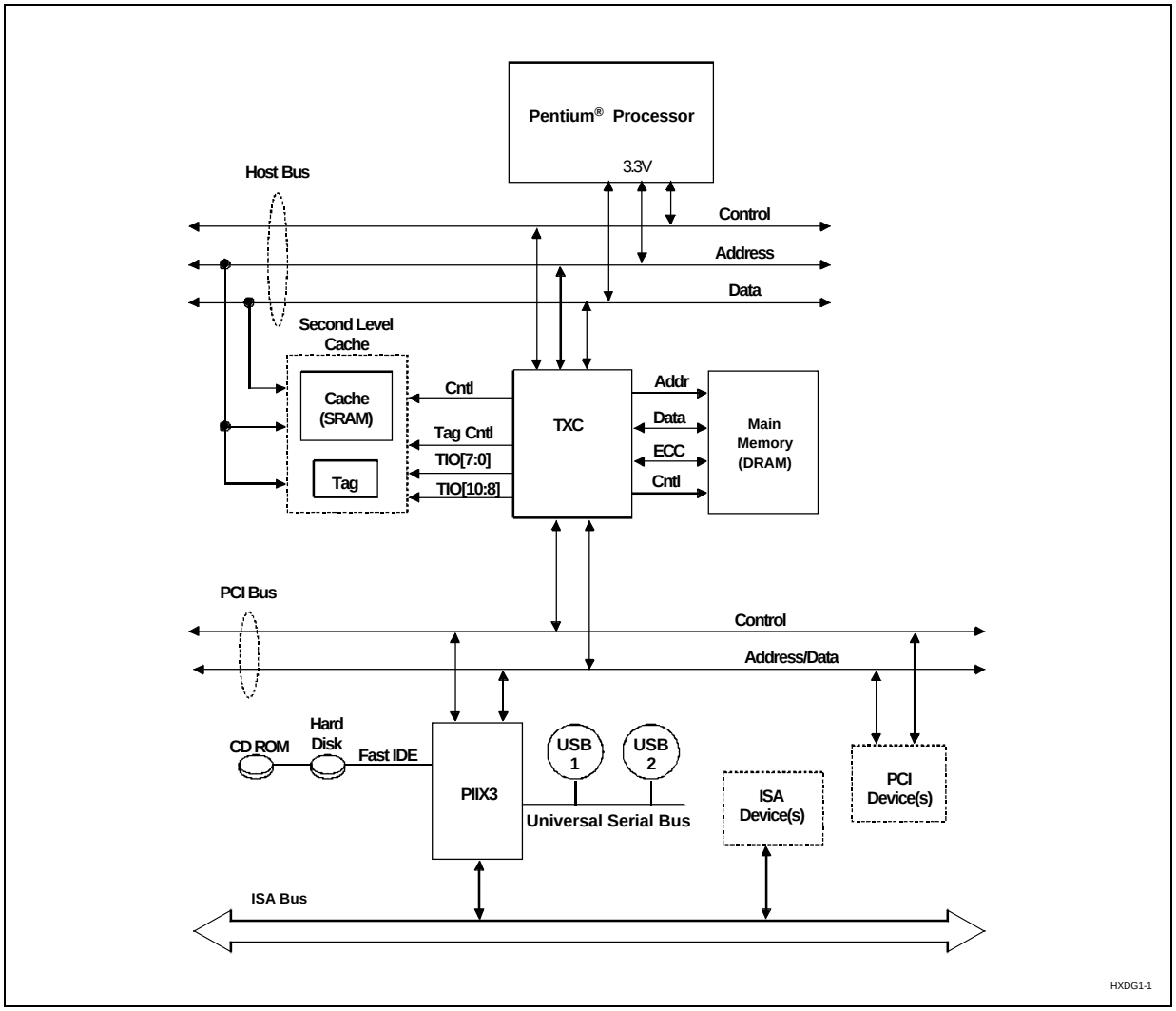


Figure 1-1. Intel 430HX PCIset System Block Diagram

1.1 Intel 430HX PCIset

The 430HX (Figure 1-1) consists of the 82439HX System Controller (TXC) and the 82371SB PCI I/O IDE Xcelerator (PIIX3). The TXC forms a Host-to-PCI bridge. The PIIX3 is a multi-function PCI device providing a PCI-to-ISA bridge, a fast IDE interface, an APIC interface, and a host/hub controller for the Universal Serial Bus (USB). The PIIX3 also provides power management.

The TXC interfaces are designed for 3V and 5V busses. The 430HX connects directly to the Pentium processor 3V host bus; The 430HX connects directly to 5V or 3V main memory DRAMs; and the TXC connects directly to the 5V PCI Bus. The TXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus.

Data Flow

Processor cycles are sent directly to the second level cache with control for the second level cache provided by the TXC. All other processor cycles are sent to their destination (DRAM, PCI or internal TXC configuration space) via the TXC. PCI Master cycles are sent to main memory through the TXC. The TXC performs snoop or inquire cycles using the host bus.

DRAM Interface

The DRAM interface is a 64/72-bit data path that supports both standard page mode and Extended Data Out (EDO) memory. The DRAM interface supports 4 Mbytes to 512 Mbytes with eight RAS lines and also supports symmetrical and asymmetrical addressing for 1M-, 2M-, and 4M-deep SIMMs and symmetrical addressing for 16 MByte-deep SIMMs.

Second Level Cache

The TXC supports a write-back cache policy providing all necessary snoop functions and inquire cycles. The second level cache is direct mapped and supports both a 256-Kbyte or 512-Kbyte SRAM configuration using pipelined burst SRAMs. The burst 256-Kbyte configuration performance is 3-1-1-1 for read/write cycles; pipelined back-to-back reads can maintain a 3-1-1-1-1-1-1-1 transfer rate. An optional mode extends the DRAM L2 cacheability range to 512 Mbytes.

PCI Interface

The TXC is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX3 bus master requests. The TXC provides the interface between PCI and main memory.

The PIIX3 incorporates a fully PCI Bus compatible master and slave interface. As a PCI master, the PIIX3 runs cycles on behalf of DMA, ISA masters, or a bus master IDE. As a PCI slave, the PIIX3 accepts cycles initiated by PCI masters targeted for the PIIX3's internal register set or the ISA bus. The PIIX3 directly supports the PCI interface running at either 25 MHz, 30 MHz, or 33 MHz.

Datapath and Buffers

The TXC datapath is optimized for minimum latency and maximum throughput operation from both the CPU and PCI masters. The TXC contains two physical sets of buffers for optimizing data flow. A six Dword buffer is provided for CPU-to-PCI writes that helps maximize the graphic writes to PCI bandwidth. An 8-Qword deep merging memory buffer is provided that is used for CPU-to-main memory writes, writeback cycles (posted at 3111), PCI-to-main memory write posting, and PCI-from-main memory read prefetching.

Error Detection and Correction

Parity or error correction are software configurable options (parity is the default). The ECC mode provides single-error correction, double-error detection, and detection of all errors confined to a single nibble for the DRAM memory subsystem.

ISA Interface

PIIX3 incorporates a fully ISA Bus compatible master and slave interface. PIIX3 directly drives five ISA slots without external data buffers. External transceivers are used on the SA[19:8] and SBHE# signals to permit these signals to be used with the IDE interface. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation, and SYSCLK generation.

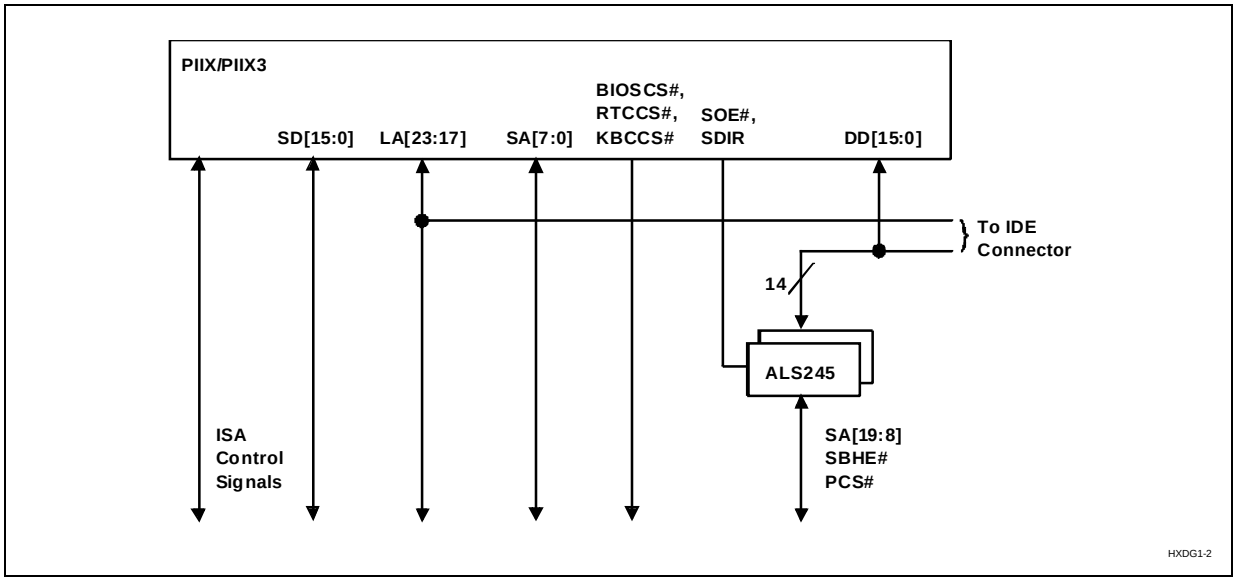


Figure 1-2. ISA Interface

DMA Interface

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Channels 0-3 and Channels 5-7). DMA Channel 4 is used to cascade the two controllers and defaults to cascade mode in the DMA Channel Mode (DCM) Register.

Each DMA channel is hardwired to the compatible settings for DMA device size; channels [3:0] are hardwired to 8-bit count-by-bytes transfers and channels [7:5] are hardwired to 16-bit count-by-words (address shifted) transfers. The PIIX3 provides the timing control and data size translation necessary for the DMA transfer between the memory (ISA or main memory) and the ISA Bus device. ISA Compatible and type F DMA timings are supported. PIIX3 provides 24-bit addressing in compliance with the ISA-Compatible specification.

PIIX3 integrates a high performance interface from PCI to IDE. This interface is capable of accelerated PIO data transfers as well as acting as a PCI Bus master on behalf of an IDE DMA slave device. PIIX3 provides an interface for both primary and secondary IDE connectors.

Universal Serial Bus

PIIX3 contains a USB Host Controller (HC). The Host Controller includes the root hub with two USB ports. This permits connection of two USB peripheral devices directly to the PIIX3 without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The USB's PCI configuration registers are located in function 2, PCI configuration space. The PIIX3 Host Controller completely supports the standard Universal Host Controller Interface (UHCI) and thus, takes advantage of the standard software drivers written to be compatible with UHCI.

Interval Timer

PIIX3 contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one PIIX3 timer unit, referred to as Timer-1. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker. The 14.31818 MHz counters normally use OSC as a clock source.

Interrupt Controller

PIIX3 provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 13 external and three internal interrupts are possible. The master interrupt controller provides IRQ[7:0] and the slave interrupt controller provides IRQ [15:8]. The three internal interrupts are used for internal functions only and are not available to the user. IRQ2 is used to cascade the two controllers together. IRQ0 is used as a system timer interrupt and is tied to Interval Timer 1, Counter 0. IRQ13 is connected internally to FERR#. The remaining 13 interrupt lines (IRQ[15,14,12:3,1]) are available for external system interrupts. Edge or level sense selection is programmable on an individual channel by channel basis.

The Interrupt unit also supports interrupt steering. PIIX3 can be programmed to allow the four PCI active low interrupts (PIRQ[D:A]#) to be internally routed to one of 11 interrupts (IRQ[15,14,12:9,7:3]).
In addition, the motherboard interrupt (MIRQ0) may be routed to any of the 11 interrupts.

Stand-Alone I/O APIC Support

The PIIX3 supports a stand-alone I/O APIC device on the ISA X-Bus. PIIX3 provides a chip select signal (APICCS#) for the I/O APIC. It also provides handshake signals to maintain buffer coherency in the I/O APIC environment.

X-Bus Peripheral Support

PIIX3 provides positive decode (chip selects) and X-Bus buffer control (XDIR# and XOE#) for a real time clock, keyboard controller and BIOS for PCI and ISA initiated cycles. PIIX3 also generates RTCALE (address latch enable) for the RTC. The chip selects are generated combinatorially from the ISA SA(16:0) and LA(23:17) address lines (Note that it is assumed that ISA masters drive SA(19:16) and LA(23:17) low when accessing I/O devices). PIIX3 also provides PS/2 mouse support via the IRQ12/M signal and coprocessor functions (FERR# and IGNNE#). Software can enable or disable the chip selects and X-Bus buffer control lines.

Coprocessor Error Function

This function provides coprocessor error support for the CPU. FERR# is tied directly to the coprocessor error signal of the CPU. If FERR# is driven active to the PIIX3, an internal IRQ13 is generated and the INTR output from the PIIX3 is driven active. When a write to I/O location F0h is detected, PIIX3 negates IRQ13 (internal to the PIIX) and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. Note that IGNNE# is not driven active unless FERR# is active.

Mouse Function

When the mouse interrupt function is enabled, the mouse interrupt function is provided on the IRQ12/M input signal. In this mode, a mouse interrupt generates an interrupt through IRQ12 to the Host CPU. PIIX3 informs the CPU of this interrupt via an INTR.

Power Management

PIIX3 has extensive power management capability permitting a system to operate in a low power state without being powered down. In a typical desktop personal computer there are two states—Power On and Power-Off. Leaving a system powered on when not in use wastes power. PIIX3 provides a Fast On/Off feature that creates a third state called Fast Off. When in the Fast Off state, the system consumes less power than the Power-On state.

The PIIX3's power management architecture is based on three functions—System Management Mode (SMM), Clock Control, and Advanced Power Management (APM). Software (called SMM code) controls the transitions between the Power On state and the Fast Off state. PIIX3 invokes this software by generating an SMI to the CPU (asserting the SMI# signal). A variety of programmable events are provided that can generate an SMI. The SMM code places the system in either the Power On state or the Fast Off state.

1.1.1 82439HX TXC Features

- Supports the Pentium® processor host bus at 66 MHz, 60 MHz, and 50 MHz at 3V
- Dual Processor Support
- PCI 2.1 Compliant
- Integrated Second Level Cache Controller
  - — Direct Mapped Organization
  - — Write-Back Cache Policy
  - — Cacheless, 256 Kbytes, and 512 Kbytes
  - — Pipelined Burst SRAMs
  - — Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - — Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1
  - — Integrated Tag/Valid Status Bits for Cost Savings and Performance
  - — Optional 512 MB DRAM Cacheability Limit
  - — Supports 5V SRAMs for Tag Address
- Integrated DRAM controller
  - — 4 Mbytes to 512 Mbytes Main Memory
  - — 64 Mbit DRAM Technology Support
  - — 8-Qword Deep Merging DRAM Write Buffer
  - — Enhanced EDO/Hyper Page Mode DRAM Supports 4-2-2-2 Reads and x-2-2-2 Writes @ 60 MHz, 5-2-2-2 Reads and x-2-2-2 Writes @ 66 MHz
  - — 8 RAS Lines Available
  - — Integrated Programmable-Strength MA Buffers
  - — CAS-Before-RAS Refresh
- Optional Parity
- Optional Error Checking and Correction (ECC)
  - — Superior DRAM Data Integrity
  - — Single Bit Error Correction, Multi-Bit Error Detection plus Nibble Failure Detection ECC Code
  - — Single and Multi-bit Error Reporting
  - — Virtual Swapable Bank Support (i.e., can swap out problem banks)
  - — Merging Write Buffer Eliminates Most Partial Writes Cycles
- Fully Synchronous, Minimum Latency 25/30/33 MHz PCI Bus Interface
  - — Zero Wait State CPU-to-PCI Write Timings (no IRDY stall) for Superior Graphics Performance
  - — Enhanced CPU-to-PCI Read Latencies for Superior Graphics/PIO Performance
  - — 21 DWORD PCI-DRAM Post Buffer
  - — 22 DWORD PCI-to-DRAM Read Prefetch Buffer
  - — Writeback Merging for PCI to DRAM Writes
  - — Writeback Forwarding for PCI to DRAM Reads
  - — Pipelined Snoop Ahead
  - — Multi-Transaction Timer to Support Multiple Short PCI Transactions Within the Same PCI Arbitration Cycle
- Supports the Universal Serial Bus (USB)
- Single 324-Pin BGA Package
- Supported Kits
  - — 82430HX PCIset ISA Kit (TXC, PIIX3)
  - — 82430HX PCIset ISA/DP Kit (TXC, PIIX3, IOAPIC)

The 430HX consists of the 82439HX System Controller (TXC) and the PCI ISA IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. The TXC provides a 64/72 bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM Error detection/correction or parity. The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

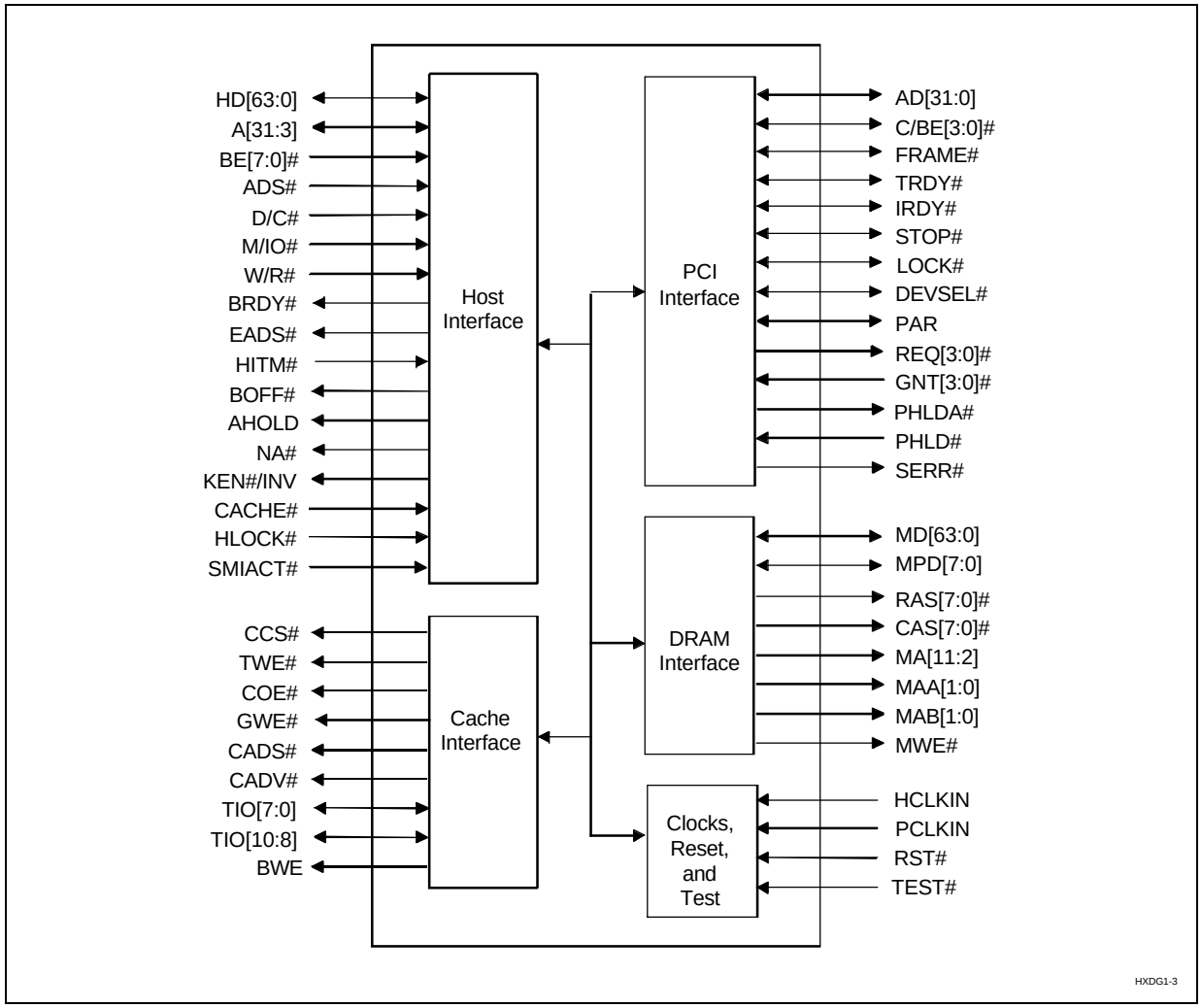


Figure 1-3. TXC Simplified Block Diagram

1.1.2 82371SB PIIX3 Features

- **Bridge Between the PCI Bus and ISA Bus**
- **Universal Serial Bus (USB) Host Controller**
  - **— Compatible With Universal Host Controller Interface (UHCI)**
  - **— Contains Root Hub With Two USB Ports**
- **PCI Specification Revision 2.1 Compliant**
- **PCI and ISA Master/Slave Interface**
  - **— PCI from 25–33 MHz**
  - **— ISA from 7.5–8.33 MHz**
  - **— Five ISA Slots**
- **Fast IDE Interface**
  - **— Supports PIO and Bus Master IDE**
  - **— Supports up to Mode 4 Timings**
  - **— Transfer Rates to 22 Mbytes/Sec**
  - **— Separate Master/Slave IDE Mode Support**
- **Plug-n-Play Port for Motherboard Devices**
  - **— 1 Steerable Interrupt Line**
  - **— 1 Programmable Chip Select**
- **Steerable PCI Interrupts for PCI Device Plug-n-Play**
- **Functionality of One 82C54 Timer**
  - **— System Timer; Refresh Request; Speaker Tone Output**
- **Two 82C59 Interrupt Controller Functions**
  - **— 14 Interrupts Supported**
  - **— Independently Programmable for Edge/Level Sensitivity**
- **Enhanced DMA Functions**
  - **— Two 8237 DMA Controllers**
  - **— Fast Type F DMA**
  - **— Compatible DMA Transfers**
  - **— Seven Independently Programmable Channels**
- **X-Bus Peripheral Support**
  - **— Chip Select Decode**
  - **— Controls Lower X-Bus Data Byte Transceiver**
- **I/O Advanced Programmable Interrupt Controller (IO APIC) Support**
- **System Power Management (Intel SMM Support)**
  - **— Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#**
  - **— Programmable CPU Clock Control (STPCLK#)**
  - **— Fast On/Off Mode**
- **Non-Maskable Interrupts (NMI)**
  - **— PCI System Error Reporting**
- **NAND Tree for Board-Level ATE Testing**
- **208-Pin QFP**

The 82371SB PCI I/O IDE Xcelerator (PIIX3) is a multi-function PCI device implementing a PCI-to-ISA bridge function and a PCI IDE function. In addition, the PIIX3 implements a Universal Serial Bus host/hub function. As a PCI-to-ISA bridge, the PIIX3 integrates many common I/O functions found in ISA-based PC systems—a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and power management support. In addition to compatible transfers, each DMA channel supports type F transfers. Chip select decoding is provided for BIOS, real time clock, and keyboard controller. Edge/Level interrupts and interrupt steering are supported for PCI plug-and-play compatibility. The PIIX3 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The PIIX3 provides motherboard plug-and-play compatibility. The PIIX3 implements one steerable interrupt line and a programmable chip select. The interrupt line can be routed to any of the available ISA interrupts. The PIIX3 also provides support for an external I/O APIC.

The PIIX3 contains a Universal Serial Bus (USB) Host Controller that is UHCI compatible. The Host Controller moves data between system memory and devices on USB by processing data structures set up by the Host Controller Driver (HCD) software and generating the transaction on USB. Optimized partitioning between software and hardware operations maximizes performance and maintains flexibility. The Host Controller's PCI Bus master capability permits high performance data transfers to system memory. The Host Controller's root hub has two programmable USB ports.

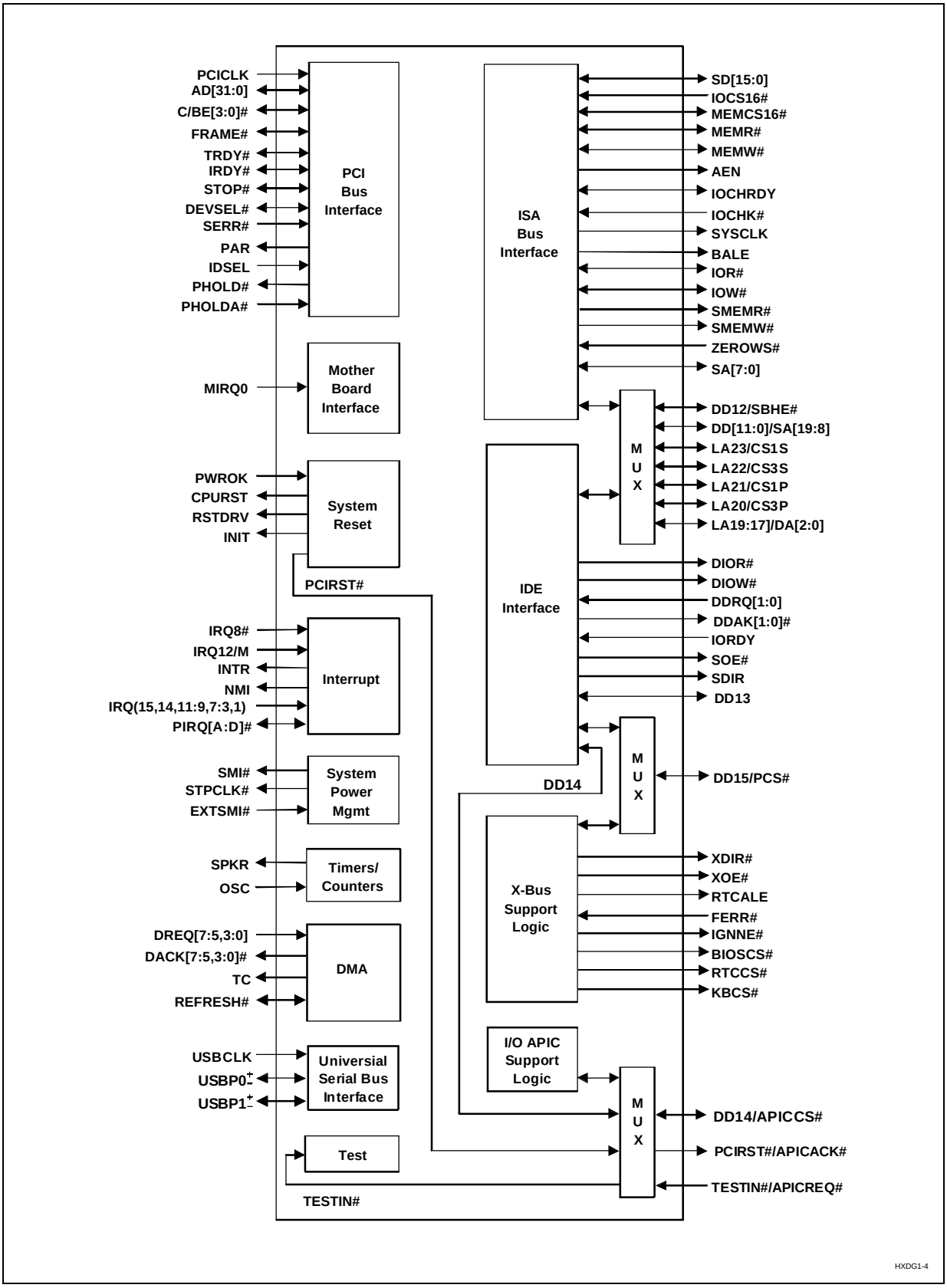


Figure 1-4. PIIX3 Simplified Block Diagram

2

Flexible Motherboard Design Layout Review Checklist

CHAPTER 2
FLEXIBLE MOTHERBOARD DESIGN LAYOUT REVIEW CHECKLIST

2. Flexible Motherboard Design Layout Review Checklist

The following checklist is a guide when designing or reviewing a board design that uses the Intel 430HXPCIset (430HX).

2.1 TXC Voltage

- Diode Protection—From the 5V reference pin (E14) connect a 100Ω resistor to the 5V power supply, and to the same 5V reference pin (E14), connect a 1.0 uF cap to ground for protection of the TXC's internal circuitry.

2.2 CPU

- Refer to the "P55C/FMB Design Review Checklist" and "Socket 7 Specification" for additional information on CPU related requirements. The P55C/FMB Design Review Checklist is available on Lotus Notes.
- Drive Strength—The CPU sets its output buffer drive strength using the BRDYC# & BUSCHK# signals which are sampled at RESET. Typically in a UP-430HX system, a low drive setting is used (only verified by proper simulation). BRDYC# has an internal pullup that will default to a low drive buffer strength. BRDYC# and BUSCHK# may be left as no connects in a UP-430HX configuration. Depending on layout and loading, the medium strength buffers may be required for DP applications and in this case, you would want to BRDYC#=0 & BUSCHK#=1.
- Frequency Selection—BF[1:0], X34 & Y33, should be supported (jumpers are flexible) to allow support of different speeds of Pentium® Processor. BF[1:0] should be connected to two 3-pin jumpers which allow strapping of the BF[1:0] pins to either VCC3 or VSS. These pins should be pulled low with 100Ω (or less) resistors. Also, it is recommended that a 100Ω (or less) resistor also be used to pullup the BF0 line to support future Pentium processor speed upgrades such as P55C.
- Host Parity—The HDP[7:0] signals are not supported by 430HX and should be pulled up to 3.3V through 4.7 kΩ resistors.
- If open collector drivers are used to generate INIT and A20M#, pull up to 3.3V (330Ω for INIT, 4.7 kΩ for A20M#).
- VCC2DET (P55C)—This signal can be used as a safeguard to prevent plugging in a P54C into a Socket set up for P55C support (2.5 Vcore), provided extra sense logic is incorporated. The P55C will always drive VCC2DET low. This pin can be used in a flexible motherboard implementation to correctly set the voltage regulator to drive the correct VCC to the CPU.
- ADSC# should be used to drive the cache subsystem, and ADS# should be used to drive the chipset. These signals are functionally identical to each other and two copies are provided by the processor for loading reasons.

- INV and KEN# should be tied together at the CPU. The 430HX muxes these signals. KEN# is used during CPU read cycles and INV is used during L1 snoop cycles.
- Voltage—VRE to the socket allows the most flexibility to support the greatest number of processor types. To date the highest current requirement is about 4.25 amps for the P54CS-166 and 5 amps for the P54CTB-200 OverDrive processor.
- P55C Voltage—The core runs off 2.5V±5% @ ~4A and the I/O portion is STDE @ ~ 0.4A.
- V_{CC} and HCLK—The PP power up specifications recommend that HCLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. Following this recommendation will ensure the long term reliability of the processor.
- Decoupling—An appropriate quantity and quality of bypass decoupling capacitors are necessary for proper CPU operation. Proper conditioning of the voltage supplies to the CPU(s) will assure operation under worst case conditions. See the Socket 7 Specification for guidelines for proper decoupling. Double check fordecoupling capacitors between V_{CC} Core and V_{CC} I/O.
- Unlike the Pentium Processor (735/90,815/100,1000/120, and 1110/133), the following inputs on the P55C are not 5 volts tolerant: (CLK, PICCLK, AHOLD, BRDYC#, EADS#, KEN, WB/WT#, INV, NA#, EWBE#, BOFF#).

2.3 Host Interface

- Pullups[1]—FRCMC#, FLUSH#, WB/WT#, AP, PEN# & TEST#—through 8.2Ωk
- The HOLD and EWBE# pins on the processor are tied directly to GND.
- No Connects—R/S#, TCK, TDI, TMS, TRST#, APCHK#, BP[3:0], HIT#, HLDA, IERR#, PCHK#, PRDY, PWT, PCD, SCYC, TDO, and CPUTYP.
- Split Core V_{CC}2 for P55C—The P55C requires two supply voltages; 2.5V±5% on its Vcore pins at about 3.0 Amps (166 MHz) required. Its external I/O pins operate at STDE (3.125-3.6V) levels and require 0.4A@166 MHz. These current requirements double for DP designs. Check the latest POR for confirmation. When shorting these planes together (P54C operation for example), please use at least 5-6 jumpers.
- A27 Strapping option—The state of A27 at reset rising determines DRAM refresh rate (the default is 66 MHz). The state is sampled and stored in DRAMC (57h) [0]. This signal has a weak pulldown and could be pulled up to allow for a host bus frequency detection of 60 MHz . It could be left as a no connect for a host bus frequency of 66 MHz. BIOS can use this bit to determine the system frequency.
- Dual CPU signals—The following list of signals should be connected between the two processors to support DP. In a UP design these signals are left as NCs. PICCLK, PICD0, PICD1, PHITM#, PHIT#, PBGNT#, SCYC.

2.4 L2 Cache

- GWE#—430HX only supports PBSRAMs that use GWE# (pin 88 on 100 pin TQFP). GWE# must be connected from the TXC to each of thePBSRAMs. AsynchronousSRAMs are not supported.
- Proper Speed Parts—Intel recommends the use of PBSRAMS with tco of 8.5 nS and cycle times of 15 nS for operation at 66 MHz host bus frequencies.

---

[1] Pullup to V_{CC}3=3.3V unless otherwise noted

- Host Bus Parity—Some PBSRAMs have 4 signals that are for host bus parity support. 430HX does not support host bus parity so these signals are not used.
- Cache Info—Host addresses, A[31:28], are sampled by the TXC at the rising edge of RESET to determine the size and type of L2 cache installed. The contents of the CC register reflect the state at RESET and can be overwritten by BIOS.
- TIO[10]—The state at reset determines the Extended Cacheability Mode (64M or 512M cacheable). Pull down through 10 kΩ to support 512M mode or pullup with 100K for standard 64M mode. This signal should also be pulled high when supporting a DRAM cache. If 512M is selected, then TIO[9:8] must not be pulled up or down.
- 512K support—A18 determines which bank is accessed. This address is connected to CE2 on the PBSRAMs of the lower bank and CE2# of the upper bank PBSRAMs (watch loading).
- 512M Cacheability—11 tag bits are required to cache 512 Mbytes of main memory.
- Coast Modules—If a COAST module is used, all recommendations and specifications contained in the "Flexible Cache Solution For the 430FX/HX/VX PCIsets (Rev 3.0) should be followed. Simulation of the critical CPU/TXC/Coast interfaces is highly recommended to guarantee proper operation when supporting a cache module.
- DRAM cache support—The 430HX reference schematics show the proper connection for supporting DRAM cache for both on board and COAST implementations.

2.5 DRAM

- DRAM support—The TXC supports 12x11, 12x10, 11x10, and 10x9 asymmetrical DRAMs.
- MA[11:2] Buffering—External buffering of the MA[11:2], MAA/B[1:0] and MWE# signals are necessary when more than 4 SIMM slots are supported.
- MAx[1:0]—These signals (MAB[1:0] are identical copy of MAA[1:0] and can be directly connected to up to 4 SIMM sockets and still maintain a x-222 EDO burst performance when programmed for 12 mA buffer strength. If more than 4 SIMMs are supported, we recommend that external buffers be used on the MAx[1:0], MA[11:2] and MWE#.
- ECC or Parity—430HX is able to support memory parity or ECC when using x72 bit memory devices.
- MWE#—Programmable for 8 or 12 mA to allow direct drive of 4 SIMM slots when in the 12 mA mode. If more than 4 slots are supported, program for 8 mA and externally buffer MWE# for each SIMM pair.
- RAS[7:0]#—Series terminating resistors (22Ω) on RAS[0:7]# are required. Note that all the RAS lines may not be used if less than 8 SIMMs are used.
- CAS[7:0]#—Series terminating resistors (10–22Ω) are recommended on CAS[0:7]#.

2.6 PCI

- Pull-up (to 5V) resistors (2.7 kΩ) on PIRQ[A:D]#, REQ[0:3]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, and pins A60/B60 (REQ64#/ACK64#) on PCI connectors.
- PCI slots—430HX supports up to 4 PCI masters with its REQ[3:0]#/GNT[3:0]# pairs.
- Pull-up resistors to $V_{CC}3$ are required on GNT[0:3]# and PHLDA# since these are outputs of the 3V TXC.
- A pull-down resistor of ~5kΩ, or stronger, needs to be connected to the PCI JTAG signal TRST#.

2.7 ISA Bridge (PIIX3)

- Pullups[2]—PHOLD#—10K; APICCS# & PCS# between 1.0 & 4.7k, these should be on the output of the 74ALS245 when demuxing APICCS# & PCS# from DD[15:14]. No pullups on DD[15:0] are needed for IDE header.
- Pullups (pullup to 3.3V)—CPURST—330; SMI#, STPCLK#, INTR#, NMI, and IGNNE# (all 4.7k).
- Pulldowns—DDRQ[1:0]—5.6K; MDRQ[1:0]—5.6k.
- SYSCLK strapping—The state of SYSCLK is sampled on the assertion of PWROK which allows for the proper SYSCLK divisor (either divide by 3 or divide by 4). In order for the PIIX3 to properly detect a high during reset (divide by 3) or detect a low during reset (divide by 4), a jumper option connected to PWROK followed by an open collector 74F07 with pullup resistors must be used. Please refer to the 430HX ISA customer reference schematics (0.4 or later).
- TESTIN#—The Test Pin functions as the APICREQ# in DP mode, and also requires an external 4.7KΩ pull-up resistor to V_{CC}s.
- SD/XD transceiver "A" side buffers point towards the ISA bus and "B" side buffers point towards the X-Bus.
- MASTER#—The PIIX3 doesn't require connection with the MASTER# signal from the ISA bus (same as the PIIX). Place a pull-up resistor (300Ω) on the MASTER# signal from the ISA connectors.
- ISA Slots—The PIIX3 will support up to 5 ISA slots.
- USB signals P0+, P0-, P1+, P1- require a 15 kΩ pulldown resistor on PIIX3 outputs.
- V_{CC}/V_{CC}3 pin: Pin 130 provides the 3V interface for the USB. Tie to 3V. Also, place a .1 µF cap on this pin to gnd.
- USB Clock—48 MHz or 24 MHz with a duty cycle of better than 45/55% (24 MHz) or 40/60% (48 MHz) should be fed into the PIIX3's USB clock input, pin 146.
- The 30Ω series termination resistors on the USBPx lines must be placed as close to the USB connector as possible.
- The 47 pF caps to ground on the USBPx lines must be placed on the PIIX3 side of the (30Ω) series termination resistors.
- Ferrite beads and by-pass caps on power and ground are recommended for EMI purposes.

2.8 IDE Interface

- Refer to the "82430HX PCIset Layout Guidelines" when implementing the IDE interface.
- Pull-up resistor on IORDY# (1 kΩ).
- Primary IDE connector uses IRQ14 and the secondary IDE connector uses MIRQ0.
- All signals running to the two IDE connectors (except for IORDY#) have series terminating resistors (22-47Ω). See 430HX PCIset Layout Guidelines.
- DD[0:15] and SA transceivers should be hooked up correctly—DDs on the "A" side and SAs on the "B" side of a '245.

---

[2] Pullup to V_{CC}=5.0V unless otherwise noted

- Layout—Proper operation of the IDE circuit depends on the total length of the IDE bus. Follow the recommendations in our IDE Guidelines App Note carefully. The total signal length from the IDE drivers to the end of the IDE cables should not exceed “18”. Therefore the PIIX3 and buffers should be located as close as possible to the IDE headers to allow the IDE cable to be as long as possible. Make sure that pin 30 of the primary and secondary IDE connector is connected to ground.

2.9 IOAPIC (DP)

- Voltage—This is a 5V device. The Vdd pin referenced in the EDS Rev. 1.0 page 9 has been eliminated. Pins 19,51,&64 are 5.0V and grounds are pins 1,33,&52.
- CLK—May be 3 or 5V but is typically connected to the PCI clocks that are 5V.
- DD14/APICCS#—The mux’ed IOAPIC chip select signal requires a pullup resistor on the output of the 74ALS245 because its output is sometimes floated. This signal is internally driven high during
  a hard reset.
- APICACK2# (pin 8)—This is not used in 430HX applications and may be left NC.
- RSTDRV—This pin changes definition depending on whether the IOAPIC function is enabled.
- SMI support—The option to route SMI through the IOAPIC is recommended depending on the OS intended for use on the platform.

2.10 Clocks

- 3V CPU clocks—The CLK input on the P54 family is 5V tolerant. The P55C’s is not 5V tolerant.
- TXC-CPU Skew—The maximum clock skew allowable between the TXC and the CPU is 300 pS. Therefore we recommend that both devices should be driven using the same clock synthesizer output through 2 parallel 10Ω resistors (series dampening). Simulating this net is highly recommended. The “Short Stub route, 2 unbalanced loads or large distances, Split at driver” topology identified in Figure 4-5 is strongly suggested.
- Clock Skews—The clock skew between any two HCLK loads must be less than 1.0 nS (follow layout recommendations or simulate). The skew between PCLKs must be less than 2.0 nS. The difference between rising edges of HCLK and PCLK must be between 2.0 and 6.0 nS.
- Clock device—Clock synthesizer vendors are beginning to offer devices with 48 MHz outputs for use with USB controllers. Older devices had 24 & 12 MHz outputs.
- L2 Clocks—Each set of PBSRAMs should be driven with their own copy of HCLK through a 10Ω series dampening resistor.
- USB Clock—48 MHz or 24 MHz with a duty cycle of better than 45/55% (24 MHz) or 40/60% (48 MHz) should be fed into the PIIX3’s USB clock input, pin 146.
- DP APIC CLK—If used for DP applications, a maximum 16 MHz clock is recommended.

2.11 Dual CPUs

- The reset signals to each of the CPUs must be synchronous to the HCLK when supporting DP designs.
- CPUTYP#—Primary CPU pulled down and the secondary pulled up.
- APICD1—At reset, the state of this signal determines if the processor takes a primary function or secondary.

- DPEN#—At reset, the state of this signal determines if the CPU's internal local APIC is enabled or not.

2.12 Flash

- Intel 2M Boot Block—Many designers are finding it difficult to keep the amount of BIOS code small enough to fit into a 1M Flash. It is highly recommended that support for an optional 2M Boot Block Flash is designed in if planning to use a 1M device (each size comes in a different package type). By simply laying out 2 pad sets, one for the 1M and another for a 2M, the board will allow use of a 2M Flash if the BIOS becomes too large for a 1M sometime in the near future.
- Support for Intel Flash devices using ATD (>=2 MBB)—The BIOSCS# directly to the Flash will not work properly due to the way the PIIX3 sometimes floats the address bus (the PIIX and PIIX3 devices multiplex some of the DD and SA lines whereas the SIO and ESC south bridge components do not). To use the Intel 2M Flash device with the PIIX3 component, BIOSCS# must be OR'd with XOE# and then driven to the CE# input of the Flash device.

2.13 ECC & Parity support

- Parity—Parity is supported when using 72 bit DRAM SIMMs.
- ECC—ECC can be supported with the use of 72 bit DRAM SIMMs.

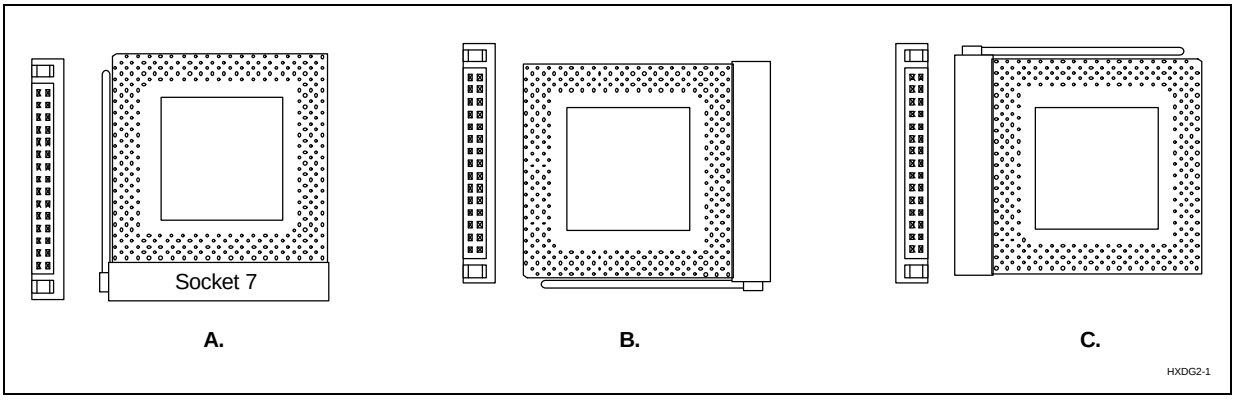
2.14 Layout

- Refer to the 430HX Layout Recommendations document for the clock and general board layout recommendations.

2.15 Header 7/VRM

- Placement: ❑ Header 7 within 1" of CPU $V_{CC}2$ pins (may be further but may experience excessive resistance in power plane).
- The physical space requirements of Voltage Regulator Module 7 have been met.
  - ❑ 1.48" total space for VRM/Header 7 from motherboard.
  - ❑ 0.5" maximum component space on front of VRM PCB (heatsink side).
  - ❑ 0.238" maximum component space on back of VRM PCB (component side).
  - ❑ 2.6" maximum VRM PCB width.
- SENSE: ❑ Routed to a CPU $V_{CC}2$ pin or the center of the CPU core voltage island.

- Circle letter noting orientation of header and CPU socket in figure below.



2.16 Miscellaneous

- It is highly recommended that the PWRGOOD signal from the power supply **not** be connected directly to logic on the board, without first going through a Schmitt trigger type circuitry to square-off and maintain the signal integrity or PWROK. Refer to the 430HX reference schematics.

3

430HX Board Layout and Routing Guidelines

CHAPTER 3
430HX BOARD LAYOUT AND ROUTING GUIDELINES

3. 430HX Board Layout and Routing Guidelines

This section describes layout and routing recommendations to follow to insure a robust design. These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

3.1 Placement

The pins on the Intel 430HX PCIset (430HX) have been assigned in order to simplify routing. Figure 3-1 shows the major signal sections of the 430HX (i.e., Host, DRAM and PCI). The component placement on the motherboard should be done with this general flow in mind. This will simplify routing and minimize the number of signals which must cross. The individual signals within the respective groups have also been laid out in order to minimize any signal crossing.

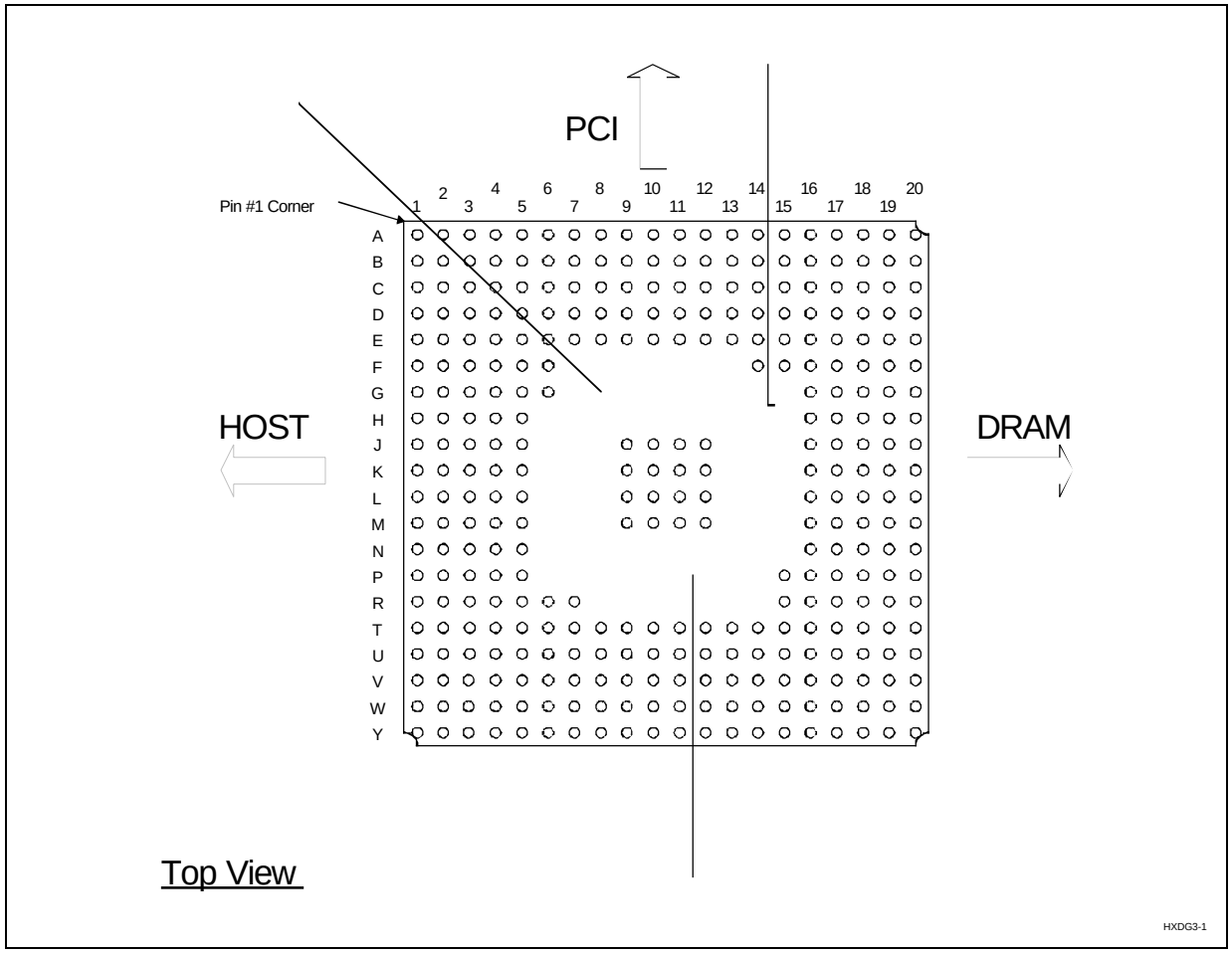


Figure 3-1. Major Signal Sections

An example of the proposed component placement for a single Pentium® processor design is shown below for a 2/3 Baby AT form factor design. Note that the example placement (Figure 3-2) shows 4 PCI slots and 3 ISA slots, while the reference design schematics show 4 PCI slots and 4 ISA slots. The figure below is for reference only and the trade-offs between the number of PCI and ISA slots, number of routed signal layers and other motherboard peripherals need to be evaluated for each design.

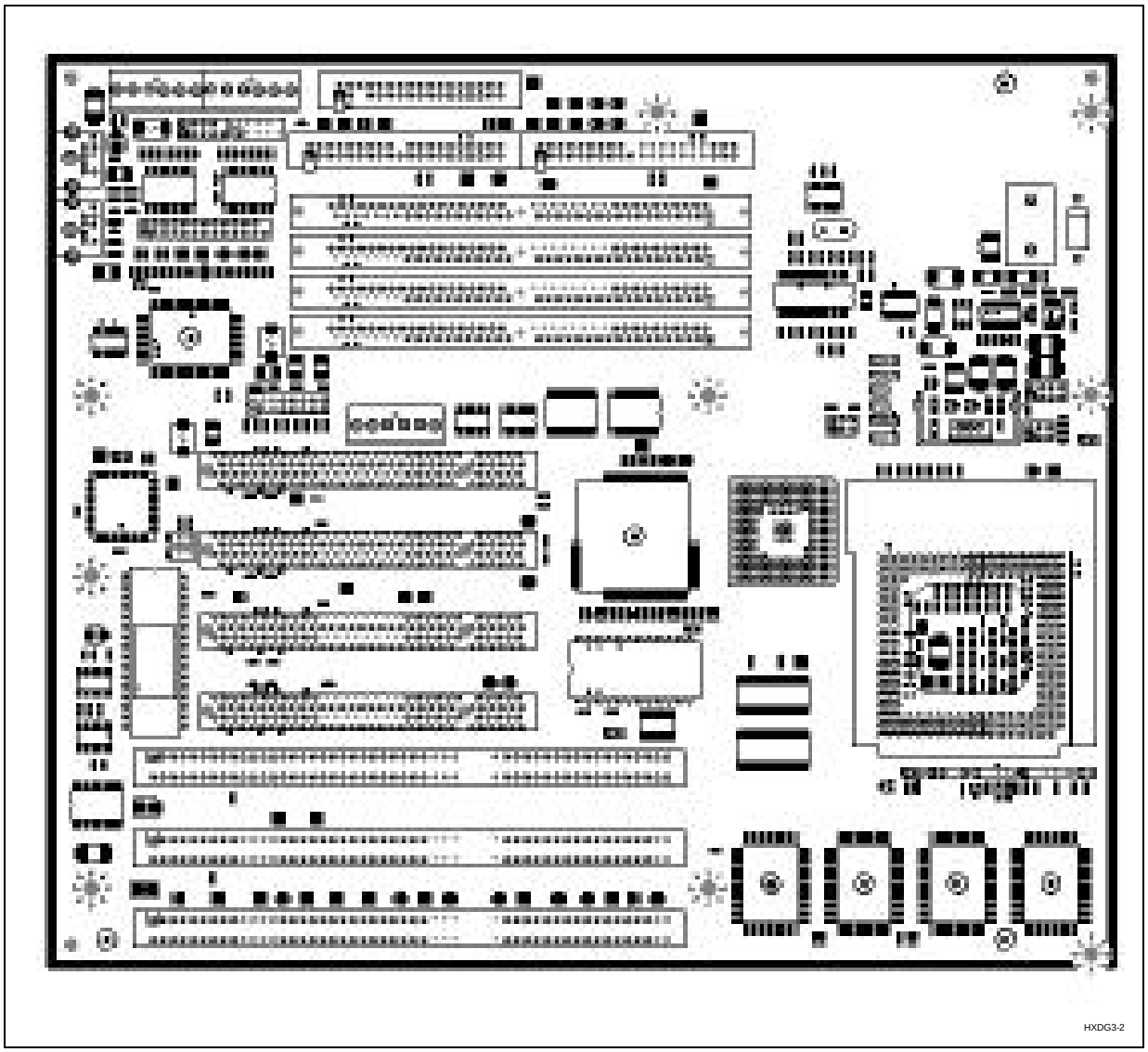


Figure 3-2. Example Baby AT Layout for Pentium processor/430HX Design

An example of the component placement for a dual Pentium processor design (6 layer board) is shown in Figure 3-3. Note that the example shows the placement for the Host, DRAM and PCI sections only. The figure is for reference only.

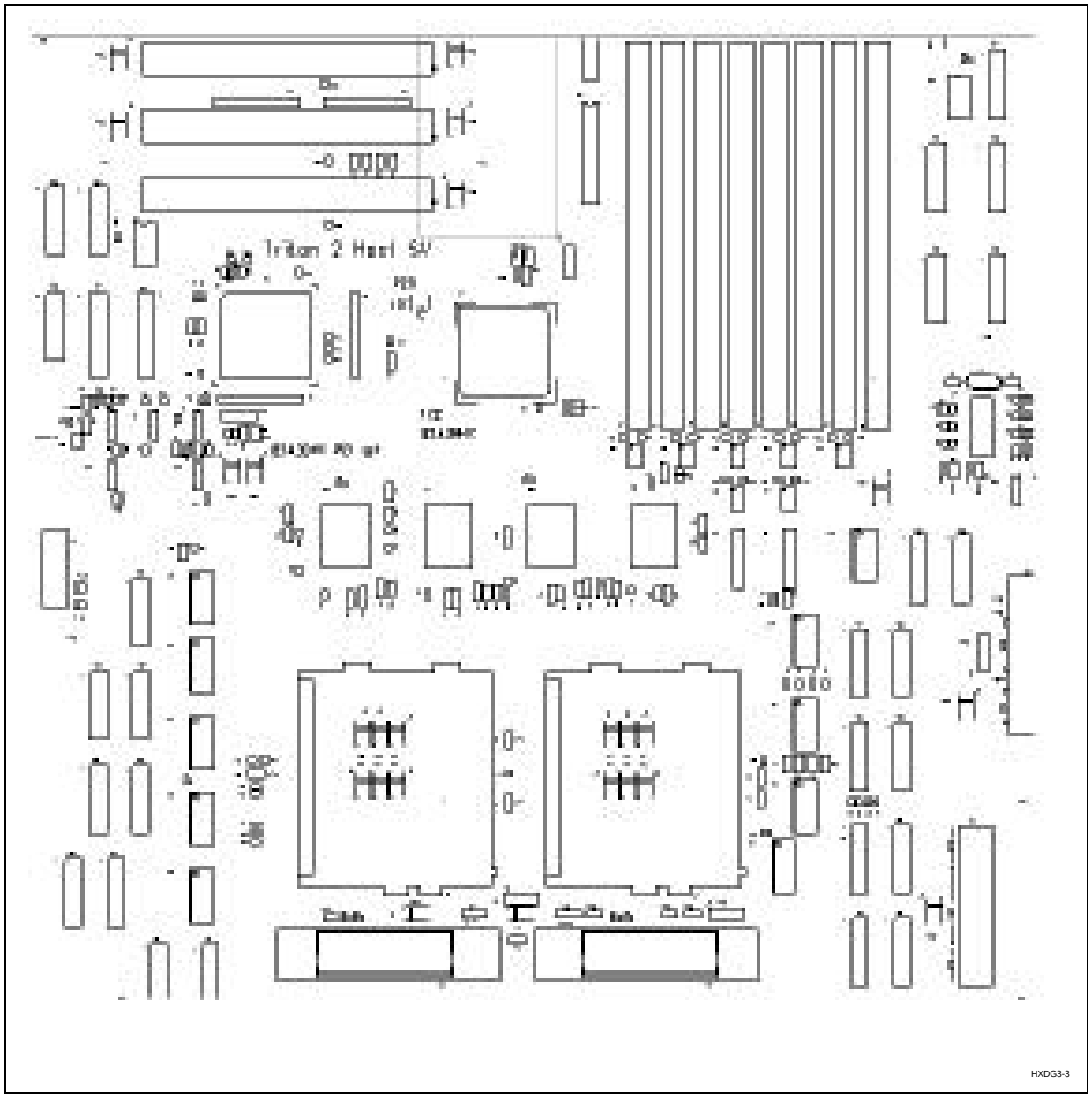


Figure 3-3. Example Dual Pentium processor/430HX Design

3.2 Board Description

A single Pentium processor/430HX PCIset motherboard can be designed using a 4-layer stack-up arrangement. The stack up of the board is shown in Figure 3-4. The impedance of all the signal layers are to be 60Ω and 90Ω. The overall board thickness is to be .062 inch.

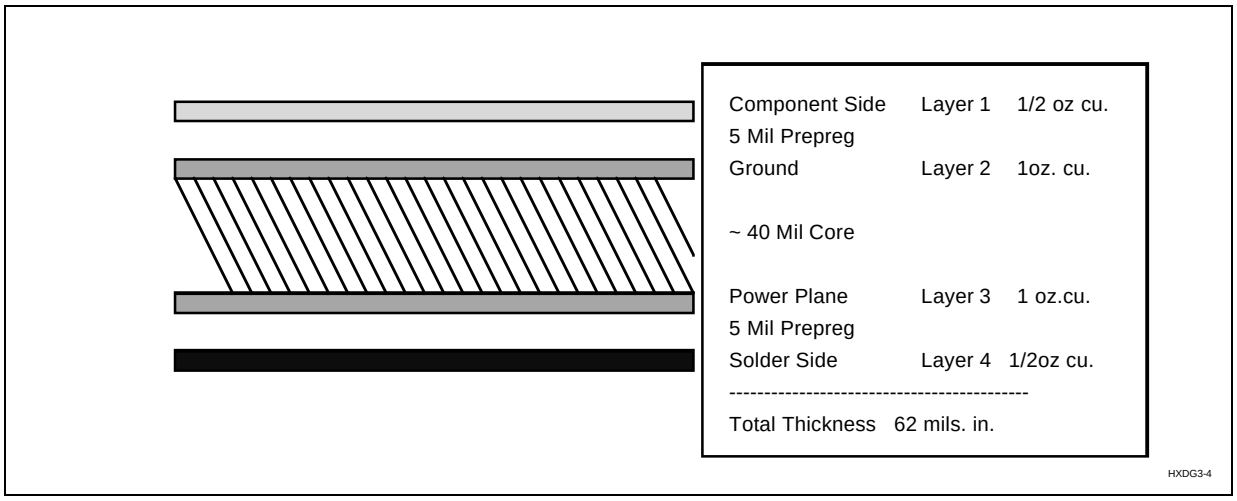


Figure 3-4. Four Layer Board Stack-up

Note that the top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will end being about 1 to 1.5 oz. cu. Please check with your fab vendor on the exact value and insure that any signal simulation accounts for this.

As mentioned above the layout of this board will first be attempted using a 4-layer stack-up. If more signal layers are needed to complete the routing of the board the following 6-layer stack-up should be used.

If a 6-layer stack-up is used, routes on the two inner layers should be orthogonal to reduce crosstalk between the layers.

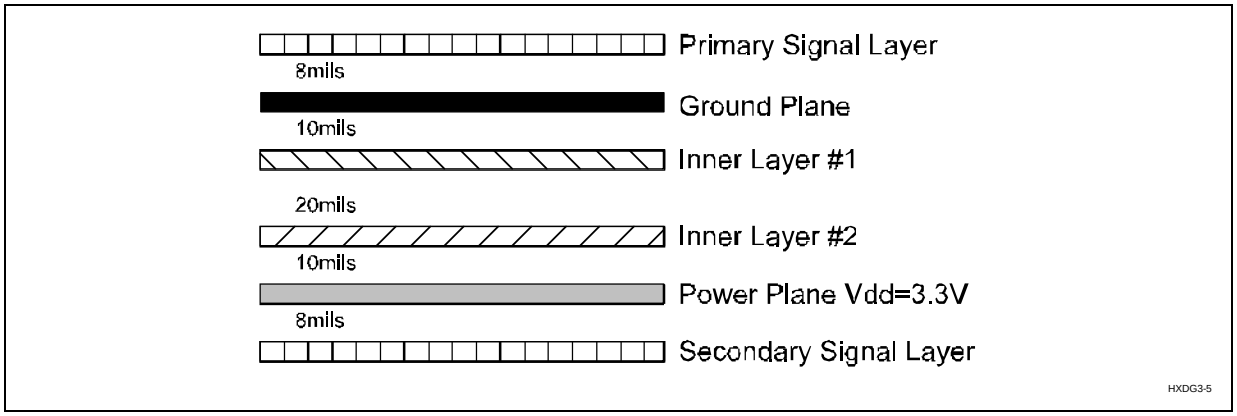


Figure 3-5. Six Layer Board Stack-up

Additional guidelines on board buildup, placement and layout include:

- The board impedence (Z) must be between 60 and 90Ω (75Ω ±20%).
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on the V_{CC} plane, not the ground plane.
- Group 5V and 3V components near each other. This will allow for fewer isolated V_{CC} islands on the power plane.
- Place vias for decoupling capacitors inside the footprint for the capacitor if possible.
- Use the first (nearest) available via site for decoupling caps if inside footprint is not possible.

3.3 BGA Component

This section addresses the layout of the 324 pin BGA component.

3.3.1 BGA Pad Size

Since the BGA component contains 5 rows of balls, it is necessary to route two traces between pads to route in a 4 layer board. Figure 3-6 shows a routing example for 24 mil and 20 mil ball pads. To route two tracks between pads, 5 mil traces and 5 mil spaces are required for a 24 mil pad size. For a 20 mil pad size, 6 mil traces and 6 mil spacing can be used. Either pad size is acceptable, so the choice is primarily determined by the manufacturer's preferred line width and spacing technology. If larger trace widths are desired, another alternative is to route 5/5 or 6/6 within the BGA pads, and then "neck up" to the larger trace widths once you have cleared the BGA component area.

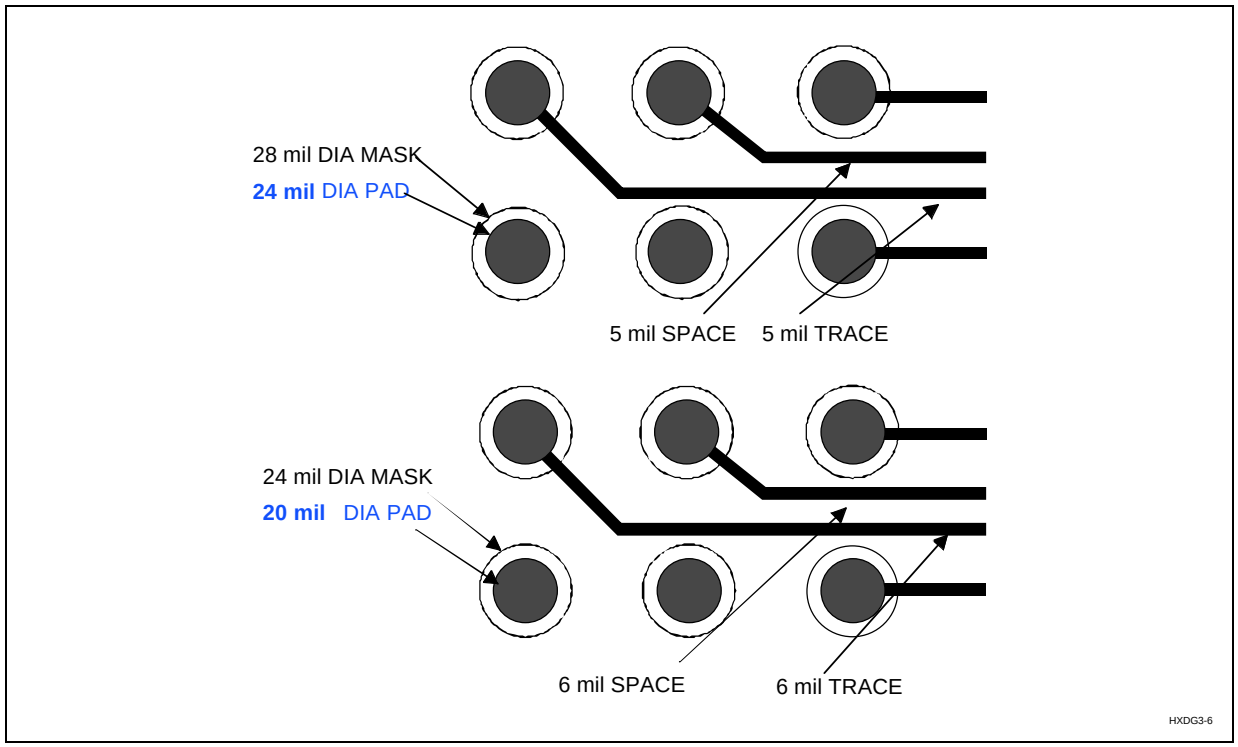


Figure 3-6. Routing Example for 24 mil and 20 mil Ball Pads

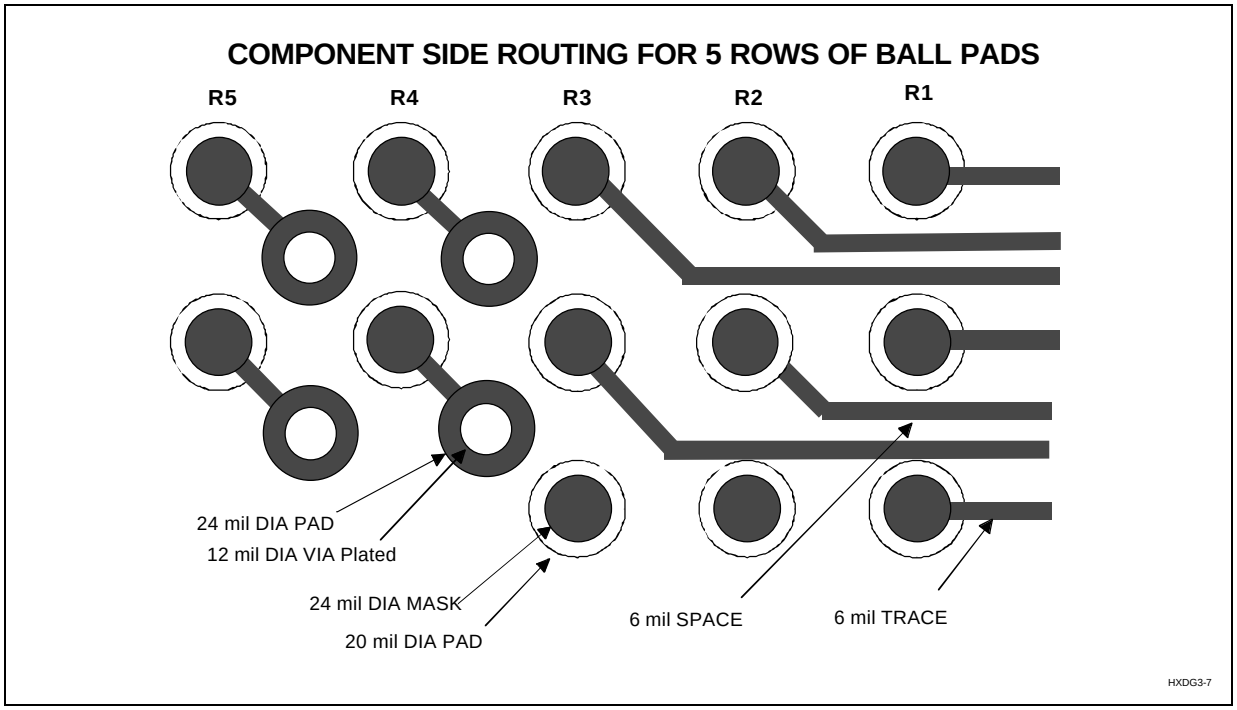


Figure 3-7. BGA Routing Example

Using the routing scheme shown above, the first 3 rows of balls can be routed on the top signal layer. The inner two rows must be routed on the bottom side of the board. As a result, vias are required in between the BGA pads. The vias will be discussed in the next section.

3.3.2 BGA Vias

Figure 3-8 shows the connection between the BGA ball pad and a via. **All vias located between the BGA ball pads must be covered with solder mask!** This prevents solder from wicking over to the via pad. A via pad size of 24 mils is recommended.

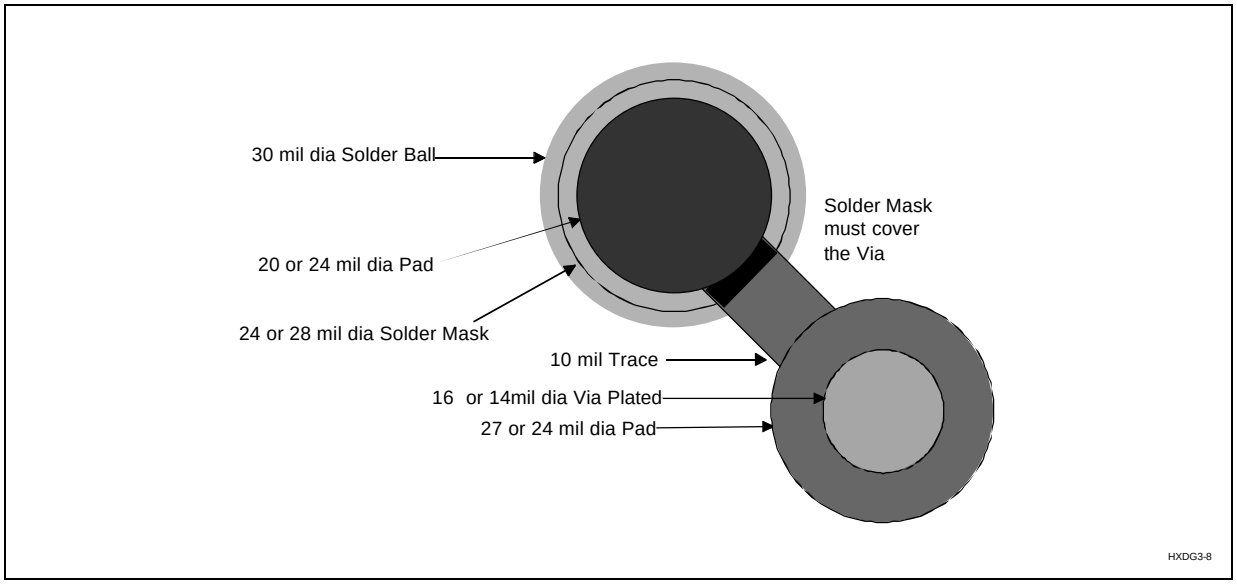


Figure 3-8. BGA Pads and Vias

3.3.3 BGA Routing

Figure 3-9 and Figure 3-10 show a routing example for both the component and solder sides of a 4-layer board. The first three rows are routed on the component side, while the inner two rows are routed on the solder side of the board. This example shows 6 mil trace widths.

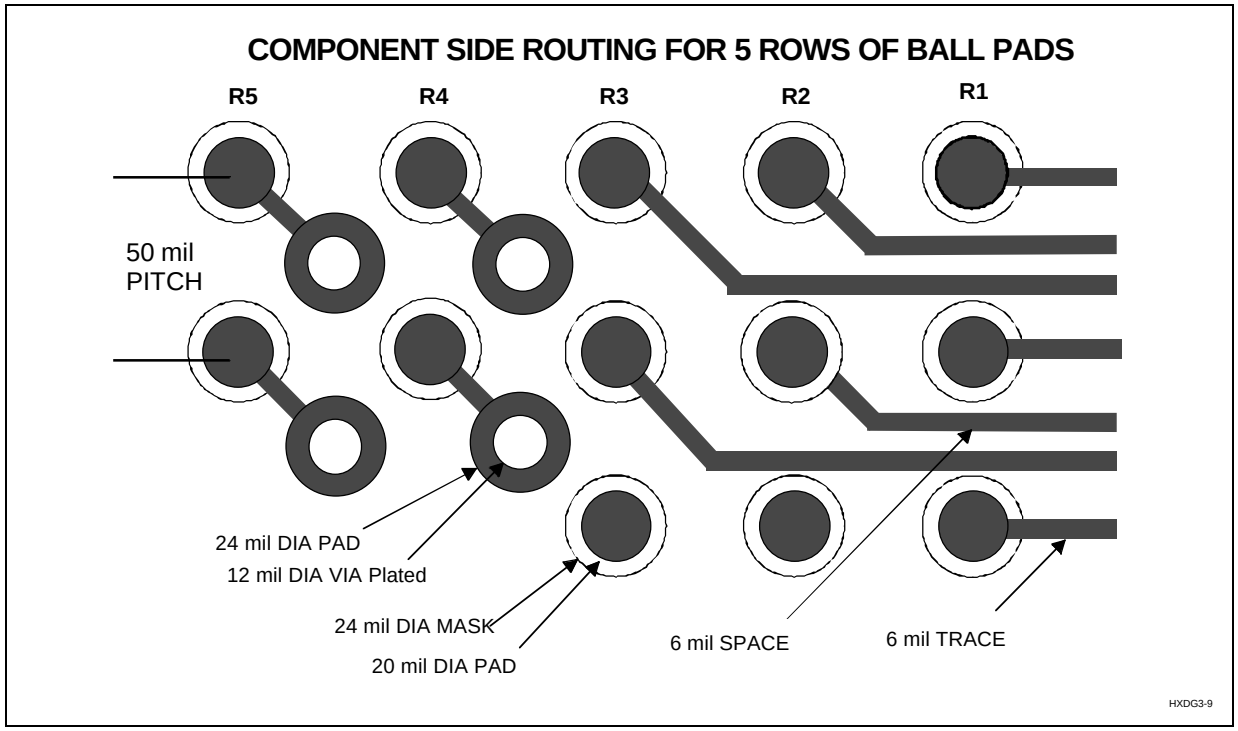


Figure 3-9. BGA Component Side Routing Example

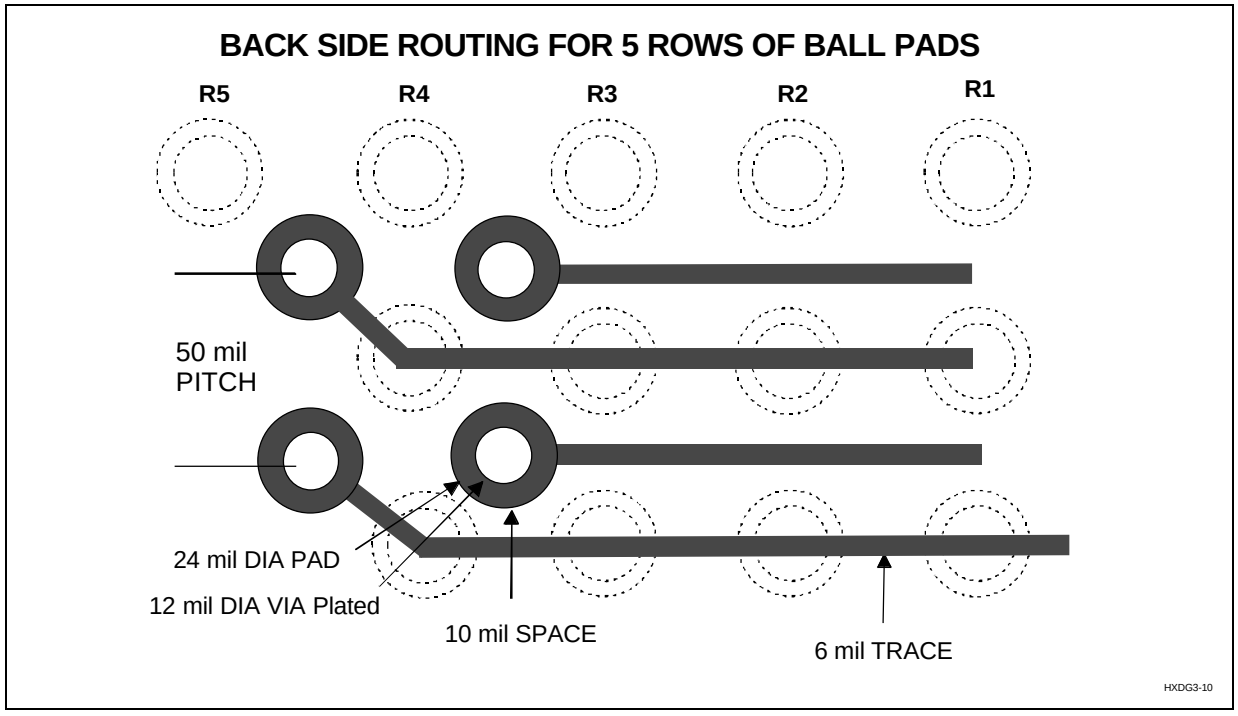


Figure 3-10. BGA Solder Side Routing Example

3.4 Routing Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. Which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed in this section are followed.

3.4.1 Host Bus Layout Guidelines

The host address, data and control signals should be routed using a “daisy chain” topology. The use of this topology implies that no stubs are to be used to connect any devices on the net. Figure 3-11 shows two possible techniques to achieve a stubless trace.

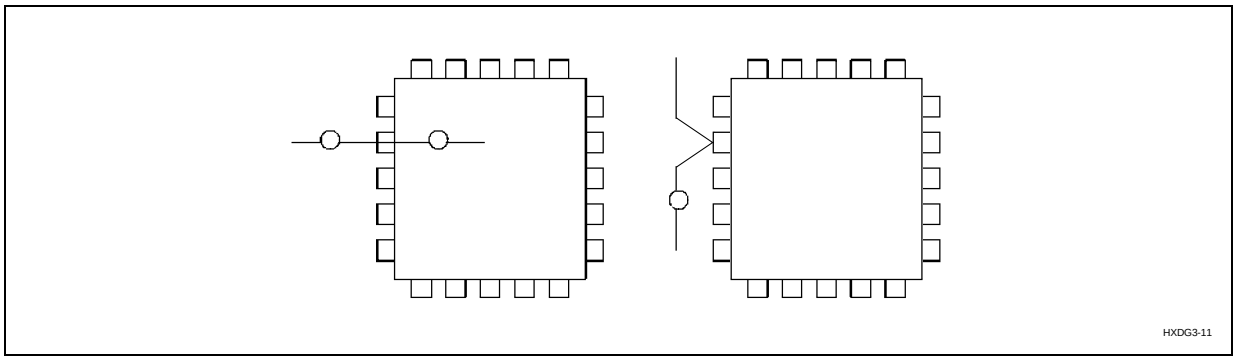


Figure 3-11. Stubless Routing Examples

In instances where it’s not possible to apply one of these two techniques (e.g., congestion), a very short stub is allowed. The length of this stub should not exceed 250 mils. Figure 3-12 shows a trace with a short stub connecting the pin.

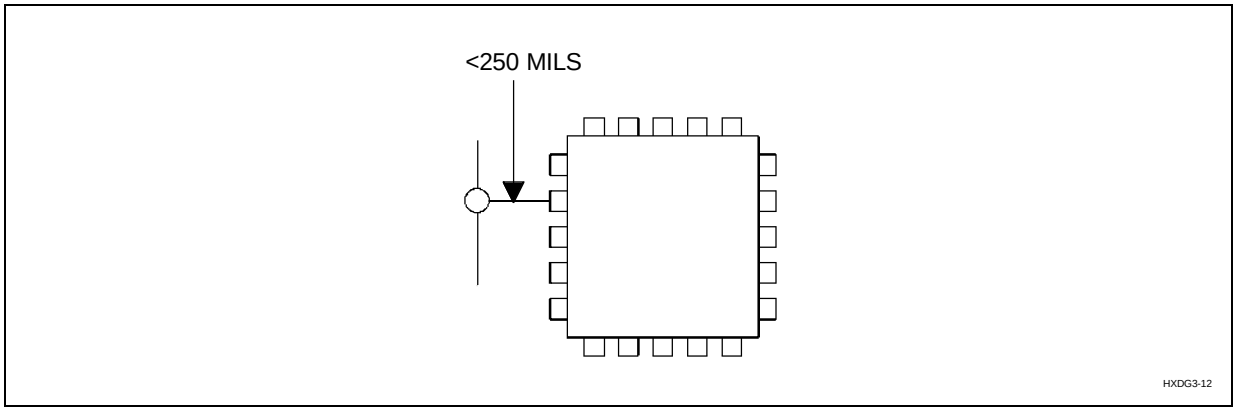


Figure 3-12. Short Stub Routing Example

Table 3-1 and Table 3-2 provide host signal trace length guidelines for single and dual processor 430HX designs.

Table 3-1. Host routing guidelines (Dual Pentium processor CPU Sockets)

Signal	Max Length	Notes
HA[31:3]	15”	CPUs, TXC, PBSRAM and Tag
HD[63:0]	10”	CPUs, TXC and PBSRAM
Control	10”	CPUs, TXC and PBSRAM

Table 3-2. Host routing guidelines (Single Pentium processor CPU Socket)

Signal	Max Length	Notes
HA[31:3]	13”	CPU, TXC, PBSRAM and Tag
HD[63:0]	8”	CPU, TXC and PBSRAM
Control	8”	CPU, TXC and PBSRAM

3.4.2 430HX Memory Subsystem Layout Guidelines

The 430HX supports a wide range of DRAM memory and system alternatives (Table 3-3).

Table 3-3. Memory Types Supported by 430HX

DRAM Type:	FPM, EDO
DRAM Module Type:	72 pin SIMM: 32 bit, 36 bit (parity), 36 bit (ECC) 168 pin DIMM: 64 bit, 72 bit
DRAM Voltage:	3.3V, 5.0V
Number of row’s of memory:	1 to 8
DRAM Speed:	50,60,70 ns
DRAM Component Width:	x4, x8, x16
CPU Bus Frequency	50, 60, 66 MHz

The text below uses the term “row” or “row of memory” to describe 64/72 bits of memory connected to the same RAS# signal. There are a few different ways to create a row of memory including:

- 2 single density 72 pin SIMMs = 1 row of memory
- 1 single density 168 pin DIMM = 1 row of memory
- 2 double density 72 pin SIMM’s = 2 rows of memory

The system designer must decide:

- how many rows of memory will the design support
- which type of DRAM module will be used

Layout guidelines are provided for two system implementation options:

- 2 to 4 rows of memory using SIMM modules
- 5 to 8 rows of memory using SIMM modules

The guidelines should be the same for DIMM modules. However, the current DIMM JEDEC standard has a drawback when used in a 430HX system design; the CAS# signals and MA[1:0] signals are buffered on the module. The 430HX has optimized performance for a non-buffered CAS# memory array. When using DIMM modules with buffered CAS# signals, an additonal wait state for the lead-off

cycle and the burst rate needs to be added. The values in Table 3-4 and Table 3-5 are for SIMM modules:

Table 3-4. Analyzed Possibilities 2 to 4 Rows of Memory:

Performance	DRAM Type	DRAM Speed (ns)	CPU Bus Freq. (MHz)
x-2-2-2	EDO	60	50, 60, 66
x-3-3-3	FPM	60	50, 60, 66

Table 3-5. Analyzed Possibilities 5 to 8 Rows of Memory:

Performance	DRAM Type	DRAM Speed (ns)	CPU Bus Freq. (MHz)
x-3-3-3	EDO	70	60, 66
x-4-4-4	FPM	70	60, 66

NOTES:

1. Analysis assumes worst case A.C. numbers for 3.3V and 5.0V DRAMs.
2. Analysis assumes worst case max load using x4 DRAMs and min load using x16 DRAMs.
3. Analysis assumes unbuffered memory signals on the SIMMs. The MA and WE# signals are unbuffered for a 2 to 4 row configuration, and buffered for 5 to 8 rows. If 168 pin DIMMs are used (which have the MA, CAS# and WE# buffered), an additional clock must be added to the lead-off and the burst rate of each cycle type above to account for the buffer delay on the CAS# signal.

The additional clock for each transfer of the burst cycle for 5 to 8 row DRAM designs is required due to:

- MA[1:0] require buffering which adds delay during burst reads (for EDO and FPM designs).
- Increased flight time on signals DRAM interface due to heavier loads with more sockets connected.

3.4.2.1 Two to Four Rows of Memory Layout Guidelines

CAS[7:0]#

Direct Connections from the TXC to the memory array. Connect each CAS# to the corresponding byte lane of memory for even CAS# loading as the DRAM rows are populated.

- Trace Length: Max: 8”
  - The CAS[7:0]# trace lengths should be the same (within 1”)
- All 8 CAS# traces should have either:
  - a series termination resistor (10 to 22Ω), or
  - a pullup and a pull down diode at the end of the trace.

RAS[3:0]#

Direct Connections from the TXC to each row of memory.

- Trace Length: Max: 8”
- The 4 RAS# traces should be the same length as the CAS# traces (within 1 inch). The RAS# signals also require a series termination resistor (22Ω).

MA[11:2], WE#

These signals do not require external buffers for a 2 to 4 row configuration. For this case, the TXC MA[11:2] and WE# buffers should be programmed to 12 ma.

- Trace Length: Max: 9” From TXC to DRAM

MAA[1:0], MAB[1:0]

In a 2 to 4 rows of memory design, MAA should be connected to the first two rows of memory, and MABx should be connected to the second two rows of memory. These signals are not buffered externally.

- Trace Length: Max: 9”

MD[63:0], MPD[7:0]

These signals connect from the TXC to each of the DRAM rows of memory.

- Trace Length: Max: 8”

Table 3-6. Summary Table for 2 to 4 Rows of Memory:

	Max Length	Notes
RAS[3:0]#	8”	TXC to DRAM
CAS[7:0]#	8”	TXC to DRAM
MA[11:2], WE#	9”	TXC to DRAM
MAA[1:0], MAB[1:0]	9”	TXC to DRAM
MD[63:0], MP[7:0]	8”	TXC to DRAM

3.4.2.2 Five to Eight Rows of Memory Layout Guidelines

CAS[7:0]#

Direct Connections from the TXC to the memory array. Connect each CAS# to the corresponding byte lane of memory for even CAS# loading as the DRAM rows are populated.

- Trace Length: Max: 10”
  - All 8 CAS# traces should be the same length (within 1 inch).
- All 8 CAS# signals should have either:
  - a series termination resistor (10 to 22Ω), or
  - a pullup and a pull down diode at the end of the trace.

RAS[7:0]#

Direct Connections from the TXC to each row of memory.

- Trace Length: Max: 10”
- The 8 RAS# traces should be the same length as the CAS# traces (within 1 inch). The RAS# signals also require series termination resistors (22Ω).

MA[11:0], WE#

These signals are all buffered using 74FCT3245A devices. Each buffered MA output should be connected to two rows of memory.

- Trace Length: Max: 10” From TXC to Buffer + Buffer to DRAM

MD[63:0], MPD[7:0]

These signals connect from the TXC to each of the DRAM rows of memory.

- Trace Length: Max: 10”

Table 3-7. Summary Table for 5 to 8 Rows of Memory:

Signal	Max Length	Notes
RAS[3:0]#	10”	TXC to DRAM
CAS[7:0]#	10”	TXC to DRAM
MA[11:0], WE#	10”	TXC to Buffer and Buffer to DRAM combined length
MD[63:0], MP[7:0]	10”	TXC to DRAM

3.4.3 Clock Routing Guidelines

Table 3-8 summarizes the clocks in a 430HX system design.

Table 3-8. Clocks in a 430HX System

Host Clocks	PCI Clocks	Miscellaneous
Pentium CPU (one or two)	TXC	USB (24 or 48 MHz)
TXC	PIIX3	Keyboard (12 MHz)
PBSRAM (4 Max)	I/O APIC (Dual CPU only)	Floppy clock (24 MHz)
	4 PCI Slots	ISA bus OSC (14 MHz)
		Bus Clock (8 MHz from PIIX3)

The host and PCI clock routing require the most attention to detail. Clock skew requirements are given below.

3.4.3.1 Host Clock Skew Requirements

The total skew between the CPU and TXC must be less than 300 ps. The total skew between the CPU or TXC and the PBSRAM must be less than 500 ps. The clock synthesizer must guarantee a maximum skew of 250 ps between any two host clock outputs. Two output pins of the clock synthesizer should be connected together and used to drive the host clocks for the CPU and TXC. This eliminates the pin to pin skew of the synthesizer. The system design must guarantee a maximum flight time skew of 250 ps or less between any two host clock receivers. The maximum length on any of the host clocks should be less than 8 inches.

3.4.3.2 Host Clock to PCI Clock

The clock synthesizer must guarantee a delay from the host clock output to the PCI clock outputs. The minimum delay must be 1 ns and the maximum delay should not exceed 5 ns. The system must insure that the host clock to PCI clock skew seen at the TXC is a minimum of +1 ns and a max of +6 ns. This means all of the PCI clock flight times should be guaranteed to be 1 ns greater than the host clock flight times.

3.4.3.3 PCI Clock Skew

The total skew between any two PCI clock loads must be less than 2.0 ns. The clock synthesizer must guarantee a maximum skew of 500 ps between any two PCI clock outputs. The system design must guarantee a maximum flight time skew of 1.5 ns between any two PCI clock receivers. PCI clock traces to on-board components should be 2.5 inches longer than PCI clock traces going to PCI slots to help minimize skew.

The maximum length on any of the PCI clocks to motherboard devices should be less than 15 inches and should be less than 12.5 inches to any PCI add-in slot.

As a final note, any clock signals crossing from 3.3V area to 5V should cross the boundary adjacent to the ground plane.

3.5 IDE Routing Guidelines

This section contains guidelines for connecting and routing the PIIX3 IDE interface. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination. The current recommendations use 47Ω resistors on DIOR#/DIOW#, while the remaining signals use resistors between 22 and 47Ω resistors.

Cabling

- **Length of cable**: Each IDE cable must be equal to or less than 18 inches.
- **Capacitance**: Less than 30 pF.
- **Placement** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

Motherboard

- **PIIX3 Placement**: The PIIX should be placed as close as possible to the ATA connector(s).
- **Resistor Location** The termination resistors should be in series and placed as close to the IDE motherboard header as possible if the PIIX < 4 inches from the IDE header. See the following figure (3-13) for a placement example. If the PIIX is > 4 inches from the IDE header, then the resistors should be placed as close as possible to the PIIX and Figure 3-13 does not apply.
- **Capacitance** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- **Series Termination** The following resistor values are the current recommendations.

Signal	Resistor
DD[15:0]	22-47Ω
DA[2:0]	22-47Ω
DIOR#	47Ω
DIOW#	47Ω
DDRQ0	22-47Ω
DDRQ1	22-47Ω
DIRQ0	22-47Ω
RESET*	22-47Ω

Signal	Resistor
CS1P#	22-47Ω
CS1S#	22-47Ω
CS3P#	22-47Ω
CS3S#	22-47Ω
DIRQ1	22-47Ω
DDAK0	22-47Ω
DDAK1	22-47Ω

* RESET comes from the PIIX3 RSTDRV signal through a schmitt trigger

One resistor per IDE connector is recommended for all signals. For signals labeled as 22Ω–47Ω, the correct value should be determined for each unique motherboard design, based on signal quality.

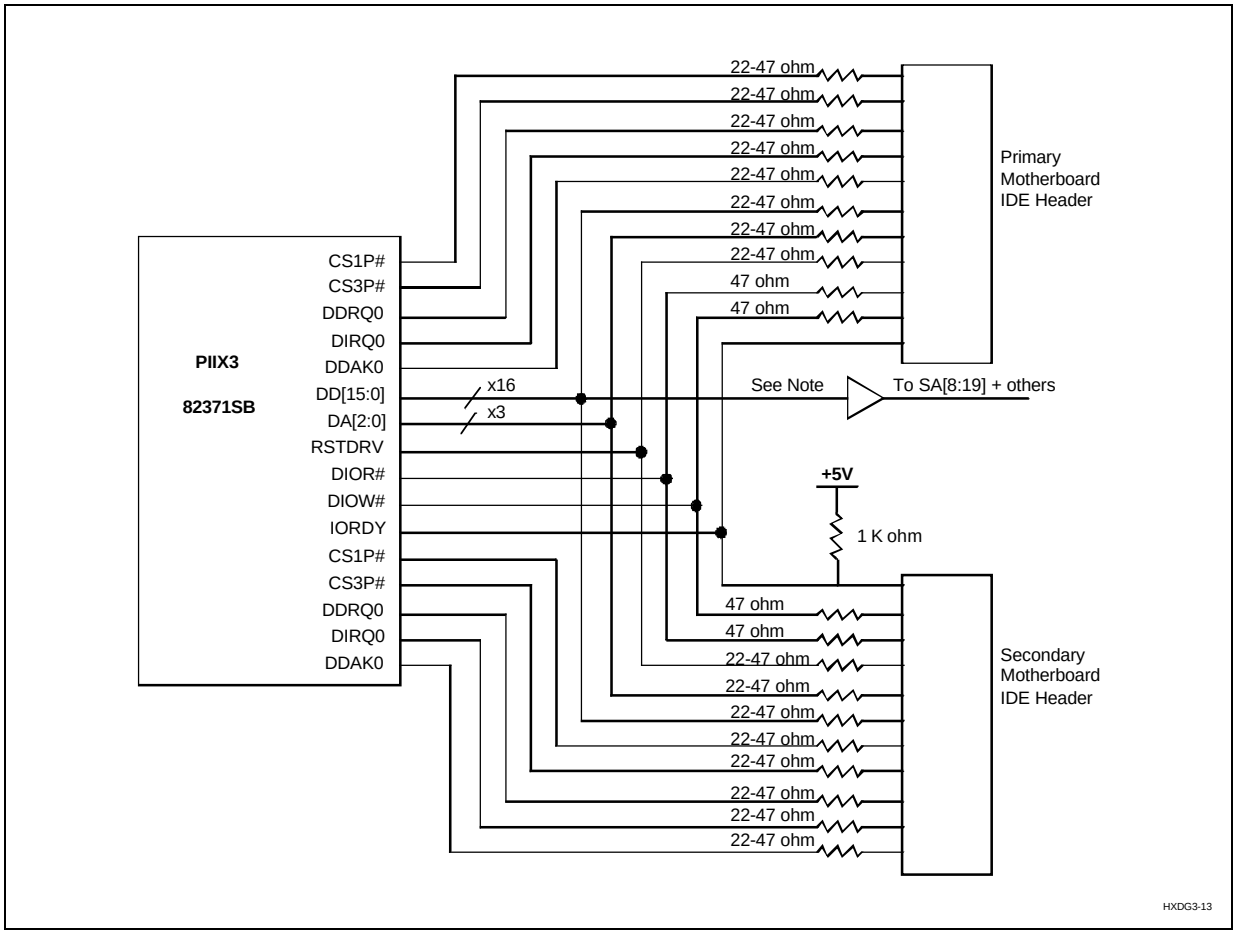


Figure 3-13. Series Resistors Required for IDE Connectors

For signals that go to both connectors, have the length on each side of the T (where the trace splits to go to each resistor then connector) as small as possible.

Note: The DD[15:0] are buffered to generate the SA[19:8], SBHE# and APICCS# signals. If possible, route the DD[15:0] traces from the PIIX3 to the the buffer input pins, then to the split for the two resistors as shown in Figure 3-14. Otherwise, keep any additional stub length from the PIIX3 DD[15:0] trace to the buffer input as short as possible.

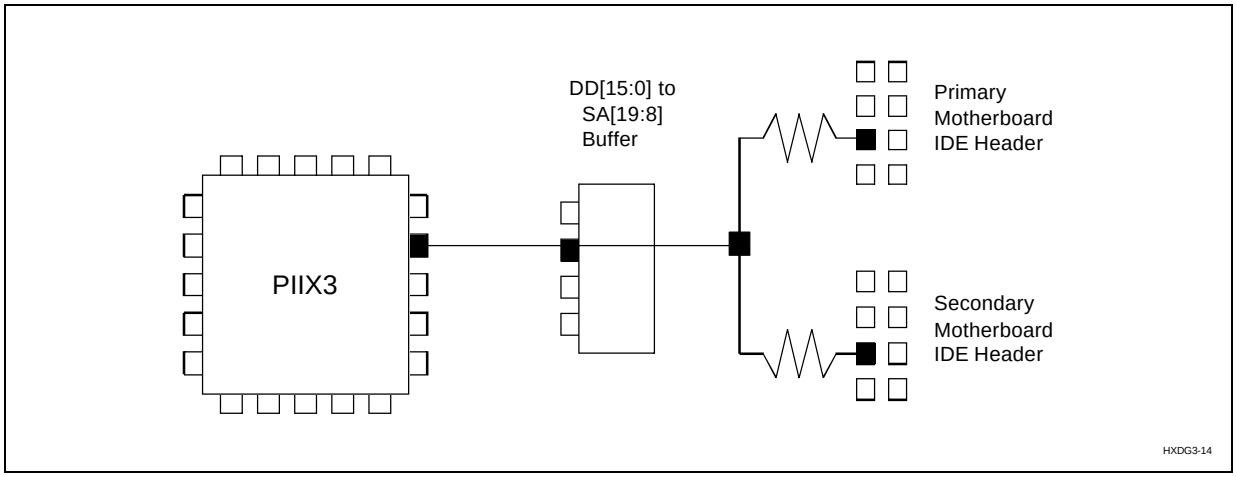


Figure 3-14. Layout Guideline for DD[15:0]

3.6 Motherboard Layout Guidelines for PIIX3 USB Implementations

3.6.1 PIIX3 Implementation

PIIX3 contains a Universal Serial Bus (USB) Host Controller which moves data between the main system memory and devices on the USB. The host controller also includes the root hub with two USB ports. This permits the connection of two USB peripherals or hub devices directly to the PIIX3. The PIIX3 Host Controller completely supports the standard Universal Host Controller Interface (UHCI) and takes advantage of the UHCI software drivers.

PIIX3 fully supports the USB Specification, Revision 1.0 electrical specifications. PIIX3 supports both full speed and low speed signalings (12 Mbps and 1.5 Mbps) and can differentiate between full speed and low speed devices connected to its USB ports.

The key electrical requirements of USB for a motherboard design are:

- The rise and fall times of 12 Mbps data signals are 4 to 20 ns.
- The rise and fall times of 1.5 Mbps data signal are 75 to 300 ns.
- 90Ω signal impedance for the full speed differential signal.
- Single-ended zero state on USB ports when no function is attached.
- 500 mA minimum of DC supply current for each USB port.
- The voltage supplied by host is 4.75V to 5.25V.

3.6.2 USB Power Distribution Layout Guideline

Following are general guidelines for USB power line and ground line:

- Each V_{CC} power line should be bypassed with no less than a 120 µF tantalum capacitor for each USB port. It should be placed between ferrite bead and EMI bypass capacitor on V_{CC}. The bypass capacitors should have a low dissipation factor to allow decoupling at higher frequencies.
- Ferrite beads and bypass caps are recommended on V_{CC} and V_{SS}, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The capacitor values should be between 0.01 µF and 0.10 µF. The recommended value of ferrite beads is 100Ω at 100 MHz.
- PolySwitch fuses, standard fuses, or some type of solid state switch should be used on each power line for overcurrent protection. USB spec requires that current be limited to 5 units load (1 unit = 100 mA) for each USB port. However, the circuit protector must be chosen so that it will not trip for power on or dynamic attach transient current. The reasonable value for the trip current is 1.5A to 2.0A, and it shall not exceed 5A maximum.

Table 3-9. DC Electrical Characteristics on V_{cc}

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Powered Host)	Vcc	4.75	5.25	V	1
Supply Current (Powered Host)		500		mA	2,3

NOTES:

1. The minimum supply voltage is 4.75V on USB port after voltage drop on power line and connector. A minimum of 120 µf tantalum cap is needed for a maximum 330 mV droop.
2. The supply current cannot exceed 5.0A. The recommended trip current (minimum) is 1.5A–2.0A.
3. The recommended time not to trip is 100 µs minimum for solid state switch circuit for power on and dynamic attach transient current.

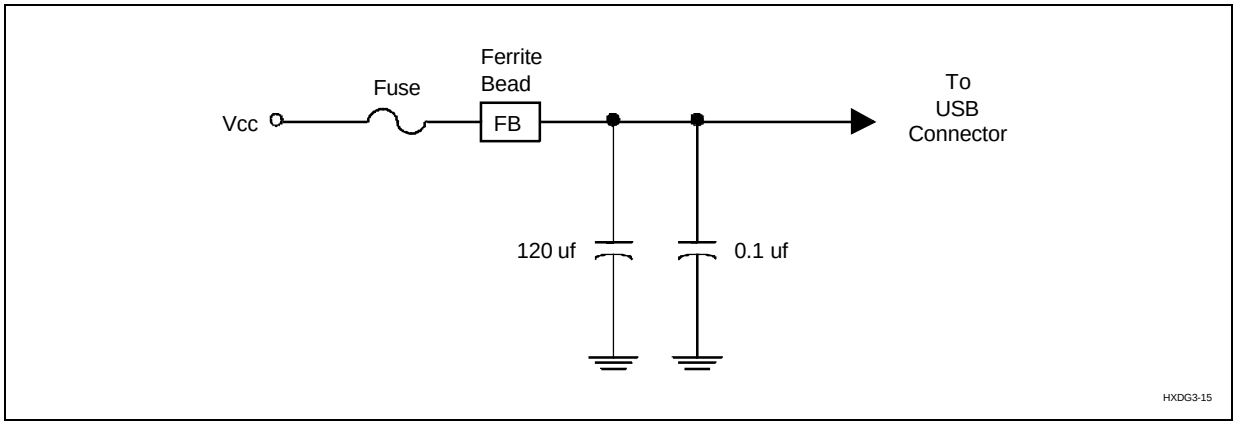


Figure 3-15. USB Power Distribution Layout

3.6.3 USB Motherboard Layout Guidelines For USB Data Signals

The goal of the following routing guidelines are to minimize the effects of ringing, crosstalk, and EMI radiation in the USB data signal lines. It is very important to ensure that high frequency system signals do not couple to the USB signals and radiate out on the USB cable. This is done by carefully matching the motherboard circuitry impedance to that of the twisted pair USB cable, by controlling signal rise and fall times, and by careful routing of the USB signals on the motherboard.

Following are general guidelines for the USB interface:

- 27Ω series resistors should be placed as close as possible to the PIIX3 (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pf caps must be placed as close to the PIIX3 as possible and on the PIIX3 side of the series resistors on the USB data lines (P0±, P1±). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are REQUIRED for signal termination by USB specification. The length of stub should be as short as possible.
- The trace impedance for the P0±, P1± signals should be 45Ω (to the ground) for each USB signal P+ or P-. The impedance is 90Ω between the differential signal pairs P+ and P- to match the 90Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90Ω is the series impedance of both wires, resulting in an individual wire presenting a 45Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as “critical signals” (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. (Common mode current is caused by differential signals whose currents are not perfectly matched.)
- Ferrite beads and bypass caps are recommended on V_{CC} and V_{SS}, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The capacitor values should be between 0.01 µF and 0.10 µF. The recommended value of ferrite beads is 100Ω at 100 MHz.

Figure 3-16illustrates the recommended USB signals schematic:

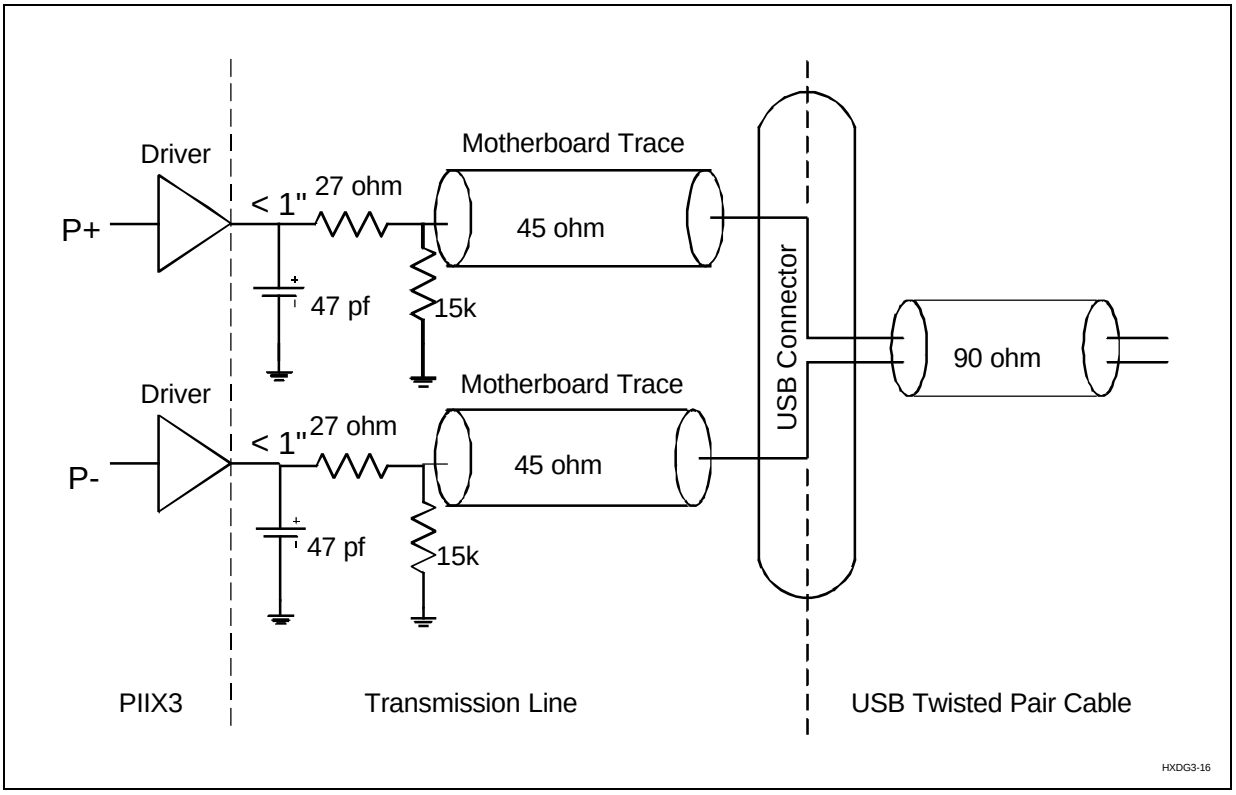


Figure 3-16. USB Data Signals

Figure 3-17 illustrates a possible configuration for having a 45Ω transmission trace. The system designer is responsible for ensuring that a particular configuration meets their requirements.

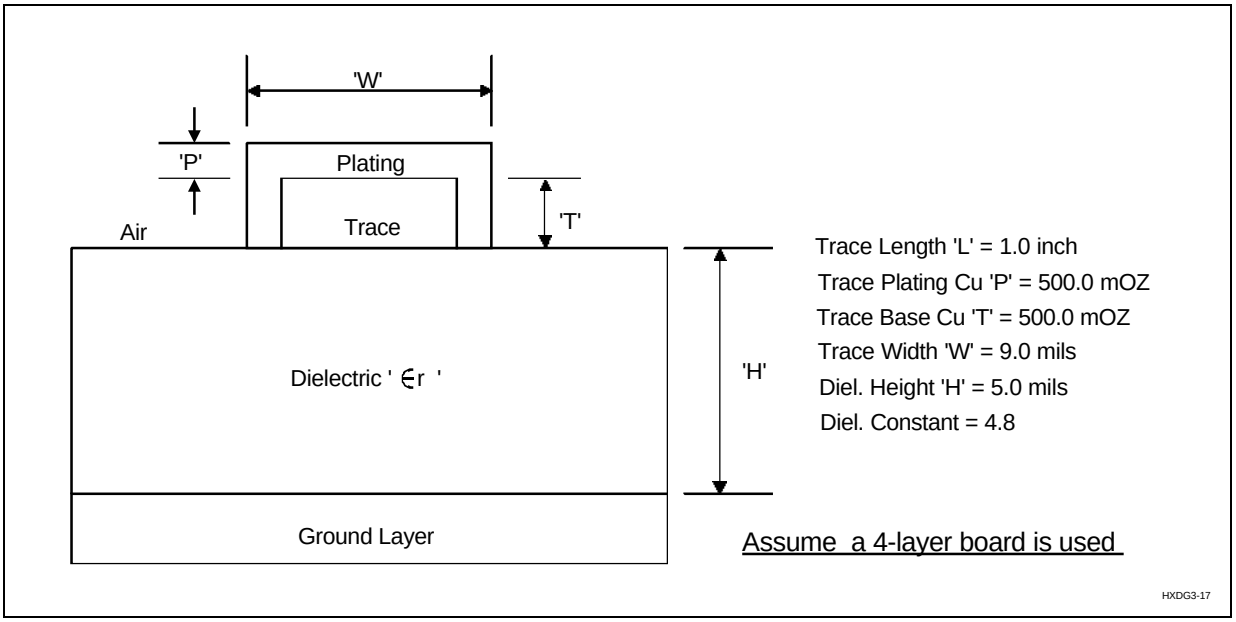


Figure 3-17. Configuration Example Using a 45Ω transmission trace

The results of above example are:

- Impedance ‘Z0’ = 45.4Ω
- Line Delay = 160.2 pSEC
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Resistance @ 20°C = 53.9 mΩ
- Trace Height = 1.4 mil

3.6.4 Options for USB Connector Implementation

There are two options recommended for attaching the USB signal and power lines to the external connector. The first is the simplest, as the connector attaches directly to the motherboard and no further design considerations are necessary. The second involves use of a printed circuit riser card to connect the USB lines from a motherboard header to a USB connector installed into a standard PC slot tab. The printed circuit riser card must be designed following the guidelines mentioned in the previous section.

A ribbon cable must not be used in place of the printed circuit riser card due to adverse effects on circuit characteristics and EMI radiation.

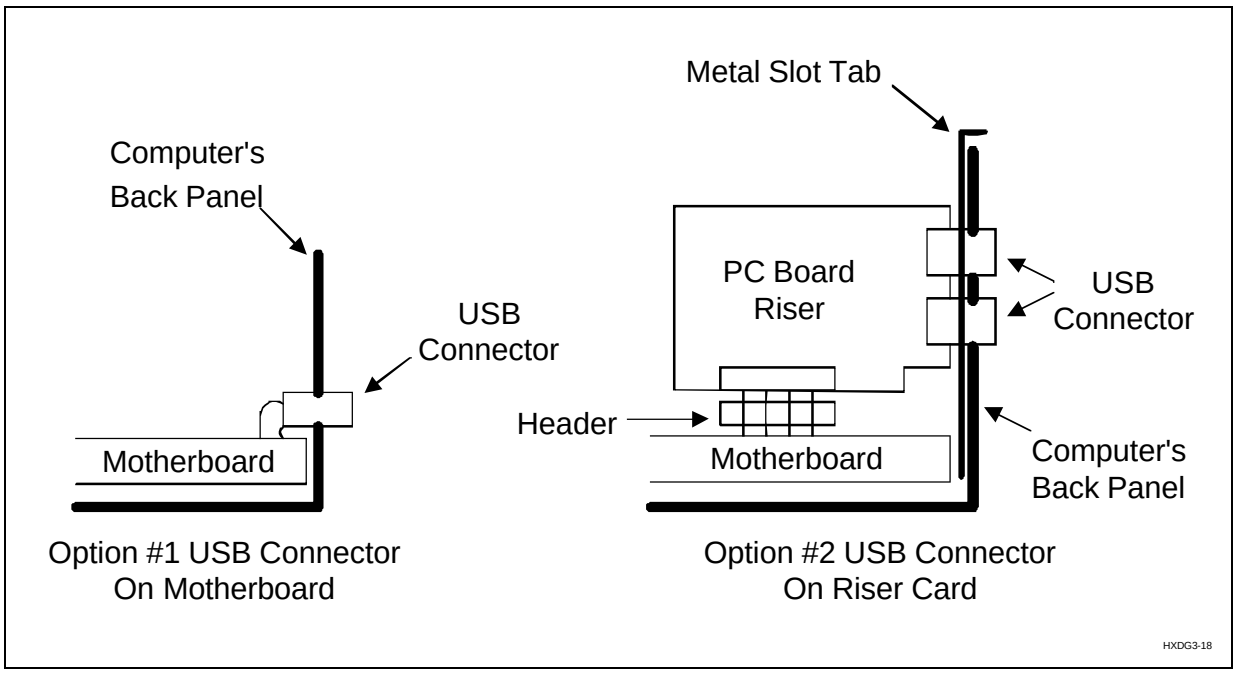


Figure 3-18. Options For USB Connector

For the printed circuit implementation, it is important that the previously described guidelines for USB signal pairs on the motherboard and the riser card are 90Ω. Figure 3-19 shows the impedance model of USB transmission lines with use of a riser card.

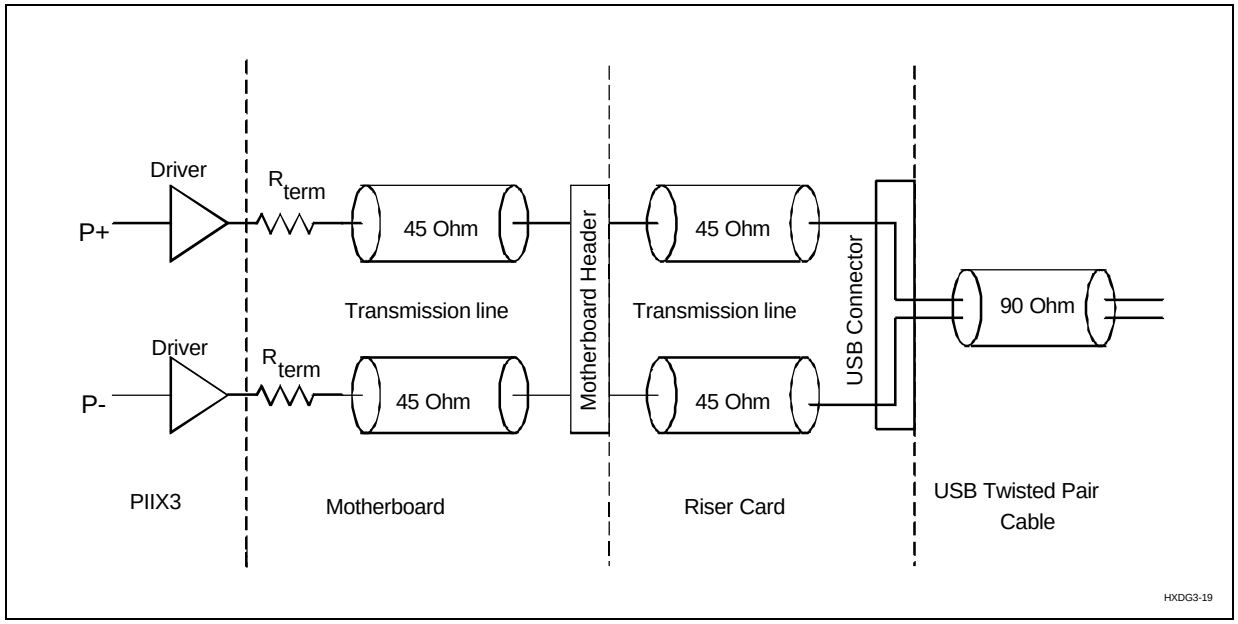


Figure 3-19. USB Data Signals With Riser Card

4

430HX System Clock Requirements

CHAPTER 4
430HX SYSTEM CLOCK REQUIREMENTS

4. 430HX System Clock Requirements

This section outlines the recommended clock synthesizer specifications for an Intel 430HX PCIset (430HX) system design.Table 4-1 lists the A.C. timing requirements of the clock generation logic.

Table 4-1. AC Timing Requirements

Sym	Parameter	66 MHz		60 MHz		Units	Notes
		Min	Max	Min	Max		
tHKP	Host CLK period	15		16.7		ns	
tHKPS	Host CLK period stability		250		250	ps	1,7
tHKH	Host CLK high time	5		5		ns	4
tHKL	Host CLK low time	5		5		ns	5
tHRISE	Host CLK rise time	0.5	2.0	0.5	2.0	ns	8
tHFALL	Host CLK fall time	0.5	2.0	0.5	2.0	ns	8
tJITTER	Host CLK Jitter		200		200	ps	
Duty Cycle	Measured at 1.5V	45	55	45	55	%	
tHSKW	Host Bus CLK Skew		250		250	ps	1
tHSTB	Host CLK Stabilization from power-up		3		3	ms	6
tPKP	PCI CLK period	30.0	∞	33.3	∞	ns	2
tPKPS	PCI CLK period stability		500		500	ps	7
tPKH	PCI CLK high time	12		13.3		ns	
tPKL	PCI CLK low time	12		13.3		ns	
tPSKW	PCI Bus CLK Skew		500		500	ps	1
tHPOFFSET	Host to PCI Clock Offset	1.0	4.0	1.0	4.0	ns	1,3
tPSTB	PCI CLK Stabilization from power-up		3		3	ms	6

NOTES:

1. These signals are measured on the rising edge of adjacent CLKs at 1.5V.
2. PCI Clock is the host clock divided by two.
3. The Host CLK must always lead the PCI CLK as shown in Figure 4-2. This must be guaranteed by design under loaded conditions. This is a function of drive strength as well as routing topologies. This is a combined CLK driver requirement and a layout requirement.
4. tHKH is measured at 2.4V as shown in Figure 4-3.
5. tHKL is measured at 0.4V as shown in Figure 4-3.
6. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
7. Defined as once the clock is at its nominal operating frequency the adjacent period changes can not exceed the time specified.
8. tHRISE and tHFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.4V (1 mA) JEDEC Specification.

4.1 PIIX3 USBCLK Requirements

This section outlines the recommended USB clock input specifications for a 82371SB PIIX3 system design. Table 4-2 lists the A.C. timing requirements of the clock generation logic.

Table 4-2. AC Timing Requirements

Sym	Parameter	48 MHz		24 MHz		Units	Notes
		Min	Max	Min	Max		
Frequency Tolerance	USB CLK Frequency Tolerance		±2500		±2500	ppm	
tUKH	USB CLK high time	7		17.5		ns	1
tUKL	USB CLK low time	7		17.5		ns	2
tURISE	USB CLK rise time		1.2		1.2	ns	3
tUFALL	USB CLK fall time		1.2		1.2	ns	3
tJITTER	USB CLK Jitter, Cycle-to-Cycle		500		500	ps	4
tJITTER, Absolute	USB CLK Jitter, Absolute		±700		±700	ps	
Duty Cycle	Measured at 1.5V	40	60	45	55	%	

NOTES:

1. tUKH is measured at 2.0V as shown in Figure 4-1.
2. tUKL is measured at 0.8V as shown in Figure 4-1.
3. tURISE and tUFALL are measured as a transition time through the threshold region Vol = 0.8V and Voh = 2.0V.
4. Frequency Tolerance needs to be taken into the consideration in a particular implementation. See USBCLK Jitter section.

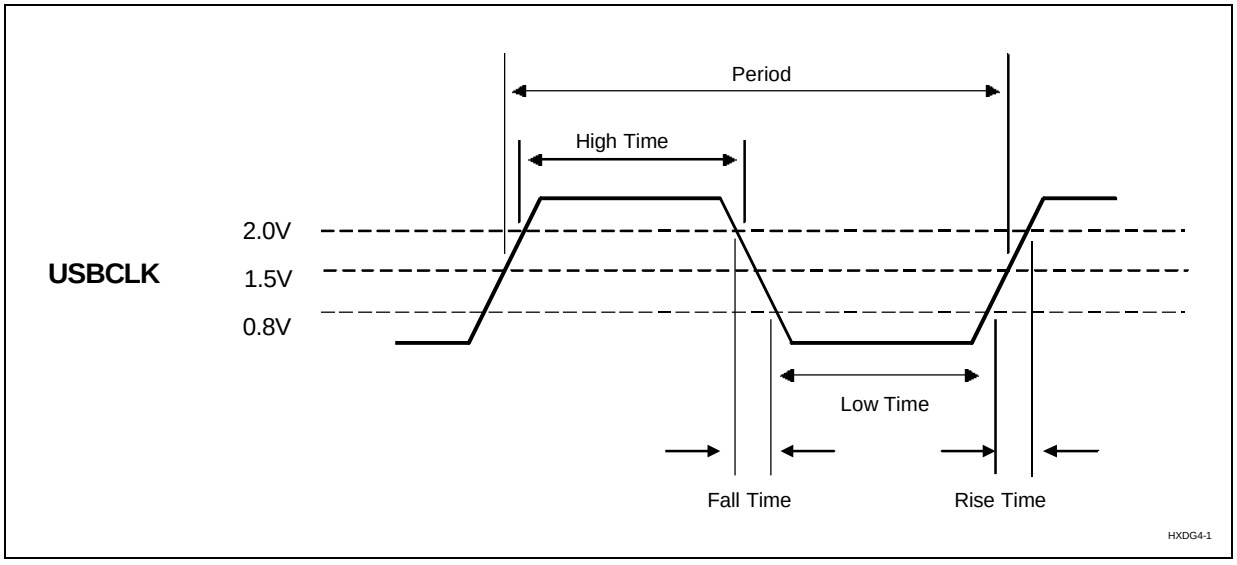


Figure 4-1. USBCLK Waveform

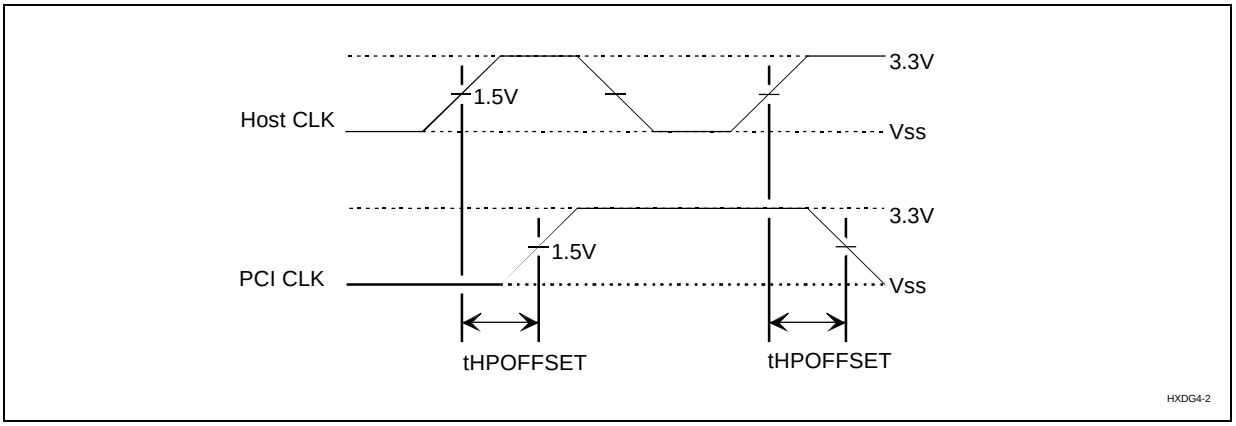


Figure 4-2. Host CLK to Host CLK Skew

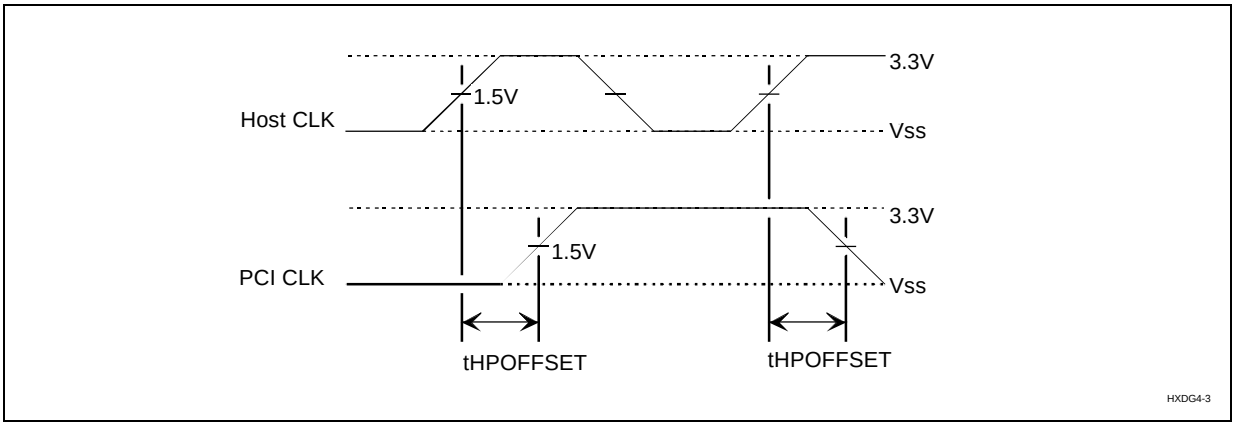


Figure 4-3. Host CLK to PCI CLK Offset

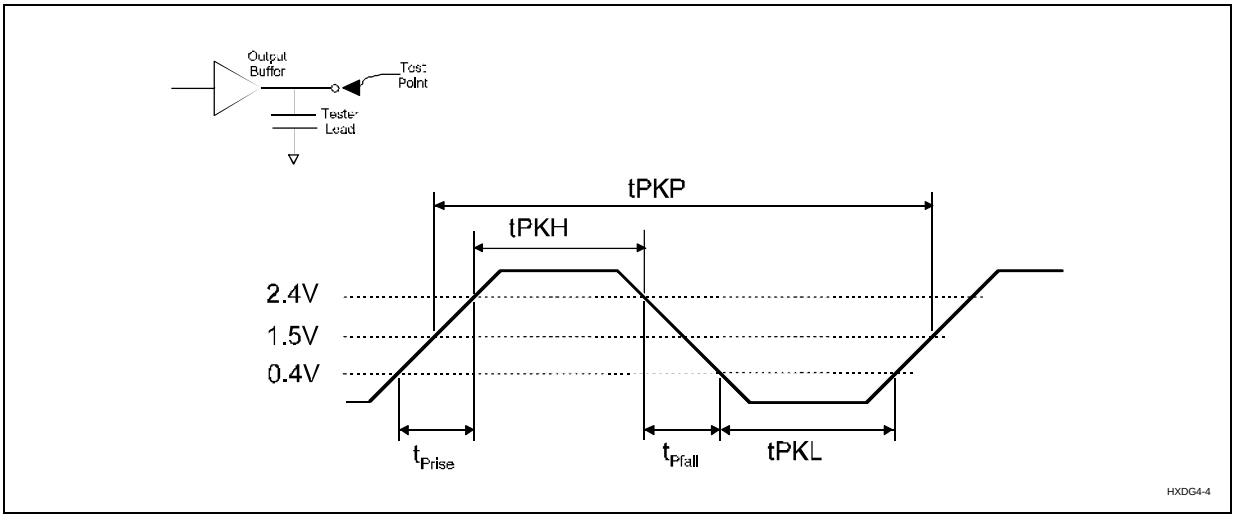


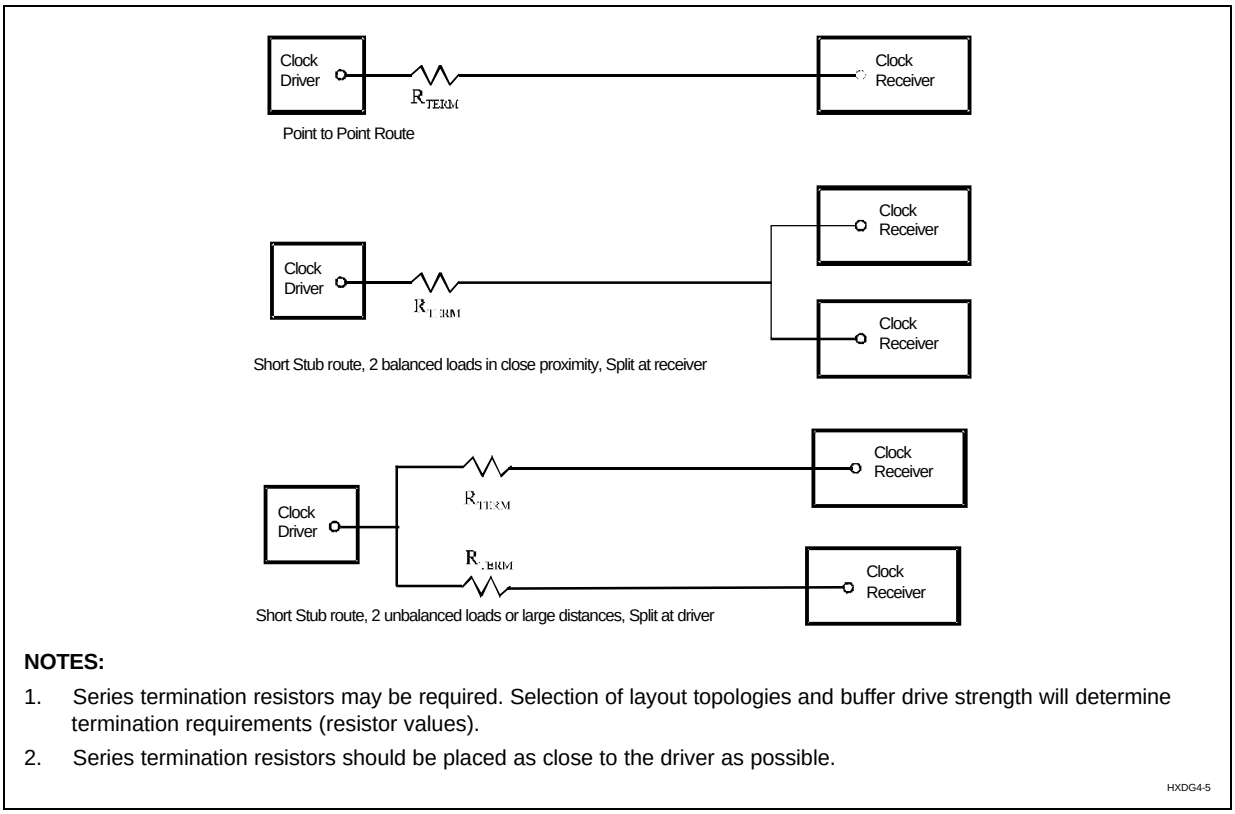
Figure 4-4. Clock Waveform

Table 4-3. Maximum Expected Capacitive Loads on Clocks

Clock	Load	Units	Notes
CPU Clocks (PCLK)	15	pF	1 or 2 loads
PCI Clocks (BCLK)	35	pF	1 slot to 2 motherboard loads
24 or 48 MHz	20	pF	2 motherboard loads
Ref0	45	pF	3 slots max.
Ref1	30	pF	2 slots max.
Ref2 or 12 MHz	25	pF	3 motherboard devices max.

4.2 System Considerations

Figure 4-5typical Clock Driver routing topologies for the 430HX platforms



NOTES:

1. Series termination resistors may be required. Selection of layout topologies and buffer drive strength will determine termination requirements (resistor values).
2. Series termination resistors should be placed as close to the driver as possible.

Figure 4-5. Clock Routing Topologies

Table 4-4. Characteristics at Clock Destination

Symbol	Parameter	Min	Max	Units	Notes
V_{ih}	3.3V Input High Voltage	2.0	V_{DD} + .3	V	1
V_{il}	3.3V Input Low Voltage	-0.3	0.8	V	1
C_{in}	Input Pin Capacitance		6	pF	

NOTES:

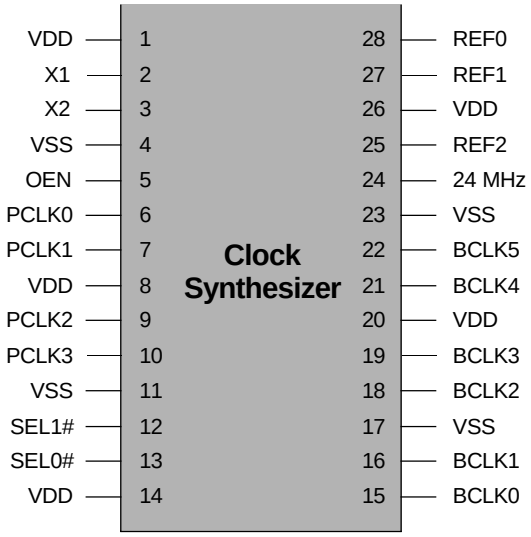
1. Signal edge is required to be monotonic when transitioning through this region.

4.3 Suggested Pinout Requirements

The following section defines a generic pinout and base requirements for 430HX Reference Platform Designs. This section can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived. Please contact the specific clock synthesizer vendors for their respective decoupling and layout guidelines.

Features:

- Four Copies of CPU Clock at 66.66 MHz or 60 MHz
- Six Copies of PCI Clock (Sync. CPU Clock/2)
- One copy of USB Clock at 24 MHz (3.3V TTL) (48 MHz can also be used)
- Three copies of Ref. Clock at 14.31818 MHz
- Ref. 14.31818 MHz Xtal Oscillator Input
- Test Mode support
- Package Type SOIC: 28 pin



NOTES:

1. Pins 1 and 26 may be used as outputs for the loop filter by some clock synthesizer vendors.
2. Please refer to your clock synthesizer vendors specifications for complete details.

HXDG4-6

Figure 4-6. Clock Synthesizer

5

Flash Design

CHAPTER 5
FLASH DESIGN

5. Flash Design

5.1 Dual-Footprint Flash Design

New features coming to the PC continue to increase the size of BIOS code, pushing the limits of the 1 Mbit boundary. OEMs have already converted many PC designs to 2 Mbit BIOS and higher, and more will follow.

Since it is difficult to predict when BIOS code will exceed 1 Mbit, OEMs should design motherboards to be flexible. Design in a dual-footprint on the motherboard that accepts both Intel's 1 Mbit flash chips and 2 Mbit boot block chips. This will make the 1M-to-2M transition easier by removing the need for PCB changes to accommodate higher density components.

Intel provides various layout tools to help OEMs design in the dual-footprint. These tools are available from Intel's BBS, WWW (http://www.intel.com/design/flcomp/devtools/flas4.html), and literature distribution center. Look for Application Note AP-623 "Multi-Site Layout Planning with Intel's Boot Block Flash Memory" (Order #: 292178-002). This document provides detailed information on flexible layouts.

Shown below are two of the reference layouts that Intel furnishes to customers. Layouts for plastic dip (PDIP) to TSOP and PSOP are also available. These layouts are described in AP-623 and are available electronically (Gerber and Postscript formats). Note the small amount of extra board space needed to implement the dual-footprint layouts.

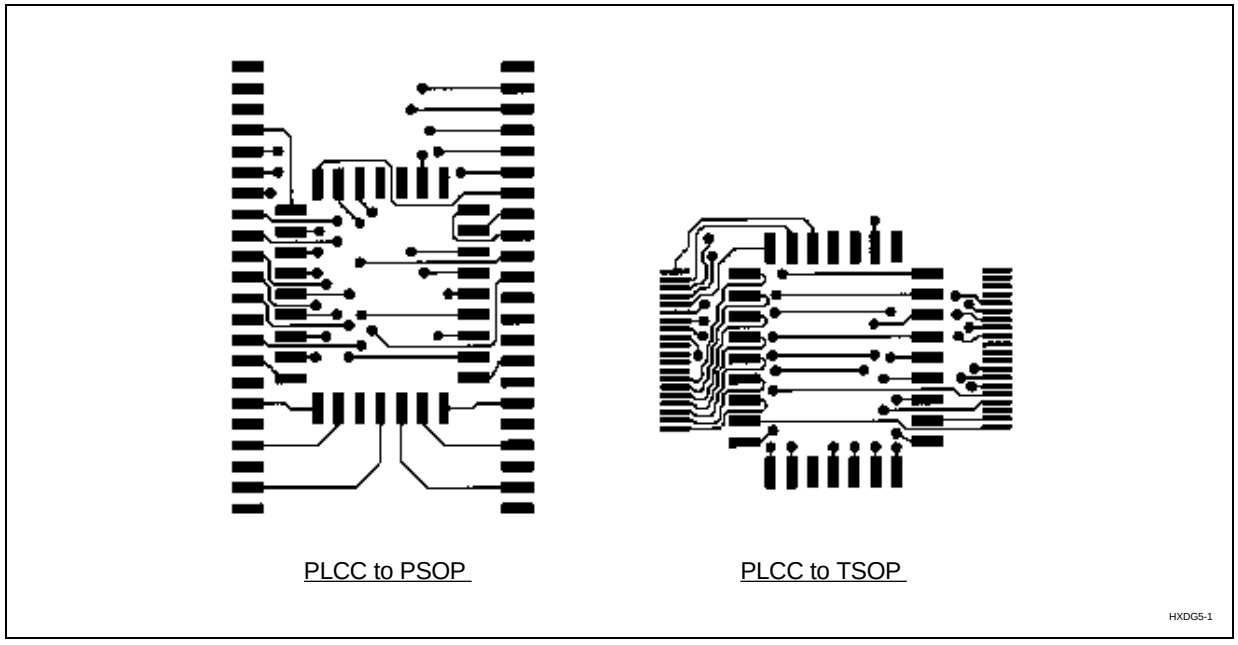


Figure 5-1. Dual Footprint Flash Layouts

5.2 2 Mb Flash Design Considerations

5.2.1 Interfacing the 28F002BX FLASH (2 Mb) with the 430HX PCIset

The following design considerations must be taken into account when Intel's 28F002BX (2 Mb) Flash devices are implemented in Intel 430HX PCIset (430HX) designs. The 2 Mb Flash devices use an Address Transition Detection (ATD) mechanism to improve their performance. When interfacing Flash devices that employ the ATD mechanism, the designer needs to make sure that the address transition time is not more than 10 ns while CE# is active (low). If the address transition time is more than 10 ns invalid data can result on the data bus. When 2 Mb Flash devices are interfaced to the ISA bus they can be exposed to address transitions in excess of 10 ns. Consequently, motherboard designer's need to interface the 2 Mb Flash with the 430HX differently than the 1 Mb Flash.

The 430HX Flexible Motherboard Reference Platform currently implements the 28F001BX (1 Mb) Flash device, which does not employ the ATD circuitry. The current implementation is shown in Figure 5-2.

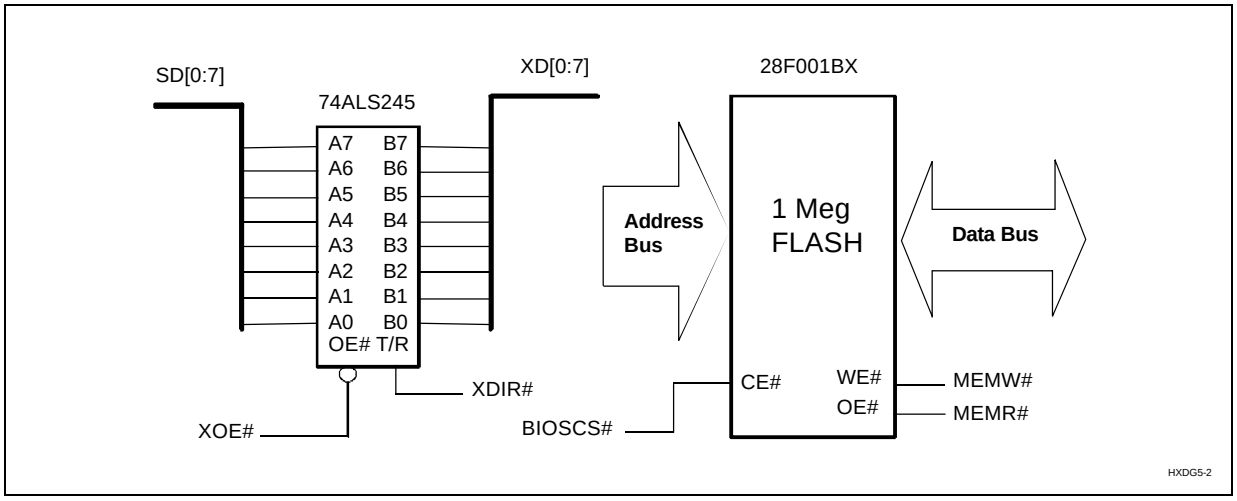


Figure 5-2. Interfacing the 1 Mbit Flash to the 430HX

For 2 Mb Flash implementations that have no other memory devices on the X-Bus, the XOE# signal can be used to drive the Flash CE# input instead of BIOSCS# (Figure 5-3). The implementation shown in Figure 5-3 ensures that the Flash device is only enabled when addresses are stable.

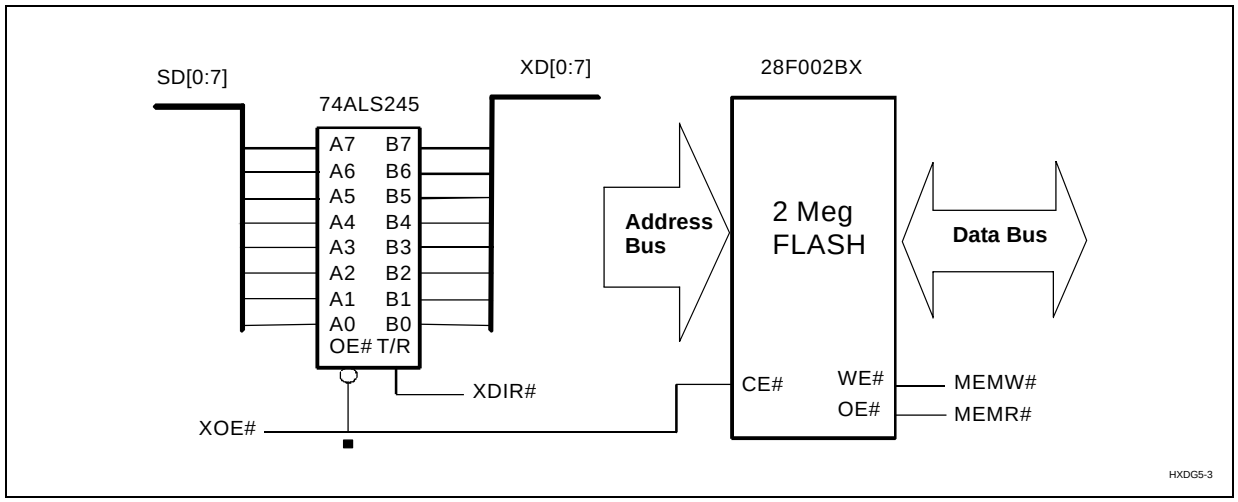


Figure 5-3. Interfacing the 28F002BX to the 430HX

If other devices are present on the X-bus, the CE# input on the Flash should be generated by OR-ing (74ALS32) XOE# with BIOSCS# as shown in Figure 5-4.

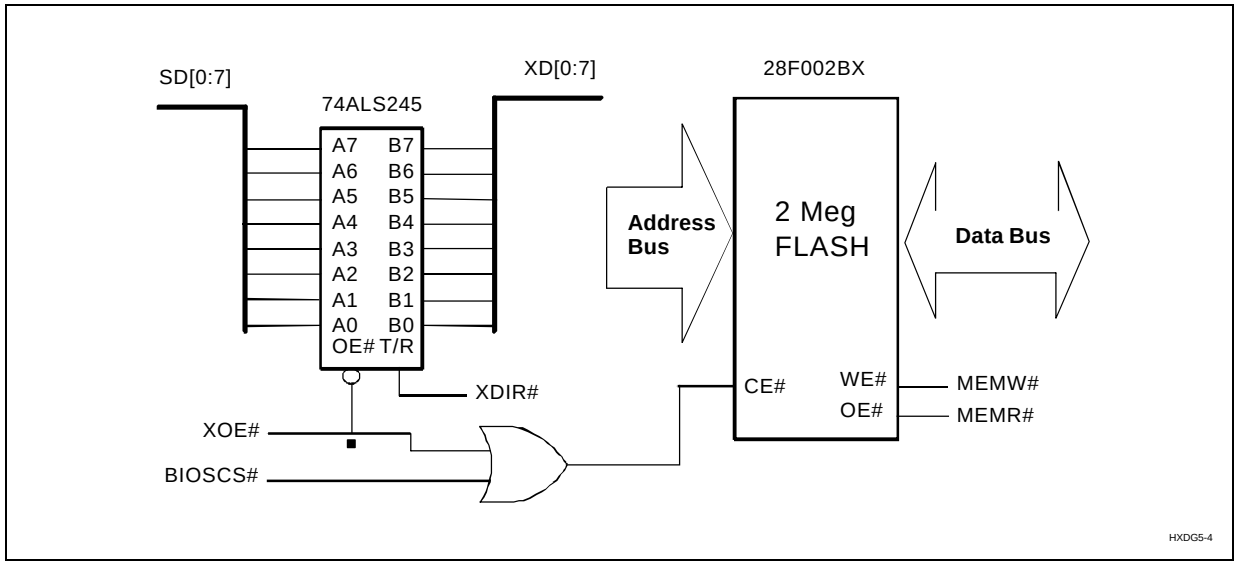


Figure 5-4. Interfacing the 28FC02BX to the 430HX When There are Other Memory Devices On the X-Bus

intel®

6

430HX PCIset Customer Reference Board Schematic Overview

CHAPTER 6
430HX PCISET CUSTOMER REFERENCE BOARD SCHEMATIC OVERVIEW

7. 430HX PCIset Customer Reference Board Schematic Overview

This section provides the schematics, jumper settings, and bill of materials for the Intel 430HX PCIset (430HX) customer reference board.

7.1 Schematics

This document contains schematics for a typical system design using a Pentium® processor and the 430HX. Some of the major features of this design include:

- Supports the Pentium processor at host bus frequencies of 66, 60, and 50 MHz.
- Up to 512 MB of main memory supported.
- Supports enhanced EDO/Hyper Page Mode and Fast Page Mode DRAM.
- Integrated, programmable-strength MAxx buffers.
- 512-KB writeback second level cache.
- Support for the Universal Serial Bus (USB).
- Full support for PCI Rev 2.1 specification.
- Integrated support for two IDE connectors with enhanced PCI Bus Master IDE performance.
- Integrated I/O support with the Advanced Integrated Peripheral (AIP) 82091AA device, floppy disk, one SerialPort, and one ECP Parallel Port.

The rest of this document gives a brief description of the logic and components on each page of the 430HX reference schematics.

Sheet 1: Index

Sheet 1 gives a table of the major active components in the design, and the page number where the device is located.

Sheet 2: Processor

A Pentium processor Socket 7 is shown on Sheet 2. Socket 7 is a superset of Socket 5 and supports all 3.3V Pentium processors. This socket also supports the P55C with split power planes and 2.5V required for the P55C core. Some of the decoupling capacitors for the processor are also shown.

Sheet 3: Clock Synthesizer

Sheet 3 shows the clock synthesizer. Note: R32 and R33 should be installed if the clock generator is an ICS device, and removed if the clock generator is an IMI device. Please note the TXC and CPU host clock connection. This has been done to minimize the host clock skew between the two devices.

Sheet 4: TXC

The 430HX System Controller is shown on Sheet 4. The TXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. This single chip also provides a 64/72 bit data path to main memory. The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC also contains read prefetch and posted write buffers.

Sheet 5: Cacheability Configuration & Tag Ram

Sheet 5 shows the tag RAMs. Also located on Sheet 5 is a table showing the strapping options for the second level cache. An optional mode to extend the DRAM cacheability range to 512 MB has been provided. Note: a pull-up is required on TIO10 for 64 Mb cacheability and pull-down is required for 512M cacheability. If 512M cacheability is not supported, TIO10 must be pulled high.

Sheets 5 and 6: PBSRAMS (Cache)

These two Sheets show the PBSRAMS. The cache memory type must be a pipelined burst SRAM with the global write enable feature. The 430HX also supports a DRAM cache solution. The implementation for a DRAM cache is shown on Sheets 5 and 6.

Sheet 7: DRAM Connectors 0&1

Sheet 7 shows the DRAM connectors (0&1). The primary changes to the DRAM interface include:

- CBR Refresh only
- Larger memory size supported, 8 banks (8 RAS lines) with a maximum of 512 Mbytes
- 64 Mbit technology support
- Enhanced EDO timings 60 ns=5-2-2-2 at 66 MHz for read page hits
- Error detection and Correction or Parity
- Improved paging algorithm
- Programmable strength MA/B[1:0], MA[11:2], MWE buffers (8 or 12 mA)

Although not shown on the schematics, pin 46 of the SIMMs should be pulled low. This is because some DRAM manufacturers have pin 46 as an output enable.

Sheet 8: DRAM Connectors 2&3

Sheet 8 shows the DRAM connectors (1&2). Refer to Sheet 8: DRAM Connectors 0&1 for the improvements of DRAM.

Sheet 9: FLASH BIOS

Sheet 9 shows the Flash BIOS. The flash device is an Intel PA28F002BX 2 MB boot flash. The flash is used for system BIOS. The PIIX3 provides the decode and control during accesses to the flash. Note that XOE- and BIOSCS- are Or'd to generate CE- of the flash part. This logic is necessary when using an Intel 2M Flash and the PIIX3.

Sheet 10: PIIX3

Sheet 10 shows the PIIX3. The PIIX3 is a multi-function PCI device implementing a PCI-to-ISA bridge. JP28 is used to select the PCI clock to SYSCLK divisor. The divisor is 3 if 50 MHz CPU bus (25 MHz PCI) is used and divided by 4 if 66 MHz/60 MHz CPU bus (33/30 MHz PCI) is used. The PIIX3 also integrates the Universal Serial Bus Controller and IDE Controller. Note: an open collector buffer is added to the SYSCLK pin. This is needed so that the leakage current from the four ISA slots SYSCLK pins do not pull the pin high if you have a resistor instead.

Sheet 11: PCI IDE Connectors

Sheet 11 shows the PCI IDE connectors. This IDE implementation supports the fastest IDE ATA mode, mode 4. 74ALS logic is used to reduce noise.

Sheet 12: AIP

Sheet 12 shows the AIP. The Advanced Integrated Peripheral is provided to control the Floppy Disk Connector, two serial port and one parallel port. Note: the resistors on signals PPDIR and DEN- place the AIP in Hardware Basic mode (HWB). Serial and parallel ports must be configured by BIOS routines.

Sheet 13: Serial Port, Floppy Connector, and USB

This design also supports two separate Universal Serial Bus ports.

Sheet 14: Parallel Port

Sheet 15: Keyboard Controller and Keyboard/Mouse Connectors

Sheet 15 shows the 82C42 keyboard controller component. The mouse connector is pinned-out to support “new style” combo mouse devices. The “new” devices default to a 6-pin mini-DIN plug, and use
a converter to connect to a 9-pin DIN socket.

Sheet 16: Battery and Real Time Clock/X-Bus Logic

Sheet 16 shows the battery and RTC circuit and X-Bus logic. Device U1 (74ALS245) is the X-bus buffer. The PIIX3 provides the control to this buffer during accesses to BIOS and RTC.

Sheet 17: Front Panel Switches, Speaker, Hard Disk LED and Power Connector

Sheet 18 and 19: PCI Connectors

The 430HX supports four PCI masters in addition to the PIIX3, IDE connectors, and USB connectors. Below are the assignments for each slot:

Slot#	IDSEL	REQ/GNT	PCI_INTA	PCI_INTB	PCI_INTC	PCI_INTD
J14	AD28	0	PIRQA-	PIRQB-	PIRQC-	PIRQD-
J15	AD29	1	PIRQB-	PIRQC-	PIRQD-	PIRQA-
J16	AD30	2	PIRQC-	PIRQD-	PIRQA-	PIRQB-
J17	AD31	3	PIRQD-	PIRQA-	PIRQB-	PIRQC-

Sheet 20: ISA Connectors

The 430HX supports up to five ISA slots. This design implements three slots.

Sheet 21: PCI and ISA Terminating Resistors

The Pull-up and Pull-down resistors required in the system for the PCI and ISA busses are shown on Sheet 21.

Sheet 22: Power Supply

Sheet 22 shows the switching power supply used to provide 3.3V. JB3 is used for split-plane (P55C) designs.

Sheet 23: Spare Gates

Sheet 24: Decoupling Capacitors

7.2 Jumpers, Connectors, and Valid Memory Configurations

This section contains jumper settings for 82430HX Customer Reference Board.

7.2.1 Jumper Settings

Default settings in ***Italics*** type.

Table 7-1. CPU Core/Bus Frequency Ratio (Jumper JB2)

Core/Bus Ratio	Jumper Position
3/2	1-3, 2-4
2/1	***3-5, 2-4***
3/1	1-3, 4-6
5/2	3-5, 4-6

Table 7-2. CPU Bus Frequency Select (Jumpers J30, J29, J25 & J28)

CPU Bus Frequency	Jumper J30 Position	Jumper J29 Position	Jumper J25 Position	Jumper J28 1-2 Position
50 MHz	2-3	2-3	don't care	OUT
60 MHz	2-3	1-2	1-2	IN
66 MHz	***1-2***	***2-3***	***2-3***	***IN***

Table 7-3. CPU Voltage Select (Jumper J26)

CPU Voltage	Jumper 1-2 Position
STD	***OUT***
VRE	IN

Table 7-4. CPU Select (Jumpers J27 & JB3)

CPU	Jumper JB3 Position
P54C	***1-2, 3-4, 5-6, 7-8***
P55C	NONE

Table 7-5. DRAM Voltage Select (Jumper JB1)

DRAM Voltage	Jumper Position
5 Volts	***1-3, 2-4***
3.3 Volts	3-5, 4-6

Table 7-6. BIOS Mode Select (Jumper J12)

Mode	Jumper Position
Non-Plug n Play	2-3
Plug n Play	***1-2***

Table 7-7. BIOS Mode Select (Jumper J11)

Mode	Jumper Position
Normal	***2-3***
Recovery	1-2

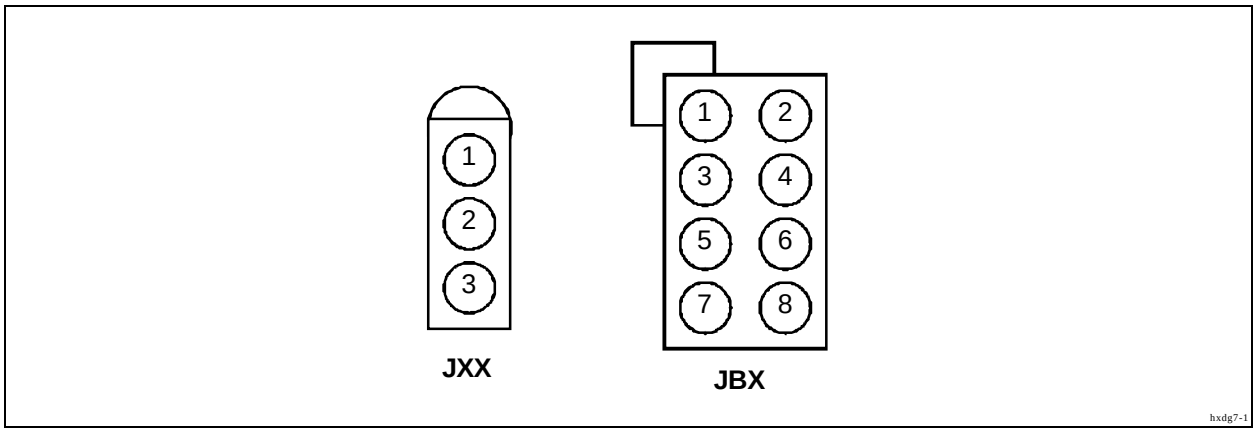
Table 7-8. Password Clear (Jumper J4)

Password Clear	Jumper Position
Normal	***Out***
Clear Password	In

Table 7-9. CMOS Clear (Jumper J24)

CMOS Clear	Jumper Position
Normal	***Out***
Clear CMOS	In

7.2.2 Jumper Header Pin Orientations



7.2.3 Connector Guide

Connector	Function
J1	PS/2 Mouse Connector
J2	Keyboard Connector
J3	Flash Boot Block Program Enable
J5	3.3V PCI Power Connector
J6, J7, J8	ISA Connectors
J9	Parallel Port Connector
J10	Serial Port "Com1" Connector
J13, J22	Main Power Connector
J14, J15, J16, J17	PCI Connectors
J18	Serial Port "Com0" Connector
J19	USB Port Header
J20	Primary IDE Connector
J21	Floppy Connector
J23	Secondary IDE Connector
J31	External SMI Connector
J32	Hard Drive LED Connector
J33	Power LED/Keylock Connector
J34	+12V Fan Connector
J35	Reset Switch Connector
J36	Speaker Connector

7.2.4 Valid Memory Configurations

Bank 0 U21	Bank 0 U20	Bank 1 U19	Bank 1 U18	Total
1Mx36	1Mx36			8M
1Mx36	1Mx36	2Mx36	2Mx36	24M
1Mx36	1Mx36	4Mx36	4Mx36	40M
1Mx36	1Mx36	8Mx36	8Mx36	72M
2Mx36	2Mx36			16M
2Mx36	2Mx36	4Mx36	4Mx36	48M
2Mx36	2Mx36	8Mx36	8Mx36	80M
4Mx36	4Mx36			32M
4Mx36	4Mx36	4Mx36	4Mx36	64M
4Mx36	4Mx36	8Mx36	8Mx36	96M
8Mx36	8Mx36			64M
8Mx36	8Mx36	8Mx36	8Mx36	128M

7.2.5 Stuffing Options

Table 7-10. ICS 9169 clock generator.

Remove	Add
U28: ICS9159-02S	U28: ICS9169-01S
R72, R75: 22Ω resistors	U26: 74ALS74AS
	R70: 10 kΩ resistor
	R74, R77: 22Ω resistors

Table 7-11. 3.3V 512 KB L2 cache fixed.

Remove	Add
R95, R94, R101, R106: 4.7 kΩ resistors	U29, U32: 32KX32PBSRMPTQ-GW-8
	U25: 32KX8SRAMSN-15
	R65: 0Ω resistor
	RP73: 1 kΩ resistor module
	R55: 220Ω resistors (already in most boards)
	R84, R96, R103, R107: 4.7 kΩ resistors

Table 7-12. New type Pburst Cache.

Remove	Add
R90: 4.7 kΩ resistor	R82: 100 kΩ resistor

Table 7-13. 2 Mbit Flash Eprom

Remove	Add
U7: 28F001BX-T150	U6: 28F002BXTSOP-T120
U7: SK32DIP	R6: 0Ω resistor
R9: 0Ω resistor	

Table 7-14. 12887 RTC

Remove	Add
J24: JP2	R38: 10 kΩ resistor

7.3 Bill of Materials

This section contains a Bill Of Materials (BOM) for 430HX Customer Reference Board.

Table 7-15. Bill Of Materials

Part Number	Package Type	Description	Qty	Reference Design
1N4148SOT23	SOT23	Diode, 1N4148	2	D1, D3
1N5820	TH	Schottky Barrier Rect.	1	D2
28F001BX-T150	DIP32	Flash Mem., 1 Mbit, w/ boot block, 150 ns	1	U7
2N3904SOT23	SOT	3904 Transistor	2	Q5, Q8
2N3906SOT23	SOT	3906 Transistor	1	Q6
32KX32PBSRMPTQ-GW-8	QFP100	32KX32 Pipelined Burst SRAM, GWE, 8 ns	2	U22, U31
32KX8SRAMSN-15	SOJ28	32Kx8 SRAM (15 ns)	1	U24
6021PB	TH	Heat Sink, stake-on for TO-220	1	HS1
7406S	SOIC14	IC, Hex Inverters, open collector	1	U4
7407S	SOIC14	IC, Hex buffer, open collector	1	U27
74ALS00S	SOIC14	IC, Quadruple 2-input NAND gate	1	U12
74ALS08S	SOIC14	IC, Quadruple 2-input AND gate	1	U11
74ALS245S	SOIC20	IC, Octal tristate transceiver	3	U1, U14, U17

Part Number	Package Type	Description	Qty	Reference Design
74ALS32S	SOIC14	IC, Quadruple 2-input or gate	1	U16
74HCT14S	SOIC14	IC, Hex Schmitt trigger inverters	1	U2
74LS125S	SOIC14	IC, Quadruple tristate buffer	1	U3
82091AA	PQFP100	Advanced Integrated Peripheral	1	U8
82372SB	PQFP208	Triton PCI ISA/IDE Accelerator III	1	U15
8242PCPL	PLCC44	Keyboard Controller; MultiKey/42 Firmware	1	U5
82439HX	BGA324	Intel TXC (Triton II Xcelerated Controller)	1	U23
C100CS00GE	SM0603	Cap., cer., 10 pF, 50V, 20%	2	C145, C146
C101CS00GE	SM0603	Cap., cer., 100 pF, 50V, 20%	16	C21, C25, C29, C31, C32, C38, C42, C45, C49, C53, C55, C56, C63, C66, C74, C75
C102CS00GE	SM0603	Cap., cer., 0.001 µF, 50V, 20%	13	C4, C89, C90, C109, C114, C121, C124, C133, C165, C166, C197, C202, C203
C103CS00EE	SM0603	Cap., cer., 0.01 µF, 25V, 20%	1	C222
C103CS00EM	SM0603	Cap., cer., 0.01 µF, 25V, +80%/-20%	12	C78, C80, C92, C93, C94, C101, C106, C108, C126, C128, C138, C226
C104CS00DM	SM0603	Cap., cer., 0.1 µF, 16V, +80/-20%	40	C1, C2, C3, C5, C6, C10, C15, C19, C26, C33, C34, C35, C43, C44, C57, C58, C59, C60, C67, C68, C69, C70, C76, C77, C81, C87, C88, C91, C95, C96, C97, C98, C99, C100, C102, C103, C104, C105, C107, C110,

Part Number	Package Type	Description	Qty	Reference Design
C104CS00DM	SM0603	Cap., cer., 0.1 µF, 16V, +80/-20%	34	C111, C112, C113, C115, C116, C117, C118, C120, C122, C123, C127, C129, C130, C135, C136, C137, C139, C140, C141, C142, C143, C144, C147, C150, C151, C152, C153, C154, C155, C156, C158, C159, C160, C161
C104CS00DM	SM0603	Cap., cer., 0.1 µF, 16V, +80/-20%	11	C162, C163, C164, C170, C171, C172, C173, C176, C204, C220, C223
C104CS00EM	SM0603	Cap., cer.,0.1 µF, 25V, +80/-20%	5	C14, C36, C46, C50, C224
C105CS01DM	SM0805	Cap., cer., 1.0 µF, 16V, +80/-20%	25	C174, C177, C178, C179, C180, C186, C187, C188, C193, C194, C195, C196, C199, C200, C201, C205, C206, C207, C209, C212, C213, C217, C218, C219, C221
C105CS02DM	SM1206	Cap., cer., 1.0 µF, 16V, +80/-20%	3	C131, C168, C225,
C106ES09DE	SM4mm	Cap., elec., 10 µF, 16V, 20%	9	C7, C8, C11, C39, C47, C86, C119, C125, C134
C106ES11EE	SM5mm	Cap., elec., 10 µF, 25V, 20%	2	C22, C23
C107TS05CE-LE	SM7343H	Cap., tant., 100 µF, 10V, 20%, .125 ESR	8	C9, C132, C148, C175, C181, C192, C208, C211
C121CS00GE	SM0603	Cap., cer., 120 pF, 50V, 20%	1	C184
C181CS00GE	SM0603	Cap., cer., 180 pF, 50V, 20%	17	C16, C20, C24, C27, C28, C30, C37, C40, C41, C48, C51, C52, C54, C62, C64, C65, C73
C224CS01GE	SM0805	Cap., cer., 0.22 µF, 50V, 20%	1	C149
C227TS05CE-LE	SM7343H	Cap., tant., 220 µF, 10V, 20%, .125 ESR	8	C157, C169, C182, C183, C185, C191, C214, C215
C332CS00GE	SM0603	Cap., cer., 3300 pF, 50V, 20%	1	C190

Part Number	Package Type	Description	Qty	Reference Design
C470CS00GE	SM0603	Cap., cer., 47 pF, 50V, 20%	4	C71, C79, C83, C85
C471CS00GE	SM0603	Cap., cer., 470 pF, 50V, 20%	11	C12, C13, C17, C18, C61, C72, C82, C84, C167, C198, C210
C472CS00GE	SM0603	Cap., cer., 0.0047 µF, 50V, 20%	1	C216
C501CS00GE	SM0603	Cap., cer., 500 pF, 50V, 20%	1	C189
CN120ED05B	TH	Conn., 120 pin, PCI	4	J14, J15, J16, J17
CN16BGD10B	TH	Conn., 8x2 pin header	1	J19
CN6FLU15C	TH	Conn., 6 pin, AT power plug	3	J5, J13, J22
CN6MDF10B	TH	Single PS2 style keyboard ms connector	2	J1, J2
CN98ED10B	TH	Conn., 98 pin card edge	3	J6, J7, J8
CNK25BGD10BA	TH	Conn., 13x2 pin header; key pin 26	1	J9
CNK33SH10B	TH	Conn., 17x2 pin header; key pin 5, shrouded	1	J21
CNK39SH10B	TH	Conn., 20x2 pin header; key pin 20, shrouded	2	J20, J23
CNK3BGS10B	TH	Conn., 4x1 pin header; key pin 2	1	J36
CNK3BGS10BA	TH	Conn., 4x1 pin header; key pin 3	1	J32
CNK4BGS10B	TH	Conn., 5x1 pin header; key pin 2	1	J33
CNK9BGD10B	TH	Conn., 5x2 pin header; key pin 10	2	J10, J18
DS12887A	DIP24	Real Time Clock w/Battery, CMOS RAM	1	U13
FBS01K	SM0805	Ferrite bead (ACT material K)	4	L3, L4, L5, L6
FBS01L	SM0805	Ferrite bead (ACT material L)	2	L2, L9
FBS04B	SM1812	Ferrite bead (ACT material B)	6	L1, L7, L8, L10, L11, L12
FUSEP1253S09D	SM9466	Poly Fuse 1.25A hold, 15V	3	F1, F2, F3
GD75232SOP	SOP20	RS 232 Transceiver 5 receivers, 3 drivers	2	U9, U10

HR-5A2R2K	TH	2.2 µH, 5A inductor	1	L14
Part Number	**Package Type**	**Description**	**Qty**	**Reference Design**
ICS9159-02S	SOIC28	Clock Generator, ICS9159-02	1	U28
INSILPAD-TO220	TO-220	Silicone insulator w/thermally conductive filters	1	HS1
IRFZ40	TO-220	N-Channel FET, 50A, 0.028	1	Q3
JB3	TH	3x2 pin header connector	2	JB1, JB2
JB4	TH	4x2 pin header connector	1	JB3
JP1	TH	1x1 pin header connector	1	J3
JP2	TH	2x1 pin header connector	6	J4, J24, J28, J31, J34, J35
JP3	TH	3x1 pin header connector	6	J11, J12, J25, J26, J29, J30
L152S06D	SM1210	1.5 µH SMT inductor	1	L13
LOCKNUT-4-40	HDWR	4-40 Locknut	1	HS1
LT1431CS	SOIC8	Regulator, Adjustable Shunt, .4%	1	Q1
LTC1266CS	SOIC16	Regulator, synchronous stepdown	1	U30
PCB		Printed Circuit Board	1	PCB1
R0000CS00SC	SM0603	Res., 0, 5%, 1/16W	5	R9, R53, R80, R109, R155
R003SCS04HC	SM2010	Res., 0.03, 5%, 1/2W	2	R121, R123
R0220CS00SC	SM0603	Res., 22, 5%, 1/16W	28	R5, R32, R33, R34, R35, R40, R42, R44, R45, R46, R50, R61, R62, R63, R64, R66, R67, R68, R69, R71, R72, R73, R75, R76, R78, R79, R116, R153
R0300CS00SC	SM0603	Res., 30, 5%, 1/16W	4	R19, R20, R21, R26
R0330CS00SC	SM0603	Res., 33, 5%, 1/16W	1	R7
R0470CS00SC	SM0603	Res., 47, 5%, 1/16W	4	R28, R29, R47, R49
R0680CS01EC	SM1206	Res., 68, 5%, 1/8W	2	R126, R127
R1000CS00SC	SM0603	Res., 100, 5%, 1/16W	3	R117, R118, R124
R1001CS00SC	SM0603	Res., 1K, 5%, 1/16W	1	R22

Part Number	Package Type	Description	Qty	Reference Design
R1002CS00SC	SM0603	Res., 10K, 5%, 1/16W	11	R8, R12, R13, R15, R16, R17, R37, R41, R52, R57, R92
R1271MS03TZ	SM0805	Res., 1.27K, 0.1%, 1/10W	1	R105
R1501MS03TZ	SM0805	Res., 1.50K, 0.1%, 1/10W	1	R108
R1872MS03TA	SM0805	Res., 18.7K, 1%, 1/10W	1	R85
R2200CS00SC	SM0603	Res., 220, 5%, 1/16W	16	R1, R2, R3, R4, R11, R23, R24, R25, R27, R36, R51, R58, R59, R60, R83, R122
R2201CS00SC	SM0603	Res., 2.2K, 5%, 1/16W	1	R128
R3300CS00SC	SM0603	Res., 330, 5%, 1/16W	12	R54, R56, R86, R91, R99, R102, R104, R110, R114, R115, R130, R131
R3302CS00SC	SM0603	Res., 33K, 5%, 1/16W	1	R112
R4701CS00SC	SM0603	Res., 4.7K, 5%, 1/16W	15	R18, R43, R87, R88, R89, R90, R93, R94, R95, R97, R98, R100, R101, R106, R111
R4702CS00SC	SM0603	Res., 47K, 5%, 1/16W	1	R125
R5601CS00SC	SM0603	Res., 5.6K, 5%, 1/16W	2	R30, R31
R8201CS00SC	SM0603	Res., 8.2K, 5%, 1/16W	3	R10, R14, R154
R9100CS01EC	SM1206	Res., 910, 5%, 1/8W	3	R119, R120, R129
R9650MS03TZ	SM0805	Res., 965, 0.1%, 1/10W	1	R113
RI100S09SC	SM3216	Res., Block., 10x4, iso., 5%, 1/16W	3	RP66, RP67, RP68
RI102S09SC	SM3216	Res., Block., 1Kx4, iso., 5%, 1/16W	8	RP4, RP7, RP8, RP9, RP15, RP42, RP49, RP60
RI103S09SC	SM3216	Res., Block., 10Kx4, iso., 5%, 1/16W	23	RP1, RP5, RP6, RP10, RP14, RP16, RP17, RP18, RP21, RP24, RP27, RP29, RP31, RP40, RP45, RP52, RP57, RP58, RP59, RP61, RP63, RP70, RP74

RI220S09SC	SM3216	Res., Block., 22x4, iso., 5%, 1/16W	8	RP20, RP22, RP23, RP25, RP43, RP46, RP50, RP54
RI272S09SC	SM3216	Res., Block., 2.7Kx4, iso., 5%, 1/16W	10	RP12, RP26, RP28, RP30, RP33, RP34, RP38, RP39, RP64, RP65
Part Number	**Package Type**	**Description**	**Qty**	**Reference Design**
RI330S09SC	SM3216	Res., Block., 33x4, iso., 5%, 1/16W	8	RP2, RP11, RP13, RP32, RP36, RP37, RP41, RP62
RI331S09SC	SM3216	Res., Block., 330x4, iso., 5%, 1/16W	2	RP35, RP56
RI472S09SC	SM3216	Res., Block., 4.7Kx4, iso., 5%, 1/16W	10	RP3, RP44, RP47, RP51, RP53, RP55, RP69, RP71, RP72, RP75
RI562S09SC	SM3216	Res., Block., 5.6Kx4, iso., 5%, 1/16W	2	RP19, RP48
SCREW-4-40-.33	HDWR	4-40 Panhead Screw, 1/3	1	HS1
SHUNTS		Jumper shunts	6	J11, J12, J25, J26, J29, J30
SI4410DY	SOIC8	N-Channel Enhancement-Mode MOSFET	1	Q2
SI9410DY	SOIC8	N-Channel Enhancement-Mode MOSFET	1	Q4
SK321PGAZIF	PGA321	ZIF Socket for Pentium processor (socket 7)	1	U33
SK72SIMVML	TH	Socket, 2MX36 SIMM, single, vert., ml	4	U18, U19, U20, U21
TL431ACS	SOIC8	Regulator, Adjustable Shunt, A version, 1%	1	Q7
Y14318186B2E-18	TH	Xtal, 14.31818 MHz, 49-U pkg, 18 pF, 20 ppm	1	Y1