21554 PCI-to-PCI Bridge

Specification Update

September 2000

Notice: The 21554 may contain design defects or errors known as errata. Characterized errata that may cause the 21554's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278219-003

Contents

Revision History

Date	Version	Description
9/15/00	003	Modified errata number 4 wording. Added specification change to PBGA package dimensions for coplanarity maximum value.
04/30/99	002	Removed related information section. In related documents section updated document titles and order numbers.
08/20/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21554 PCI-to-PCI Bridge for Embedded Applications Product Preview Datasheet	278089-001
21554 PCI-to-PCI Bridge for Embedded Applications Hardware Reference Manual	278091-001

Nomenclature

Errata are design defects or errors. These may cause the 21554's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 21554 PCI-to-PCI Bridge product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	AA	#	#			
1	x			11	Eval	Hang condition detected when CLS=4 and the 64-bit interface is enabled.
2	x			11	Eval	Posted write address/data corruption subsequent to midburst PW Target Abort.
3	x			12	Eval	Arbiter initialization issue when Arbiter Control<9>=0
4	x			12	Eval	Incorrect address driven on AD<63:32> during DAC second address phase.
5	x			13	Eval	VPD has incorrect Capability ID.
6	X			13	Eval	Some PCI-related signals are not reset asynchronously.
7	X			13	Eval	s_rst_l not asserted asynchronously.

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	AA	#			
1	X		15	Doc	VDP ECP ID incorrectly identified.
2	X		15		PBGA package dimensions for coplanarity changed from maximum value 0.15 mm to a maximum value of 0.2 mm.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	AA	#	#			
1	X			16	Doc	$I_2$0 Post_List and Free_List alignments.
2	X			16	Doc	Indirect transmission generation limitations.
3	X			16	Doc	Initialization without local processor and serial preload.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	EC-R8WGB-TE	17	Doc	Section 6.2.2.17
2	278089-001	17	Doc	Section 6.0, Table 31, 304-Point 2-Layer PBGA Package Dimensions
3	278089-001	17	Doc	Section 4.0, Instruction Register

Identification Information

Markings

21554

- This document contains errata for the 21554 PCI-to-PCI Bridge product. The 21554 device revision that is affected by this errata can be identified as order number 21554-AA.

Errata

1. Hang condition detected when CLS=4 and 64-bit interface is enabled.

Problem: The 21554 stops delivering and accepting posted memory writes in one direction, signaling target retry forever when the following conditions occur:

- Cache line size is 4 dwords (primary CLS for downstream writes, or secondary CLs for upstream writes).
- Memory Write Disconnect Control = 0.
- Bridge has partially delivered a posted write in that direction. For example, 2 dwords of a 4-dword write have been delivered.
- The posted write queue for that direction has room for exactly an address and 6 dwords.
- The posted write queue contains writes of ONLY these lengths (in dwords):

  1,2, 5,6, 9,10, 13,14, 17,18, 21, 22, 25, 26, 29, 30, 33, or 34.
- The 21554 accepts a 64-bit memory write in the same direction with no IRDY# slips. The 21554 disconnects after 6 dwords.

Implication: The system will hang when this condition occurs.

Workaround: Either of the following actions provide workarounds for this problem:

- The 64-bit interface should not be enabled when the cache line size for that interface is set to 4 dwords (or vice versa).
- The Memory Write Disconnect Control bit should be set to 1. This disconnects all writes at cache line boundaries (4 dwords in this case).

Status: For the steppings affected, see the Summary Table of Changes.

2. Posted write address/data corruption subsequent to mid-burst PW target abort.

Problem: Posted memory write addresses and data may be corrupted when the following conditions occur:

A posted write is forwarded with these properties:

- Accepted and delivered in 32-bit data mode.
- Address is 64-bit aligned.
- Length is exactly CLS + 1.

As the posted write is being delivered, a Target Abort with no target stall cycles is returned after an EVEN number of dwords, total, have been delivered to the target. Note that some data may have been accepted in earlier transactions where the target disconnected the 21554. These count toward the total that must be even.

Additionally, the 21554 must deassert FRAME# due to a MLT timeout during the same cycle as the target abort is returned. That is, FRAME# is deasserted at the same time TRDY# and DEVSEL# deassert and STOP# asserts.

Implication: Data integrity may be compromised after a target abort when the above conditions are met.

Workaround: None. However, target abort is a serious error and should not occur in a properly functioning system. It may be desirable to enable SERR# assertion for Target Aborts during Posted Writes.

Status: For the steppings affected, see the Summary Table of Changes.

3. Arbiter initialization issue when Arbiter Control <9> = 0

Problem: The arbiter may hang if all of the following are true:

- The Arbiter Control configuration register bit <9> is set to 0 through serial pre-load.
- After reset, the first master to request the secondary bus is not the 21554.

If the hang occurs, the arbiter can be kicked out of the hang state by either of the following:

- Writing the Secondary Reset bit to a 1, then a 0.
- Causing the 21554 to request the secondary bus by forwarding or generating a downstream transaction.

The Arbiter Control register assigns each secondary bus master to a high or low priority ring. Arbiter Control bit <9> is assigned to the 21554. The reset value of Arbiter Control <9> is 1. See Section 12.2.1 “Secondary Bus Arbitration Using the Internal Arbitor” and Section 6.2.5.5 “Arbiter Control Register” in the *DIGITAL Semiconductor 21554 PCI-to-PCI Bridge for Embedded Applications Hardware Reference Manual.*

Implication: The secondary bus will hang if the above conditions are true. The system may not boot.

Workaround: Do not set the Arbiter Control <9> to 0 during serial pre-load. Arbiter Control <9> may be set to 0 by either the host or local processor after serial pre-load.

Status: For the steppings affected, see the Summary Table of Changes.

4. Incorrect address driven on AD<63:32> during DAC second address phase

Problem: The 21554 may drive incorrect values on AD<63:32>, C/BE#<7:4> and PAR64 during the second address phase of a dual-address cycle transaction; the correct parity is maintained on PAR64. This error occurs when the 21554 initiates a transaction containing a 64-bit address using the 64-bit transaction protocol (REQ64# asserted).

Implication: This can affect targets that decode the high 32-bits of address on the upper 32-bits of the AD bus and relies on these signals remaining stable during the second address phase. Note that the high address, parity, and command are driven correctly on AD<63:32> during the first address phase, and on AD<31:0> during the second address phase (along with correct values on C/BE#<3:0> and PAR). Although PAR64 might be driven to an incorrect value during the second address phase, it is always valid with respect to the value of AD<63:32>.

Workaround: None, although it should be noted that all Intel PCI sets that support 64-bit PCI (e.g., Intel 840, Intel 82450NX, Intel Profusion) and Intel 64-bit PCI networking products (e.g., PRO1000 Gigabyte adapters) will not generate any failures as a result of this errata.

Status: For the steppings affected, see the Summary Table of Changes.

5. VPD has incorrect Capability ID

Problem: The VPD Capability ID incorrectly reads as 04h. The proper value is 03h. See Section 6.2.2.17 “VDP ECP Register” in the *DIGITAL Semiconductor 21554 PCI-to-PCI Bridge for Embedded Applications Hardware Reference Manual*.

Implication: Software looking for a capability ID of 3h for VPD will not identify this feature in the 21554. Software looking for a capability ID of 4h for Slot Numbering Capabilities may identify the 21554 as supporting this feature, though it does not.

Workaround: None.

Status: For the steppings affected, see the Summary Table of Changes.

6. Some PCI-related signals are not reset asynchronously

Problem: The following PCI related signals are not asynchronously reset during power up:

- p_inta_l
- s_inta_l
- p_serr_l
- s_serr_l
- p_enum_l
- l_stat
- p_pme_l

These signals will reset as soon as p_clk is applied during reset. However, it is possible that after power up, while reset is asserted and p_clk is inactive, any of these signals may assert.

Implication: This is primarily an issue when the 21554 is used on Compact PCI boards that are hot swap capable. Even a 1-cycle assertion of p_serr_l when a card using the 21554 is inserted into a live system may cause the system to crash. If the 21554 nevers powers up in an already operating system, then it may not be an issue.

Workaround: FETs gated with p_rst_l may be used as an isolation mechanism for any of these signals determined to be problematic.

Status: For the steppings affected, see the Summary Table of Changes.

7. s_rst_l not asserted asynchronously

Problem: Secondary PCI reset, s_rst_l, is not asserted asynchronously when p_rst_l is asserted and p_clk is inactive. s_rst_l is asserted as soon as p_clk is applied while p_rst_l is asserted.

Implication: The local sub-system will not be reset until a primary clock is supplied. This may be an issue when the secondary clock is supplied independently, where the secondary clock is could start operating before the secondary devices have been reset.

Workaround: An external hardware workaround may be implemented where the s_rst_l signal is isolated during power-up reset and secondary reset applied externally.

Status: For the steppings affected, see the Summary Table of Changes.

Specification Changes

1. VPD ECP ID

ITEM: The Enhanced Capabilities ID for the Vital Product Data (VPD) feature is incorrectly specified as 04h. The correct value is 03h.

2. PBGA Package Dimensions for coplanarity changed from maximum value 0.15 mm to maximum value 0.2 mm.

Per PCN notification 961, the 304-point 2-layer PBGA package dimensions for symbol aaa, coplanarity, are changed from maximum value 0.15 mm to maximum value 0.2 mm.

Specification Clarifications

1. I_2O Post_List and Free_List Alignments

ITEM: The I_2O MFA lists stored in local memory must each be located on an aligned address boundary. The alignment granularity is the same as the size of the list. The automatic increment/decrement/wrap functions of the head and tail pointer for the list assume this alignment. For example, if the I_2O list is 4 K entries (4 K dwords or 16 KB) deep, then the list must be located in local memory starting on an aligned 4 K dword or 16 KB boundary. Failure to align the I_2O lists will result in pointer wrap errors.

The I_2O lists are:

- I_2O Inbound Post_List
- I_2O Inbound Free_List
- I_2O Outbound Post_List
- I_2O Outbound Free_List

2. Indirect Transaction Generation Limitations

ITEM: The 21554 does not respond to a transaction generated by itself, whether it is forwarded through the forwarding BARs or generated using the Indirect Transaction Generation mechanism. For example, the host processor cannot use Downstream Indirect Configuration Transaction feature to access 21554 registers from the secondary bus. It is recommended that a general bus scan not be used with the Indirect Configuration Transaction Generation mechanism unless this is taken into account.

3. Initialization without Local Processor and Serial Preload

ITEM: It is not recommended to use the 21554 in an application that does not use serial ROM pre-load or local processor initialization (i.e., host processor initialization only). The address setup configuration registers for the Base Address Registers are accessible from serial pre-load or secondary bus only. By using only a host processor for initialization from the primary side, all forwarding BARs are disabled and no memory transactions can be forwarded across the 21554.

Documentation Changes

1. Section 6.2.2.17

ITEM: The Enhanced Capabilities ID for the Vital Product Data (VPD) feature is incorrectly specified in Table 6-21 as 04h. The correct value is 03h.

Table 6-21. Vital Product Data (VPD) ECP Register

Bit	Name	R/W	Description
7:0	VPD ECP ID	R	VPD Enhanced Capabilities Port ID. Read only as 03h to identify these ECP registers as VPD registers.

Note: The *DIGITAL Semiconductor 21554 PCI-to-PCI Bridge for Embedded Applications Hardware Reference Manual* (EC-RW8GB-TE) is being converted to the *21554 PCI-to-PCI Bridge for Embedded Applications Hardware Reference Manual* (278091-001). This document change will be included in the new Intel document.

2. Section 6.0, Table 31, 304-Point 2-Layer PBGA Package Dimensions

The maximum value for symbol aaa, dimension coplanarity, has been changed from 0.15 mm to a value of 0.2 mm.

3. Section 4.0, Instruction Register

The first sentence is changed to read:

The 4-bit instruction register selects the test mode and features.