Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R)

Datasheet

August 2000

Order Number: 298022 - 002

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Revision History

Rev.	Description	Date
-001	• Initial Release	January 2000
-002	• Removed support for 2 MRH-Rs per MCH channel. MCH only supports one MRH-R per channel. • Minor Edits for clarity	August 2000

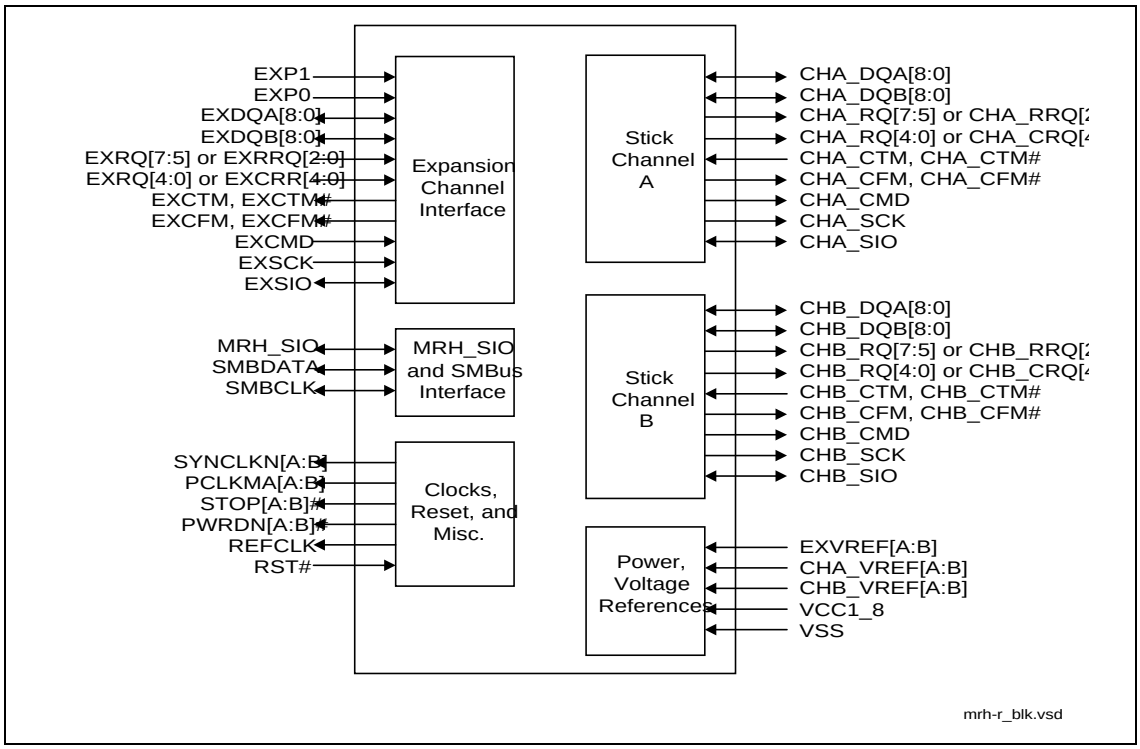
Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R)

Product Features

- Supports two Direct RDRAM ‘stick’ channels and one ‘expansion’ channel.
- Pass through architecture for Read and Write accesses.
- Supports 64Mbit, 128Mbit, and 256Mbit RDRAM technologies.
- Maximum Memory Array Sizes: Up to 1 GB using 64Mbit RDRAM devices, 2 GB using 128Mbit RDRAM devices, and 4 GB using 256Mbit RDRAM devices.
- Integrates logic to do Nap Exit, Powerdown Exit, Refresh, and Post-Refresh Precharge on a channel upon request from the Memory Controller Hub (MCH).
- Integrates logic to do ‘expansion’ channel and ‘stick’ channel current calibration
- Support of 2 wire RSL sideband channel to support up to two MRH-Rs per ‘expansion’ channel in the memory array.
- Integrates control of 2 external DRCG clock generators.
- 6 rclk round trip delay for RSL signals through the MRH-R
- Support of RDRAM CMOS signals to facilitate initialization, read/write of registers and Nap and Powerdown exits.
- MRH-R internal registers accessed through CMOS signal interface
- Integrated System Management Bus (SMB) controller to read and write data from/to SPD EEPROM on the RIMMs
- 324 pin miniBGA

The Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Simplified Block Diagram



1. Overview

1.1. System Architecture

The ‘Expansion’ channel is the interconnect between the MCH and the MRH-R. The MRH-R component provides the capability to support multiple Direct RDRAM channels off each ‘expansion’ channel of a MCH.

As an example, the Intel® 82840 MCH supports one MRH-R on each of its ‘expansion’ channel buses for a maximum of two MRH-Rs in an Intel® 840 chipset system memory array.

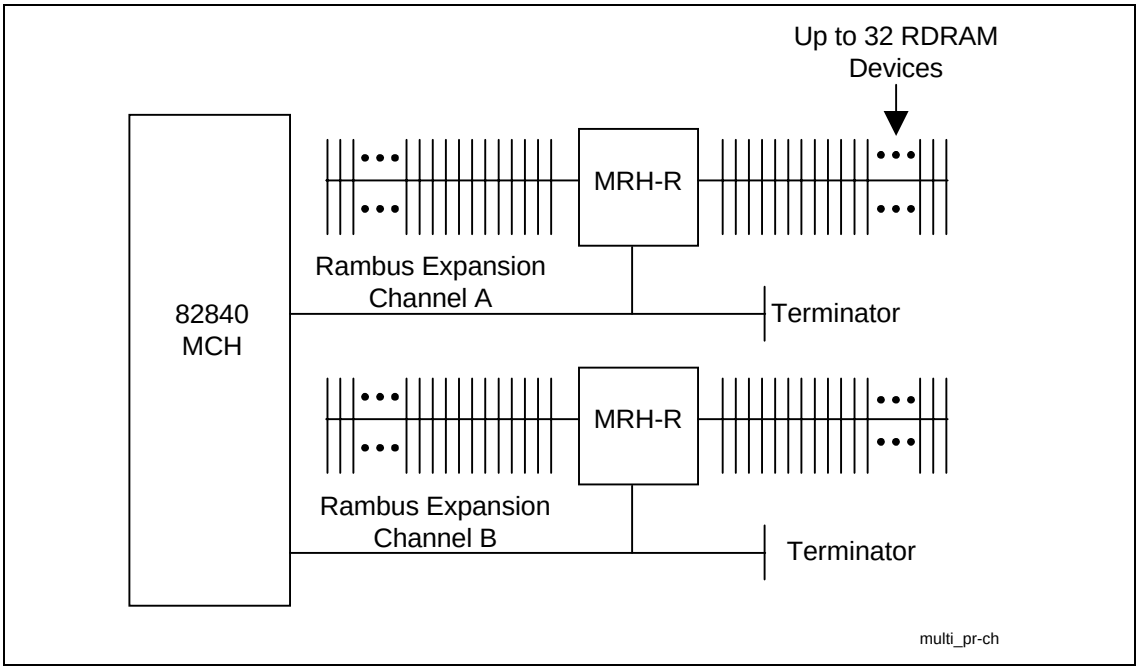
Note: Future Intel chipsets will support the MRH-Rs as well.

Table 1. Maximum Memory Support

RDRAM Technology	Max Memory w/ one MRH-R	Max Memory w/ two MRH-Rs
64Mbit	512 MB	1 GB
128Mbit	1 GB	2 GB
256Mbit	2 GB	4 GB

Figure 1 is a block diagram of an Intel® 840 memory subsystem using two MRH-Rs per ‘expansion’ channel to support four Direct RDRAM Channels.

Figure 1. Intel® 840 Chipset Memory Subsystem with MRH-Rs

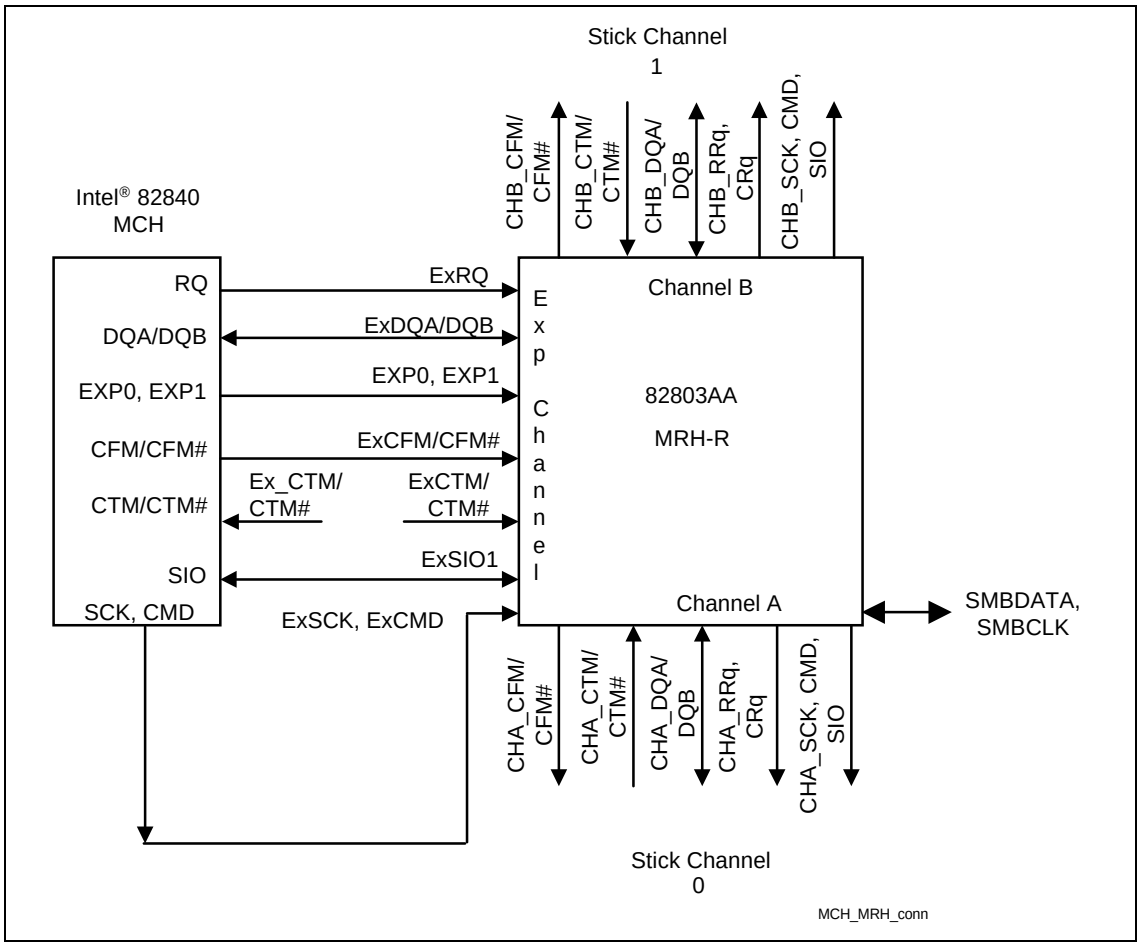


1.2. ‘Expansion’ Channel Interface

The ‘expansion’ channel is the interconnection between the MCH and the MRH-R. The ‘expansion’ channel is a superset of the Direct RDRAM channel. In addition to the Direct RDRAM channel signals, the ‘expansion’ channel has two RSL signals to communicate channel and control information from the MCH to the MRH-R. These two signals are known as expansion control signals, EXP0 and EXP1.

The ‘expansion’ channel interface consists of 28 RSL, 4 clock and 3 CMOS signals. Figure 2 shows the interface signals between the MCH and the MRH-R.

Figure 2. 82840 MCH to 82803AA MRH-R Interconnect Diagram



1.3. MRH-R Direct RDRAM ‘Stick’ Channel Interface

The MRH-R supports two Direct RDRAM channels referred to as Channel A (CHA) and Channel B (CHB) as shown in Figure 2. These two channels are also referred to as ‘Stick’ Channel A and ‘Stick’ Channel B. Each ‘stick’ channel interface consists of 26 RSL, 4 clock and 3 CMOS signals, and supports up to 32 RDRAM devices.

1.4. Register Interface

The MRH-R has internal configuration and control registers. These registers are accessed through the SCK, CMD and SIO CMOS signal interface (ExSCK, ExCMD, and ExSIO for the 'Expansion' Channel). The internal registers in the RDRAM devices are also accessed through the same CMOS signal interface (CHA_SCK, CHA_CMD, and CHA_SIO for 'Stick' Channel A; CHB_SCK, CHA_CMD, and CHB_SIO for 'Stick' Channel B).

In addition, the MRH-R also provides a System Management Bus (SMBus) interface to read the SPD EEPROM on the RIMM module. The SMBus interface consists of two CMOS signals, SMBDATA and SMBCLK.

1.5. Terminology

RAMBUS*

RSL	Rambus* Signaling Level is the name of the signaling technology used by Rambus*.
Rclk	Rclk refers to the RSL bus' high speed clock in a generic fashion, often in the context of clock counts in timing specs.
RAC	Rambus* ASIC Cell. It is the embedded cell designed by Rambus* that interfaces with the Rambus* devices using RSL signaling.
RMC	Rambus* Memory Controller. This is the logic that directly interfaces to the RAC.
RIMM	Rambus* Interface Memory Module.

Components

Intel® 82840 MCH	The Memory Controller Hub component that contains the CPU interface, Rambus* controller, and AGP interface. It communicates with the ICH over a proprietary interconnect called Hub Interface.
Intel® 82803AA MRH-R	The Memory Repeater Hub for RDRAM.
'Expansion' Channel	The RSL bus which connects the Memory Controller Hub to the MRH-R.
'Stick' Channel	The pair of RSL busses which connects an MRH-R to its RDRAM devices. An MRH-R can support a maximum of 2 'stick' channels, 'Stick' Channel A and 'Stick' Channel B.

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2. Signal Description

2.1. ‘Expansion’ Channel Interface

Signal	Type	Description
EXP1	I RSL	**Expansion Row Control.** This signal carries the row control packets (ExRCP) from the MCH to attached MRH-Rs.
EXP0	I RSL	**Expansion Column Control.** This signal carries the column control packets (ExCCP) from the MCH to attached MRH-Rs.
ExDQA[8:0]	I /O RSL	**Expansion Data Bus (Data Byte A).** Bi-directional 9 bit data bus A. These correspond to the CHx_DQA[8:0] signals on the Direct RDRAM ‘Stick’ Channels.
ExDQB[8:0]	I/O RSL	**Expansion Data Bus (Data Byte B).** Bi-directional 9 bit data bus B. These correspond to the CHx_DQB[8:0] signals on the Direct RDRAM ‘Stick’ Channels.
ExRQ[7:5]/ ExRRq[2:0]	I RSL	**Expansion Row Request.** These signals carry row request packets from the MCH to the MRH-Rs. These correspond to the CHx_RQ[7:5]/CHx_RRq[2:0] signals on the Direct RDRAM ‘Stick’ Channels.
ExRQ[4:0]/ ExCRq[4:0]	I RSL	**Expansion Column Request.** These signals carry column request packets from the MCH to the MRH-Rs. These correspond to the CHx_RQ[4:0]/CHx_CRq[4:0] signals on the Direct RDRAM ‘Stick’ Channels.
ExCTM	I RSL	**Expansion Clock To MCH.** One of the two differential transmit clock signals used for MRH-R to MCH operations.
ExCTM#	I RSL	**Expansion Clock To MCH Complement.** One of the two differential transmit clock signals used for MRH-R to MCH operations.
ExCFM	I RSL	**Expansion Clock from MCH.** One of the differential receive clock signals used for MCH to MRH-R operation.
ExCFM#	I RSL	**Expansion Clock From MCH Complement.** One of the differential receive clock signals used for MCH to MRH-R operation.
ExSIO	I/O CMOS	**Expansion Serial IO Chain.** Serial input/output pins used for reading and writing control registers. These correspond to the SIO signals on the Direct RDRAM ‘Stick’ Channels.
ExSCK	I CMOS	**Expansion Serial Clock.** Clock source used to used for timing of the ExSIO and ExCMD signals. This corresponds to the SCK signal on the Direct RDRAM ‘Stick’ Channels.
ExCMD	I CMOS	**Expansion Serial Command.** Serial command input used for control register read and write operations. This corresponds to the CMD signal on the Direct RDRAM ‘Stick’Channels.

2.2. ‘Stick’ Channel A Interface

Signal	Type	Description
CHA_DQA[8:0]	I/O RSL	**Channel A RDRAM Data Bus (Data Byte A).** Bi-directional 9 bit (8 data plus one parity) data bus A.
CHA_DQB[8:0]	I/O RSL	**Channel A RDRAM Data Bus (Data Byte B).** Bi-directional 9 bit (8 data plus one parity) data bus B.
CHA_RQ[7:5]/ CHA_RRq[2:0]	O RSL	**Channel A Row Request.** RQ[7:5]/RRq[2:0] are used to transmit Row Request Packets to RDRAM
CHA_RQ[4:0]/ CHA_CRq[4:0]	O RSL	**Channel A Column Request.** RQ[4:0]/CRq[4:0] are used to transmit column request packets to RDRAM.
CHA_CTM	I RSL	**Channel A Clock To MRH-R.** One of the two differential receive clock signals used for RDRAM to MRH-R operation.
CHA_CTM#	I RSL	**Channel A Clock To MRH-R Complement.** One of the two differential receive clock signals used for RDRAM to MRH-R operation.
CHA_CFM	O RSL	**Channel A Clock From MRH-R.** One of the differential transmit clock signals used for MRH-R to RDRAM operation.
CHA_CFM#	O RSL	**Channel A Clock From MRH-R Complement.** One of the differential transmit clock signals used for MRH-R to RDRAM operation.
CHA _CMD	O CMOS	**Channel A Command.** This signal is used for SIO framing sequence, pin initialization and power management.
CHA_SCK	O CMOS	**Channel A Serial Clock.** The signal provides SIO clocking for register accesses and selects RDRAM devices for power management.
CHA_SIO	I/O CMOS	**Channel A Serial Input and Output.** This bi-directional signal is used to carry data for SIO operations: register accesses, device reset and device ID initialization.

2.3. 'Stick' Channel B Interface

Signal	Type	Description
CHB_DQA[8:0]	I/O RSL	**Channel B RDRAM Data Bus, Data Byte A.** Bi-directional 9 bit (8 data plus one parity) data bus A.
CHB_DQB[8:0]	I/O RSL	**Channel B RDRAM Data Bus, Data Byte B.** Bi-directional 9 bit (8 data plus one parity) data bus B.
CHB_RQ[7:5]/ CHB_RRq[2:0]	O RSL	**Channel B Row Request.** RQ[7:5]/RRq[2:0] are used to transmit Row Request Packets to RDRAM
CHB_RQ[4:0]/ CHB_CRq[4:0]	O RSL	**Channel B Column Request.** RQ{4:0]/CRq[4:0] are used to transmit column request packets to RDRAM.
CHB_CTM	I RSL	**Channel B Clock To MRH-R.** One of the two differential receive clock signals used for RDRAM to MRH-R operation.
CHB_CTM#	I RSL	**Channel B Clock To MRH-R Complement.** One of the two differential receive clock signals used for RDRAM to MRH-R operation.
CHB_CFM	O RSL	**Channel B Clock From MRH-R.** One of the differential transmit clock signals used for MRH-R to RDRAM operation.
CHB_CFM#	O RSL	**Channel B Clock From MRH-R Complement.** One of the differential transmit clock signals used for MRH-R to RDRAM operation.
CHB_CMD	O CMOS	**Channel B Command.** This signal is used for SIO framing sequence, pin initialization and power management.
CHB_SCK	O CMOS	**Channel B Serial Clock.** The signal provides SIO clocking for register accesses and selects RDRAM devices for power management.
CHB_SIO	I/O CMOS	**Channel B Serial Input and Output.** These bi-directional signals are used to carry data for SIO operations (register accesses, device reset, and device ID initialization).

2.4. Miscellaneous Signals Interface

2.4.1. MRH_SIO and SMBus Signal Interface

Signal	Type	Description
MRH_SIO	I/O CMOS	**MRH-R Serial Input and Output.** This bi-directional signal is used to carry data for SIO operations between MRH-Rs. These operations include: register accesses, device reset and device ID initialization.
SMBDATA	I/O CMOS	**SM Bus Data.** SM bus data.
SMBCLK	I/O CMOS	**SM Bus Clock.** SM bus clock.

2.4.2. Clocks, Reset, and Miscellaneous

Signal	Type	Description
SYNCLKNA	O CMOS	**Phase Detector Input to DRCG.** This signal is connected to the SYNCLKN pin of the DRCG (Direct Rambus* Clock Generator) used for clocking RDRAM channel A.
SYNCLKNB	O CMOS	**Phase Detector Input to DRCG.** This signal is connected to the SYNCLKN pin of the DRCG (Direct Rambus* Clock Generator) used for clocking RDRAM channel B.
PCLKMA	O CMOS	**Phase Detector Input to DRCG.** This signal is connected to the PCLKM pin of the DRCG (Direct Rambus* Clock Generator) used for clocking RDRAM channel A.
PCLKMB	O CMOS	**Phase Detector Input to DRCG.** This signal is connected to the PCLKM pin of the DRCG (Direct Rambus* Clock Generator) used for clocking RDRAM channel B.
STOPA#	O CMOS	**DRCG A STOP Signal.** This signal is connected to the DRCG's STOP# input corresponding to stick channel A.
STOPB#	O CMOS	**DRCG B STOP Signal.** This signal is connected to the DRCG's STOP# input corresponding to stick channel B.
PWRDNA#	O CMOS	**DRCG A PWRDN Signal.** This signal is connected to the DRCG's PWRDN# input corresponding to stick channel A.
PWRDNB#	O CMOS	**DRCG B PWRDN Signal.** This signal is connected to the DRCG's PWRDN# input corresponding to stick channel B.
REFCLK	O CMOS	**Reference Clock to DRCGs.** This pin is connected to the REFCLK inputs on both DRCGs .
RST#	I CMOS	**Reset.** When asserted, this signal asynchronously resets the MRH-R logic. This is the system reset signal used for resetting the MCH, ICH, etc.

2.4.3. Voltage/Ground References

Signal	Description
EXVREF[A:B], CHA_VREF[A:B], CHB_VREF[A:B]	**RDRAM Reference Voltage[1.4V].** RSL reference voltage for 'expansion' channel and Direct RDRAM 'Stick' channels.
VCC1_8	**1.8V Power Pins.** Power pins for RSL interface.
VSS	**Ground Pins.** Ground pins for RSL interface.

3. Register Description

3.1. MDID—MRH-R Device ID Register

Address: 02h
Default: 04C0h
Access: R/W (bits 5:14 are read only)
Size: 16 bits

Bit	Descriptions
15:13	Reserved
12:10	**Channel ID Mask.** This field is used to mask the MRH-R ID bits from the Device ID to get the channel ID. Device ID bits 2:1 are used for MRH-R ID. When a mask bit has a value of 0, it masks the corresponding bit in the device ID. 001 **=** This field is hardwired to 001.
9:8	Reserved
7:5	**MRH-R ID Mask.** This field is used to mask the channel ID bits from the Device ID to derive the MRH-R ID. The Device ID bit 0 is used for channel ID. When a mask bit has a value of 0, it masks the corresponding bit in the device ID. 110 = This field is hardwired to 110.
4:3	Reserved
2:0	**Device ID.** This field specifies the device ID of the MRH-R. The device ID is compared against the device ID in the ExRCP and ExCCP packets to determine if this is the addressed MRH-R device.

3.2. EXCC—Expansion Bus Current Control Register

Address: 04h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Enable Stick Channel B.** When this bit is set to 0, all the logic and circuits including DLLs and clock generator associated with channel B are turned off. This bit must not be turned on and off dynamically. Once the BIOS determines there are devices on channel B it can set this bit to 1 to activate that channel.
9	**Enable Stick Channel A.** When this bit is set to 0, all the logic and circuits including DLLs and clock generator associated with channel A are turned off. This bit must not be turned on and off dynamically. Once the BIOS determines there are devices on channel A it can set this bit to 1 to activate that channel.
8:7	Reserved
6:0	**Current Control A.** This seven bit field controls the current for the EXDQA[8:0] and EXDQB[8:0] 'expansion' channel RSL pins.

3.3. CACC—Channel A Current Control Register

Address: 06h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:7	Reserved
6:0	**Current Control A.** This seven bit field controls the current for the CHA_DQA[8:0] and CHA_DQB[8:0] 'stick' channel RSL pins.

3.4. CBCC—Channel B Current Control Register

Address: 08h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:9	Reserved
8:7	Reserved
6:0	**Current Control A.** This seven bit field controls the current for the CHB_DQA[8:0] and CHB_DQB[8:0] 'stick' channel RSL pins.

3.5. SPDRDR—SPD Read Data and Status Register

Address: 0Ah
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15	**Read Data Status.** 1 = The SPD Read Data located in bits[7:0] of this register, is valid. 0 = This bit is cleared when this register is read by the MCH.
14	**Write Operation Done.** 1 = Set by MRH-R when the SPDW command execution is successfully completed on the SMBUS. 0 = Cleared when this register is read by the MCH.
13	**SMBUS Error.** 1 = Set by the MRH-R if the transaction initiated on the SMBUS did not complete successfully. 0 = Cleared when this register is read by the MCH.
12:8	Reserved
7:0	**SPD Register Read/Write Data.** This field contains the data read from the EEPROM due to an SPDR command issued by the MCH. This data field is valid only when the "Read Data Status" bit (bit 15 of this register) has a logic value of 1.

3.6. CCR—Clock Control Register

Address: 0Bh
Default: 0000h (bit '0' is Read Only)
Access: Read/Write
Size: 16 bits

Bit	Description
15:6	Reserved
5	**DRCG B STOP#.** This bit is directly connected to the STOPB# pin on the MRH-R. This pin is then connected to the STOP# pin on the channel B DRCG.
4	**DRCG B PWRDN#.** This bit is directly connected to the PWRDNB# pin on the MRH-R. The PWRDNB# pin is connected to the channel B external DRCG PWRDN# pin. Note that this pin defaults to '0' so that the DRCG is disabled at powerup.
3	**DRCG A STOP#.** This bit is directly connected to the STOPA# pin on the MRH-R. This pin is then connected to the STOP# pin on the channel A DRCG.
2	**DRCG A PWRDN#.** This bit is directly connected to the PWRDNA# pin on the MRH-R. The PWRDNA# pin is connected to the PWRDN# pin on the channel A external DRCG. Note that this pin defaults to '0' so that the DRCG is disabled at powerup.
1	**External Clock Generation.** When set to '1', this bit indicates that external DRCGs will generate the clocks for 'stick' channels A and B.
0	**Expansion Skip Status Bit (ESS).** This bit contains a value indicating the phase relationship of the CFM/CTM clocks.

3.7. LMTR—Levelization Mode And Timing Register

Address: 0Eh
Default: 0000h
Access: Bit 15 read only, bits 14:12 write-only, bits 11:8, 7, 6:4, 3:0 are write-gated
Size: 16 bits

Bit	Description
15	**Levelization Mode Status (LMS)—RO.** 1 = MRH-R is in levelization mode. (i.e., via SLM command described below.) 0 = Normal operation for the MRH-R.

Bit	Description
14:12	**Levelization Commands (LCMD).** 000 = **NOP.** no command. 001 = **Write to tCAC field (W_TCAC).** write-enables the tCAC field (bits 11:8) in this register. 010 = **Write to tRDLY field (W_TRDLY).** write-enable for tRDLY field (bits 6:4). This field can be written to in levelization or non-levelization mode. However, while in levelization mode, the value contained in this register will NOT affect 'stick' channel read delay towards the 'expansion' channel. 011 = **Write to tRDLY_stick field (W_STRDLY).** tRDLY_stick field (bits 2:0) are written. In this case, the measured value during levelization is overwritten. If the MRH-R is in levelization mode, then this command has no effect. 100 = **Write to clock frequency bit (W_FREQ).** The MCH writes to Bit 7 of this register before RAC initialization to determine the RDRAM Clock Frequency for the MRH-R. 101 = **Write ALL Fields (W_ALL).** Causes all fields (tCAC, tRDLY, tRDLY_stick, and frequency) to be written to. Can be used for R/W testing of the register bits. Note that the tRDLY_stick field write restriction still applies while in levelization mode. 110 = **Clear Levelization Mode (CLM).** Causes the MRH-R to exit levelization mode. The last measured read data delay value during levelization - the tCAC value in bits 11:8 of this register will be contained in the tRDLY_stick bits. During normal mode, the value of the tRDLY register will now also affect the delay in the MRH-R read FIFO unload to the 'expansion' bus (which effectively delays read data towards the MCH). 111 = **Set Levelization Mode (SLM).** This command causes the MRH-R to enter levelization mode. In this mode, read data delay from the 'stick' channels to the 'expansion' channel remains fixed at 3 rclks – tTR, regardless of the value in the MRH-R tRDLY register and the tRDLY_stick field of this register. The MRH-R also starts measuring (on-the-fly), the # rclks from an expansion SCP read command to when a leading '1' bit is detected in the internal read path from either 'stick' channel on 'stick' channel data signal DQA5, or in other words, the 'stick' channel's read delay. The desired read to be measured is to the last (furthest) RDRAM on the 'stick' channel.
11:8	**RDRAM tCAC read access delay (tCAC).** (Write-gated by W_TCAC above). This field defines the minimum delay in rclks for RDRAMs from a Read SCP command to read data on the 'stick' channels (4-9). Values of 0-3, and A-Fh are illegal. The MRH-R must use this parameter to time its read data path.
7	**RDRAM Clock Frequency (freq).** (Write-gated by W_FREQ above]. Must be set to proper value before RAC initialization begins. 0 = 300 MHz bus operation 1 = 400 MHz bus operation.
6:4	**Expansion Channel Time Domains (tRDLY).** [Write-gated by W_TRDLY above]. This field controls the read data delay from the MRH-R to the 'expansion' channel. Its purpose is to allow time domain equalization to be achieved among ALL 'stick' channels behind ALL MRH-Rs to the MCH. During levelization, the value of this register will not affect read data delay thru the MRH-R which remains fixed at 3-tTR rclks. In normal operation, its value will add to the total read data delay from all RDRAM devices on the MRH-R's 'stick' channels to the MCH. It is written to using the W_TRDLY command (see above) via a CMOS serial write to this register.
3	Reserved
2:0	**Stick Channel Time Domains (tRDLY_stick).** (Write-gated by W_STRDLY above). This field is written to by the MRH-R itself while in levelization mode with a measured delay (0-7 rclks) from a 'stick' channel SCP read packet to the first non-zero data seen on 'stick' channel signal DQA5 at the MRH-R 'stick' channel interfaces. It is used internally by the MRH-R primarily to control its read data delay FIFO loading and to control the 'stick' channels to 'expansion' channel data steering mux. It can also be written to using a W_STRDLY command (see above) via a CMOS serial write to this register, but while the MRH-R is in levelization mode, it is Read-Only (ie. wrt CMOS bus). BIOS can read this field to determine the number of time domains on the addressed MRH-R's 'stick' channels.

3.7.1. RIR—RAC Initialization Register

Address: 0Fh
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:5	Reserved.
4	**RAC Initialization Complete (RC).** The MRH-R sets this bit after it has completed RAC initialization. BIOS must check this bit to make sure the RACs have been properly initialized before initiating memory accesses. 1 = Initialization Complete 0 = Initialization not Complete
3	**Initiate RIC operation (IRO).** BIOS must check that this bit is 0 before writing to this bit again. 1 = Execution In-Progress. Execution of the RIC command specified by bits 2:0 begins. 0 = Execution Complete. After the operation is completed, the MRH-R clears this bit to 0.
2:0	**RAC Initialization Command (RIC).** This field allows BIOS to initialize the MRH-R RACs. BIOS programs this field with the appropriate command then sets bit 3 to 1. The MRH-R then executes the command specified in this field. When the operation is complete, the MRH-R clears bit 3 to 0. 000 = Reserved 001 = **Initialize Expansion RAC.** When the MRH-R receives this command, it performs initialization sequence on the MRH-R RAC. The initialization process includes executing the power-up sequence to the RAC, powering up the DRCG's for enabled 'stick' channels, and Current and Temperature Calibrating of the MRH-R 'expansion' channel RAC. 010 = **Manual Current Calibrate the RAC.** When the MRH-R receives this command, it issues a Manual Current Calibrate sequence to ALL the RACs. The current control values specified in the EXCC, CACC, CBCC registers are used as the manual current control values. 011 = **Temperature Calibrate the RAC.** When the MRH-R receives this command, it issues a Temperature Calibrate sequence to ALL the RACs. 100 = **Set Fast Clock (SETF).** When the MRH-R receives this command, it issues a Set Fast clock sequence to the RAC. 101 = **Initialize Stick RACs.** When the MRH-R receives this command, it performs initialization sequence on the MRH-R 'stick' channel RACs. The initialization process includes executing the power-up sequence to the RAC, and RAC Current and Temperature Calibration. 111 = Reserved

3.8. RACAL—Stick Channel A RAC Configuration Low WORD Register

Address: 10h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:0	**RAC Configuration Bits [15:0].** Bits [15:0] of the RAC configuration.

3.9. RACAH—Stick Channel A RAC Configuration High WORD Register

Address: 11h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:0	**RAC Configuration Bits [31:16].** Bits [31:16] of the RAC configuration.

3.10. RACBL—Stick Channel B RAC Configuration Low Word Register

Address: 12h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:0	**RAC Configuration Bits [15:0].** Bits [15:0] of the RAC configuration.

3.11. RACBH—Stick Channel B RAC Configuration High Word Register

Address: 13h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:0	**RAC Configuration Bits [31:16].** Bits [31:16] of the RAC configuration.

3.12. RACXL—Expansion Channel RAC Configuration Low Word Register

Address: 14h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:0	**RAC Configuration Bits [15:0].** Bits [15:0] of the RAC configuration.

3.13. RACXH—Expansion Channel RAC Configuration High Word Register

Address: 15h
Default: 0000h
Access: Read / Write
Size: 16 bits

Bit	Description
15:12	Reserved
11:10	**On-die Termination Resistor Enable.** 00 = Disabled 01 = Reserved 10 = Reserved 11 = Enabled
9:0	Reserved

3.14. INIT—MRH-R Initialization Register

Address: 21h
Default: 009Fh
Access: R/W
Size: 16 bits

Bit	Descriptions
15:8	Reserved.
7	**SIO repeater bit (SRP).** This bit controls the value on the MRH_SIO pin. After an SIO Reset command is executed, SRP will have a logic value of 1. 1 = MRH_SIO = ExSIO 0 = MRHSIO = 1
6:5	Reserved
4:0	**Serial ID.** This field specifies the Serial ID of the MRH-R. The serial ID is compared against the serial address in initialization request packets to determine if this is the addressed MRH-R device.

3.15. CNFGA—MRH-R Configuration Register

Address: 23h
Default: 8001h
Access: Read only
Size: 16 bits

Bit	Descriptions
15	**MRH-R Identification.** This field identifies the addressed device. When set to 1, the device is MRH-R. When set to 0, the addressed device is an RDRAM device. **This field must be set to 1 for MRH-R**.
14:6	Reserved
5:0	**Manufacturer.** This field specifies the manufacturer ID.

3.16. ST—Stepping Register

Address: 24h
Default: 0000h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7:4	**Protocol Revision.** This field specifies the version of the Direct RDRAM channel implemented.
3:0	**Stepping.** This field specifies the manufacturer version number. 000 = A-1 Stepping 010 = A-2 Stepping All others = Reserved

4. Functional Description

4.1. MRH-R and the Direct RDRAM Channel

4.1.1. Operation Overview

The MRH-R acts as a Direct RDRAM channel expander by duplicating the signal activities on the ‘expansion’ channel to the specified ‘stick’ channel and vice versa. There is a time delay between the signal activities happening on the ‘expansion’ bus and the same signal activities on the ‘stick’ channels. This time delay must be constant under all operating conditions. The delay for RSL signals and delay for CMOS signals are different.

The MRH-R has the logic capability to help the MCH to maximize channel efficiency. This includes doing Refresh, Precharge After Refresh, Nap Exit, Power-down Exit, RAC Current Calibrate, RAC Current Calibrate & Sample, and Temperature Calibrate of devices on a channel upon request from the MCH.

The MRH-R contains registers for configuration and control. These registers are accessed through a three signal CMOS interface. The MRH-R implements a similar three signal CMOS interface for each ‘stick’ channel to reset and initialize RDRAMs. The same interface is used for accessing the internal registers of the RDRAM devices.

4.1.2. Signal and Protocol Overview

The ‘Expansion’ Channel (Ex) consists of the set of signals used to transmit information to and from the MRH-Rs and the protocol that defines the format and sequencing of this information. Both the signals and protocol of the ‘expansion’ channel are a superset of the their counterparts on the Direct RDRAM ‘stick’ channels. This allows efficient use of the multitude of ‘stick’ channels supported. Access can be pipelined with and across the Direct RDRAM channels, and sufficient control bandwidth is provided so that channel service operations such as refresh can proceed in parallel with fully pipelined memory accesses.

A Direct RDRAM Channel consists of two groups of high speed (RSL) control signals, a high speed (RSL) data bus, and a group of low speed CMOS control signals. The control signal groups are referred to as the Row Request Bus and the Column Request Bus. Each of these request busses has a request packet format associated with it—Row Request Packet (RRQP) and Column Request Packet (CRQP). Row and Column request packets can be pipelined to maximize data throughput to and from the memory.

To achieve full bandwidth operation on the ‘expansion’ channel, all control operations must be pipelined with the memory request packets. Further, independent expansion control must be allocated for the Row Request (RRq) and Column Request (CRq) packets on the ‘stick’ channels to maintain the variable RAS to CAS timings. This requirement results in two extra signals on the ‘expansion’ channel—Row Control Bus (EXP1), and Column Control Bus (EXP0).

Control packets on the ‘expansion’ channel are issued using EXP1 and EXP0 with the corresponding Row Request and Column Request packets. They are used to select the MRH-R that supports the targeted

'stick' channel. The EXP1 and EXP0 are used by the MRH-R to decode the Channel ID and route the incoming request packets appropriately. Because the underlying 'expansion' channel request packets have the same format as the 'stick' channel request packets, there is no command or address translation involved.

Expansion control packets provide support operations and the requisite control channel bandwidth for maintaining the many memory channels in a system. For example, the 'expansion' channel provides a channel refresh command that can be overlaid on memory access requests and that does not reduce memory bandwidth. In addition to refresh, the 'expansion' control packets provide commands for memory channel powerdown exit, nap exit, precharge after refresh, current control and temperature calibrate for 'expansion' bus. These, as well, have control channel bandwidth allocated so that memory accesses are not impacted.

4.1.2.1. Refresh and Post-Refresh Precharge

The 'expansion' channel architecture supports the issue of broadcast refresh and post-refresh precharge operations to a specified 'stick' channel that can be carried out concurrent with memory accesses. This allows the effective BW overhead of memory refresh to be reduced.

4.1.2.2. Power Mode Control

The 'expansion' channel provides a control mechanism that allows an entire channel to be NAP-exited as well as device-specific NAP exited.

The 'expansion' channel architecture also provides a control mechanism that allows a channel to be activated from the power-down state concurrent with memory accesses. This is useful when a system is being powered up. The first channel to be accessed will be powered up using an RDRAM request packet. The 'expansion' channel mechanism allows additional channels to be powered up concurrently with accesses to already powered channels.

Refer to Rambus* Technical Documentation for detailed information.

4.1.2.3. Current Calibration

The current calibration of an RDRAM device on a MRH-R 'stick' channel is performed by the MCH through a Secondary Control Packet (SCP) command. The MCH issues three consecutive Current Calibrate SCP commands followed by a Current Calibrate and Sample SCP command to the targeted RDRAM device.

The current calibration of the 'expansion' channel RAC and the 'stick' channel RACs in the MRH-R is accomplished through an EXP0 packet. The MCH issues three consecutive Expansion Current Calibrate commands followed by a Expansion Current Calibrate and Sample command to the targeted MRH-R.

On its 'expansion' channel interface (slave RAC), the MRH-R drives the ExDQB[4:3] pins to perform the current calibration function. On the Direct RDRAM 'stick' channel A and 'stick' channel B (master RACs), the MRH-R performs current calibration on the CHx_DQB[2:1] pins. This allows the MCH to perform current calibration at the same time as the MRH-Rs on the 'expansion' channel. Note also that an MRH-R can perform current calibration on it's own RACs at the same time as an RDRAM on it's own 'stick' channels since they use different DQ pins.

4.1.2.4. Thermal Sensor Read

RDRAM devices report their thermal sensor status on DQA[5] during a current calibrate cycle. The MRH-R simply treats this as read data and passes the data back to the MCH with read data levelization. Refer to Rambus* Technical Documentation for more information.

4.1.2.5. Temperature Calibration

In addition to the current calibration, all RDRAM devices on the ‘stick’ channels must be temperature calibrated. The temperature calibration is accomplished through the CMOS interface signals on the ‘stick’ channels. The MCH issues an EXP0 packet with a temperature calibration command to the specified channel. After receiving this command, the MRH-R issues a Temperature Calibrate Enable command followed immediately by a Temperature Calibrate command via the CMOS interface signals to the RDRAM channel. Refer to Rambus* Technical Documentation for detailed information.

4.1.3. CMOS Protocol

4.1.3.1. Overview

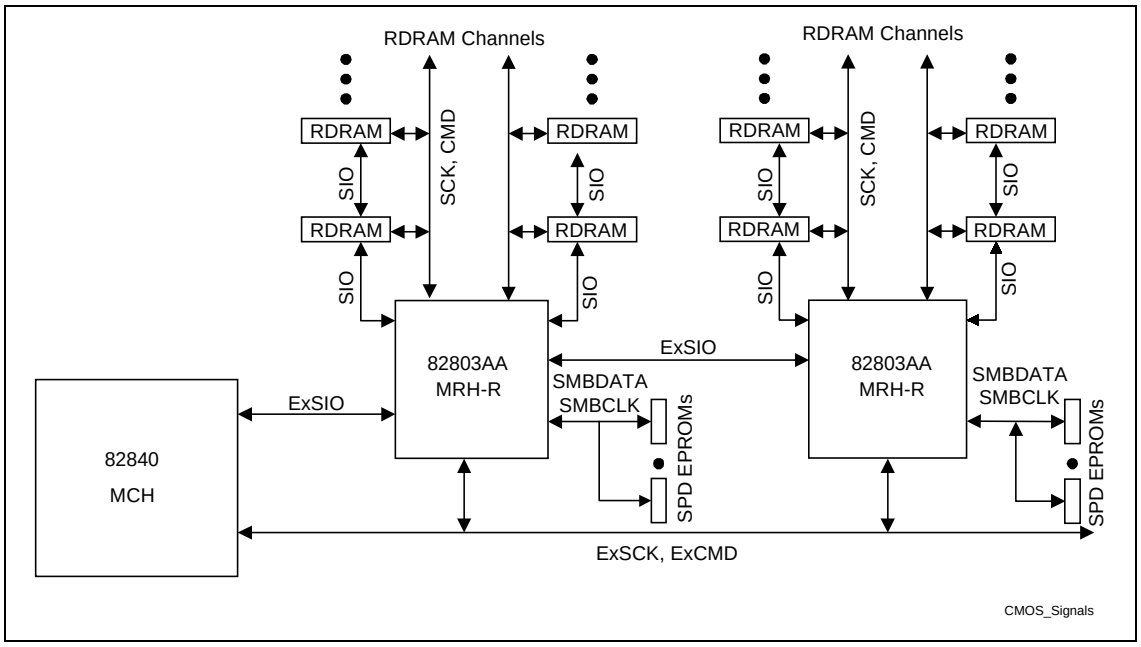
The CMOS protocol on the MRH-R Direct RDRAM ‘Stick’ Channels is used for RDRAM initialization, RDRAM register reads, RDRAM register writes, and RDRAM power mode exit control.

The CMOS protocol on the ‘expansion’ channel is used for MRH-R initialization, MRH-R register reads, MRH-R register writes, and SPD EEPROM reads/writes. For interfacing to the SPD EEPROMs on the RIMMs, there are two additional CMOS signals (SMBDATA, SMBCLK) provided from the MRH-R. These CMOS signals are not considered to be part of ‘expansion’ channel.

The connection of CMOS signals between the MCH, MRH-R, and RDRAM channels is illustrated in Figure 3 below.

Note: This figure depicts the connectivity on one Intel® 82840 MCH Direct RDRAM channel. A second channel exists, so the same implementation is required on the second channel.

Figure 3. Connection of CMOS Signals



An augmented CMOS control packet format is used on the ‘expansion’ channel. This is a superset of the packet format used with RDRAM devices and is described in the next section. The protocol allows packets to be directed to individual MRH-Rs, broadcast to all MRH-Rs, or forwarded to selected ‘stick’ channels.

4.1.3.2. Packet Formats

The serial control packets used on the ‘expansion’ bus are a superset of those used on the ‘stick’ channels. These packets can be directed to a specified MRH-R, broadcast to all MRH-Rs, forwarded to a specified ‘stick’ channel, or broadcast to all ‘stick’ channels. Four types of packets are defined:

- Expansion serial request packets, ExSRQ.
- Expansion serial address, ExSA.
- Expansion serial interval, ExSINT.
- Expansion serial data, ExSD.

The following figures show the layout of Register Read, Register Write, and Non-Register Operation packet types.

Figure 4. Expansion Bus Register Read Packet Format

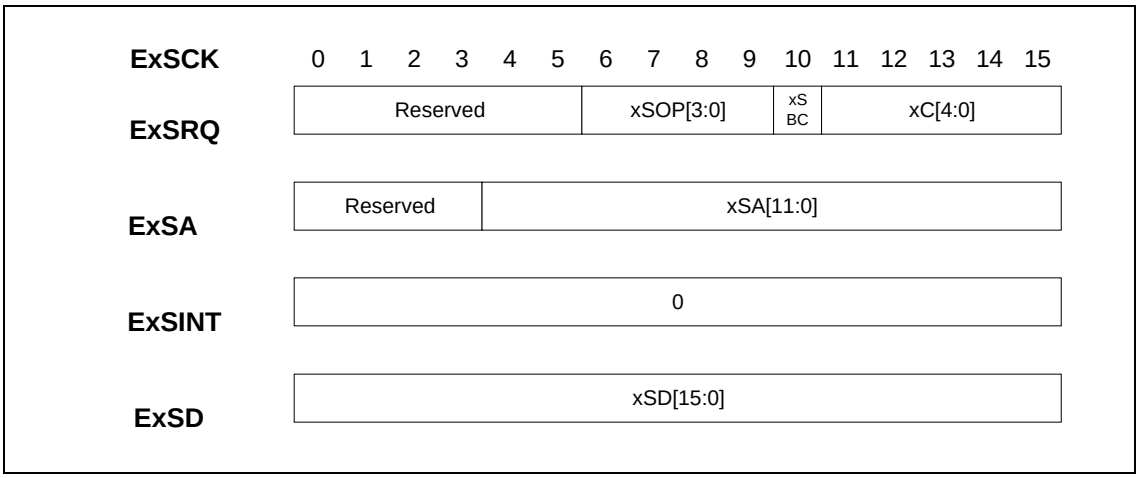


Figure 5. Expansion Bus Register Write Packet Format

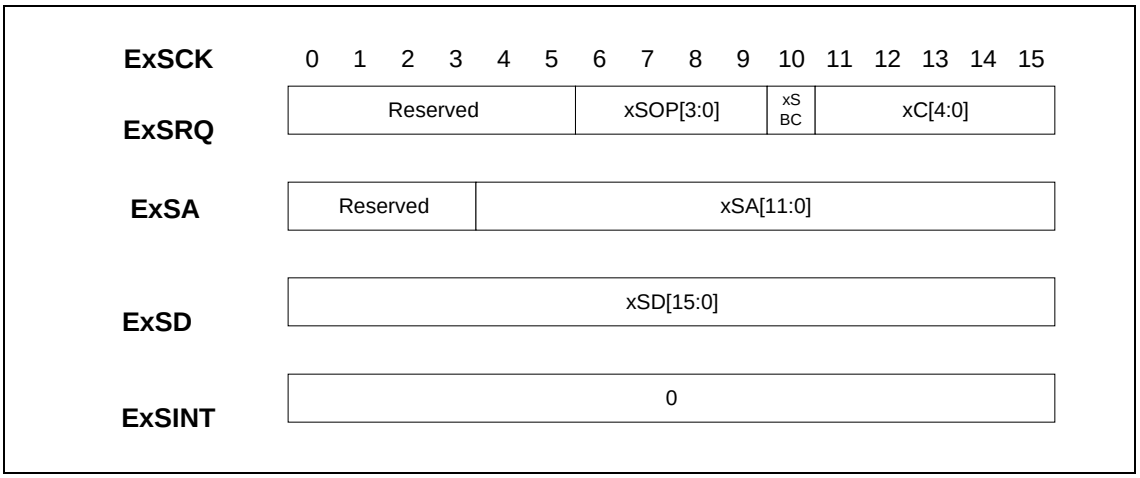
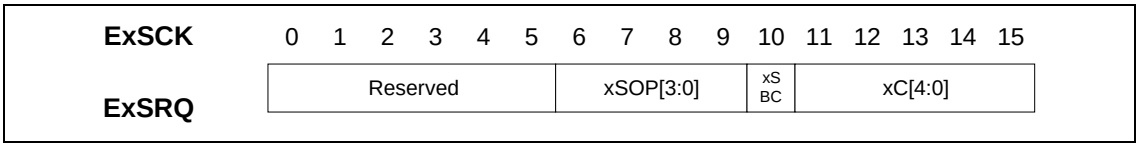


Figure 6. Expansion Bus Non-Register Operation Packet Format



Note that these packet formats are the same as those used by the Direct RDRAM devices. Table 2 describes each of the fields for these serial packets.

Table 2. Expansion Bus Serial Packet Field Definitions

Field	Description
xSOP[3:0]	**Expansion Serial Op-code (ExSOP):** Specifies command for control register operations. Encodings not listed are reserved. 0000 - SRD: Serial read of control register specified in xSA[11:0]. The read could be either from MRH-R specified by xC[4:0] or from the RDRAM device on 'stick' channel specified by previous RNC command. 0001 - SWR: Serial write of control register specified in xSA[11:0]. The write could be either to MRH-R specified by xC[4:0] or to the RDRAM device on 'stick' channel specified by previous RNC command. 0010 - SETR: Set reset bit in the MRH-R specified by xC[4:0] or set reset bit in the RDRAM device specified by the previous RNC command. This command is ignored by the MRH-R and is treated as a NOP. 0100 - SETF: Set Fast Clock bit in the MRH-R specified by xC[4:0] or set Fast Clock bit in the RDRAM device specified by the previous RNC command. This command is ignored by the MRH-R and is treated as a NOP. 1000 - RNC: Route the next ExSOP command to the 'stick channel specified by xC[4:0]. 1001 - RSIO: Perform SIO Reset sequence on the 'stick' channel specified by xC[4:0]. 1011 – CLRR: Clear reset bit in MRH-R specified by xC[4:0] clear reset bit in RDRAM device specified by the previous RNC command. This command is ignored by the MRH-R and is treated as a NOP. 1101 - SPDW: Write Byte to SPD EEPROM specified by xC[4:0], xSA[7:0] and xSD[7:0]. The xC[4:0] specifies the MRH-R associated with the SPD EEPROM. The xSA[7:0] contains the slave address, xSD[157:0] contains the byte address and xXD[15:8] contains the data to be written to the SPD EEPROM. 1110 - SPDR: Random Read the SPD EEPROM specified by xC[4:0], xSA[7:0] and xSD[7:0]. The xC[4:0] specifies the MRH-R associated with the SPD EEPROM. The xSA[7:0] contains the slave address and xSD[7:0] contains the byte address. The Random read operation consists of two transactions on the SMBUS. The first transaction is a write to the SPD EEPROM and the second transaction is a read from the SPD EEPROM. The data read from the EEPROM is placed in the SPDRDR register. Bit 15 of this register indicates whether the data contained in bit[7:0] is valid or not.
xSBC	**Expansion Serial Broadcast**
xC[4:0]	**Expansion Buffer Serial Address:** Compared to bits [4:0] of the INIT control register to select the MRH-R that the expansion serial transaction is directed. Compared to bits [4:0] of the INIT control register to select the RDRAM channel to which the associated serial transaction is directed.
xSA[11:0]	**Expansion Serial Register Address:** xSA[11:0] selects which control register of the selected MRH-R is read or written. xSA[7:0] specifies the slave address for SPDR and SPDW xSOP commands.
xSD[15:0]	**Expansion Serial Data:** The 16 bits of data read from or written to the selected control register in the selected MRH-R. The xSD[7:0] specifies the byte address for SPDR and SPDW commands. The xSD[15:8] specifies the write data for SPDW command.

The following sections detail the available packet formats and the operations that can be performed on the serial control bus (CMOS interface).

4.1.3.3. Transactions

Reset

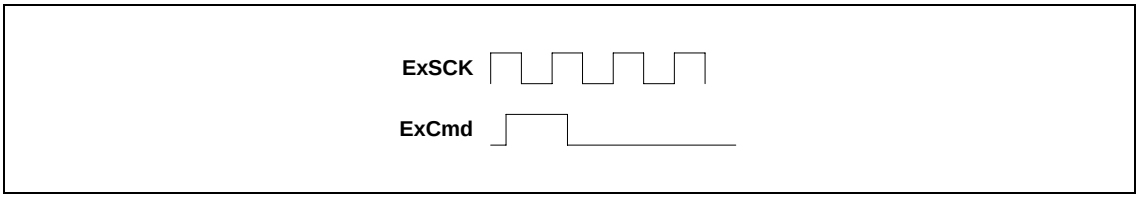
After power-on, the MRH-Rs and all of the RDRAMs in the memory system must be reset. This process uses the following steps:

1. Reset the ExSIO chain that connects the MRH-Rs together.
2. Reset all MRH-Rs on the ‘expansion’ channel using serial control packets. At this point a register read can be issued to determine if the devices connected are MRH-Rs or RDRAMs.
3. Reset SIO serial chain of all RDRAMs on channels A and B.
4. Reset all RDRAMs on RDRAM ‘stick’ channels A and B using serial control packets.

The details of each of these steps are described below.

First, the ExSIO serial chain is reset by issuing an ExSIO reset sequence as shown in Figure 7 ExCMD is sampled on both the rising and falling edges of ExSCK. A 1100 sequence on ExCMD resets the state machine controlling the ExSIO pins in each MRH-R. After this reset, the ExSIO pin is configured as an input and the MRH_SIO pin is configured as output on every MRH-R. Also, the SIO repeater bit in the MRH-R is set to 1.

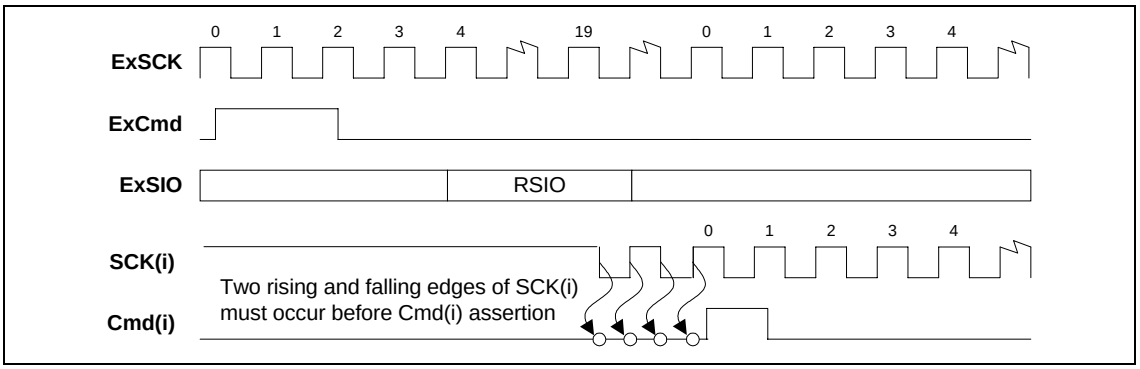
Figure 7. ExSIO Reset Sequence



At this point the RDRAM devices must be reset. This is accomplished by first broadcasting an RSIO command to all MRH-Rs. Upon receiving this command the MRH-R will generate an SIO Reset sequence on RDRAM ‘stick’ channels A and B. The SIO reset sequence is shown in Figure 8.

This completes the resetting of all RDRAMs.

Figure 8. RDRAM SIO Reset Sequence



Now, all MRH-Rs and RDRAMs are reset and ready for levelization and initialization.

4.1.3.4. Levelization

Levelization equalizes all RDRAM device read delays to the furthest device's delay as seen by the MCH. This allows RDRAM timings to remain consistent for each device as seen by the MCH.

4.1.3.5. Initialization

The following steps are performed to initialize the MRH-R based memory subsystem after reset.

1. Assign unique serial addresses to all MRH-Rs.
2. Read all read-only registers and process the information.
3. Update the necessary read-write registers.
4. Initialize the MRH-R 'expansion' RAC via a CMOS broadcast command, enable the external DRCG clock generators for ALL the 'stick' channels. Repeat for all MRH-Rs in the memory subsystem.
5. Assign unique device IDs to each RDRAM and channel IDs to each MRH-R.
6. Repeat steps 1 to 3 for all levels of MRH-R and for all RDRAM channels.
7. Disable and powerdown the DRCGs and 'stick' RACs whose channels have no RDRAM devices attached.
8. Wait for 5 ms from step 4 for the 'stick' channel clocks to stabilize and lock to the 'expansion' channel clocks. Note that steps 5-7 can proceed while waiting for this timeout.
9. Initialize the 'stick' channel RACs of ALL MRH-Rs (can be done using a CMOS Broadcast command). Any 'stick' channel RACs that were powered down in step 7 will remain in that state and will not be initialized.
10. Perform the levelization sequence.

4.1.3.6. MRH-R Register Operations

This section describes the serial read and write operations for control registers within the MRH-R. Figure 9 shows the control register read operation and Figure 10 shows the control register write operation.

Figure 9. MRH-R Register Read

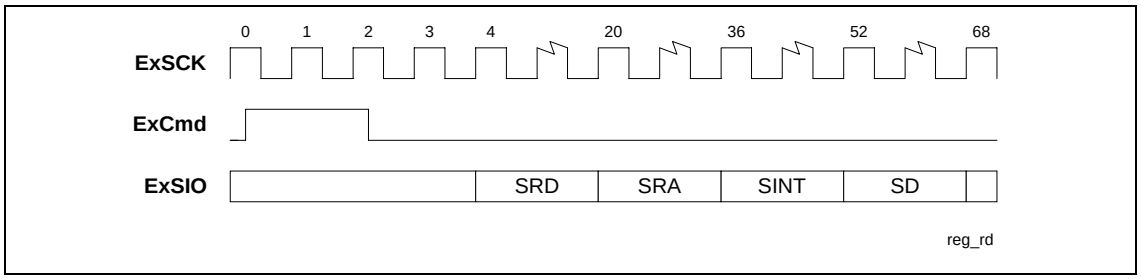
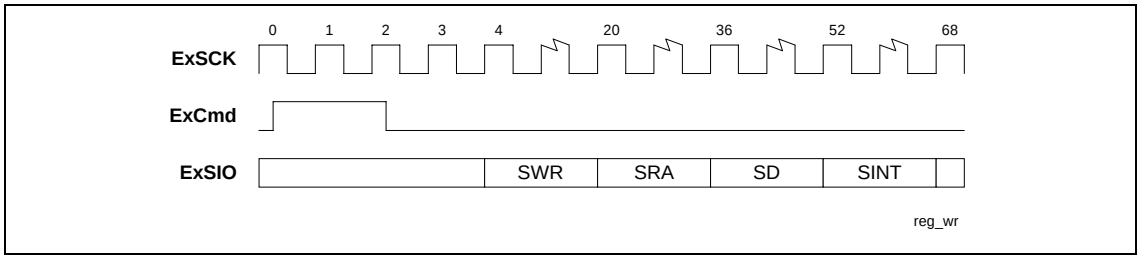


Figure 10. MRH-R Register Write



4.1.3.7. RDRAM Register Operations

This section describes the serial read and write operations for control registers in RDRAM devices. Figure 11 shows the RDRAM register read sequence and Figure 12 shows the RDRAM register write sequence.

Figure 11. RDRAM Register Read from the Expansion Serial Bus

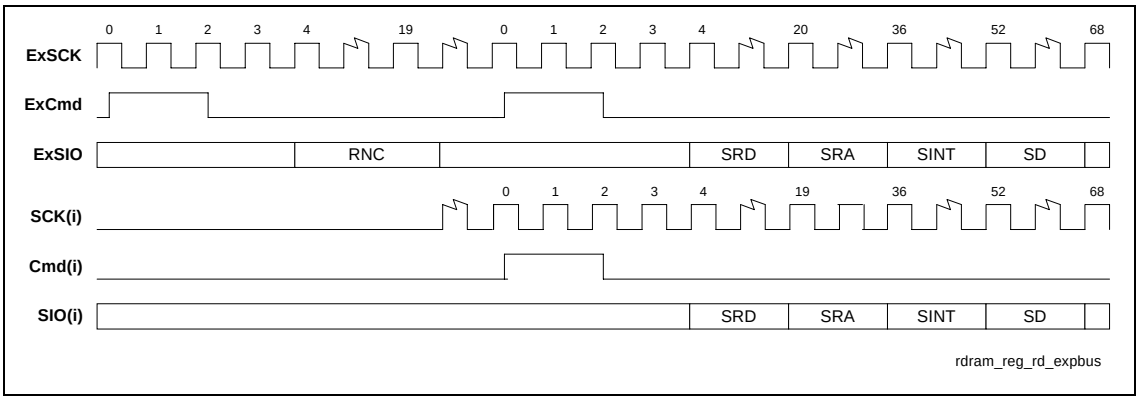
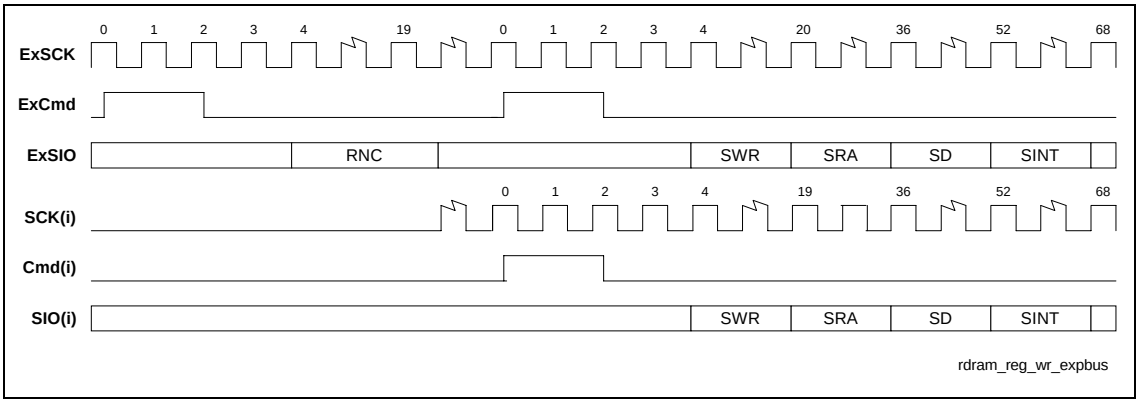


Figure 12. RDRAM Register Write from the Expansion Serial Bus



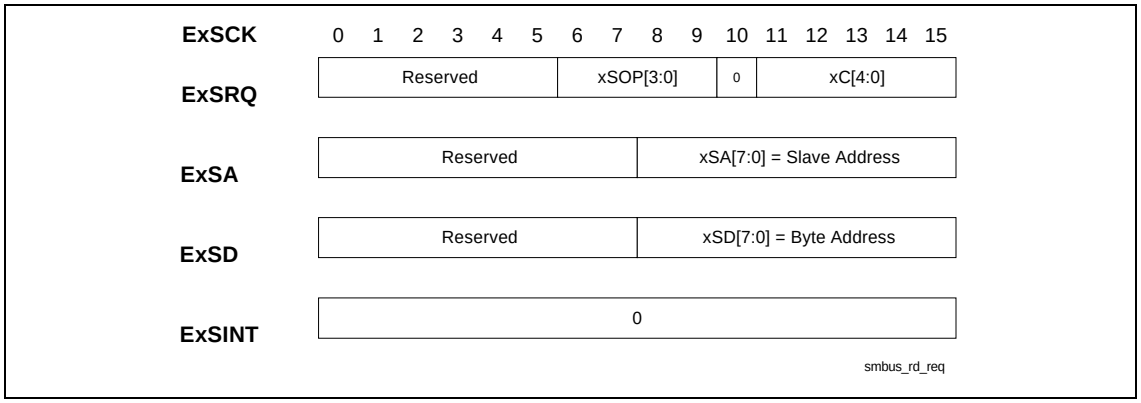
4.1.4. SMBUS Operation

The MRH-R integrates an SMBUS controller to access data to and from the SPD EEPROMs on the RIMMs residing on its channels. There can be a maximum of 8 SPD EPROM associated with two channels. The BIOS accesses the SPD EPROM by issuing a command to the MCH. The MCH in turn sends this command to the appropriate MRH-R through an SIO request packet using the SCK/CMD/SIO interface signals. Once the MRH-R receives this command, it generates the appropriate SMBUS commands to the SPD EEPROMs.

4.1.4.1. SIO Request Packet for SPD Random Read

The SIO request packet format for the SPD EEPROM Random Read command is shown below.

Figure 13. SMBUS SIO Random Read Request Packet Format



After receiving the SPDR command from the MCH, the MRH-R generates two command sequences to the addressed SPD EEPROM. The first command sequence is for writing an 8 bit address to the SPD EEPROM specified by the slave address. The second command is to read the data from the address written by the previous command. The data read from the SPD EEPROM is placed in the SPDRDR register. Bit 15 of this register indicates whether data contained in the SPDRDR register is valid or not. The BIOS can do an MRH-R register read operation to retrieve the data from the SPDRDR register. Bit 15 of the SPDRDR register is reset when the SPDRDR register is read by MCH.

The following figures show the SPDR command sequence from the MCH and the subsequent SMBUS transactions by the MRH-R.

Figure 14. SPDR Command sequence

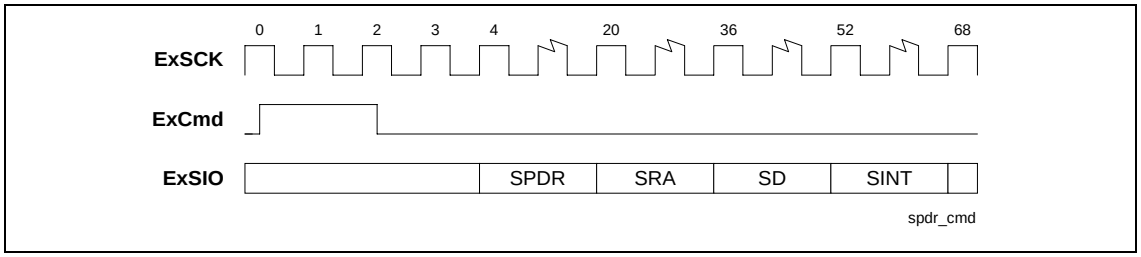
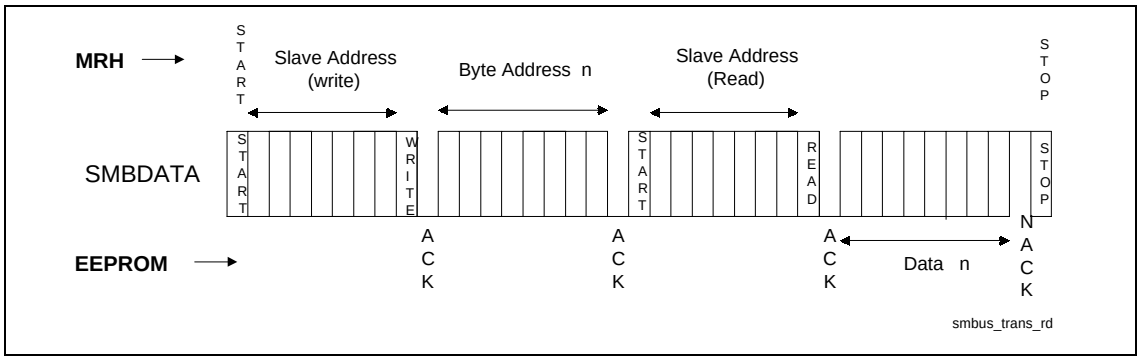


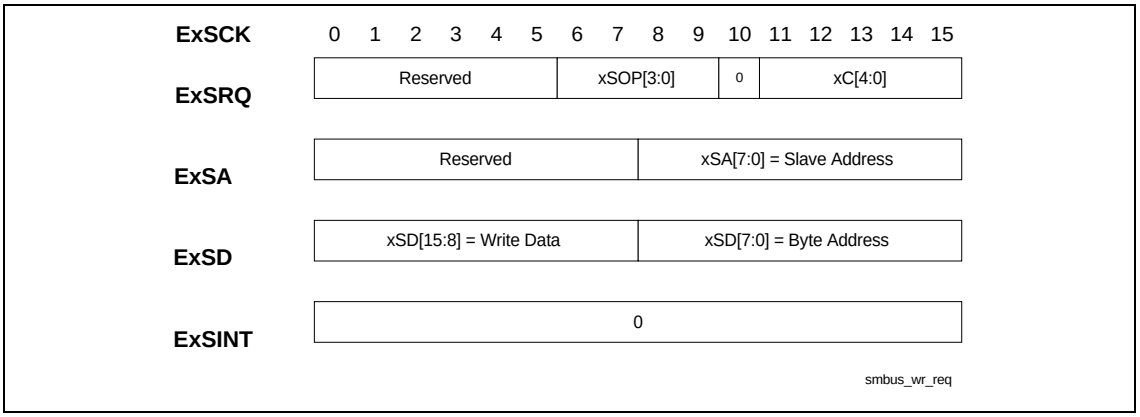
Figure 15. SMBUS Transactions to Read EEPROM



4.1.4.2. SIO Request Packet for SPD Write Command

The SIO request packet format for the SPD EEPROM Write command is shown below.

Figure 16. SMBUS SIO Random Write Request Packet Format



After receiving the SPDW command from the MCH, the MRH-R generates a write command sequence to the addressed SPD EEPROM as shown below**.** The MRH-R sets bit 14 of the SPDRDR register when the SPDW command is successfully completed by the MRH-R. BIOS should check this bit before sending a new command to the SPD EEPROM.

The following figures show the SPDW command sequence from the MCH and the subsequent SMBUS transactions by the MRH-R.

Figure 17. SPDW Command sequence

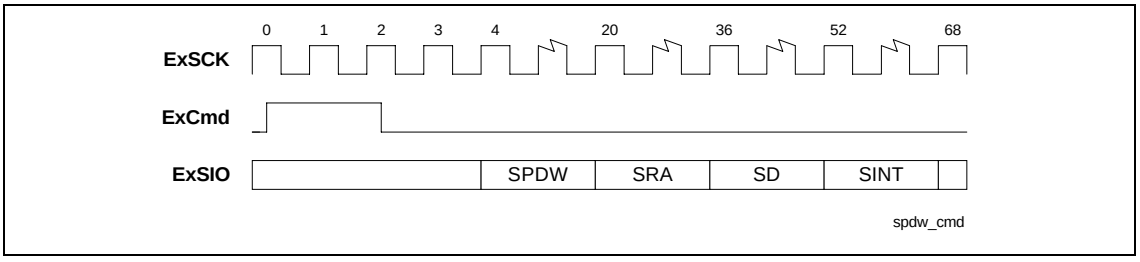
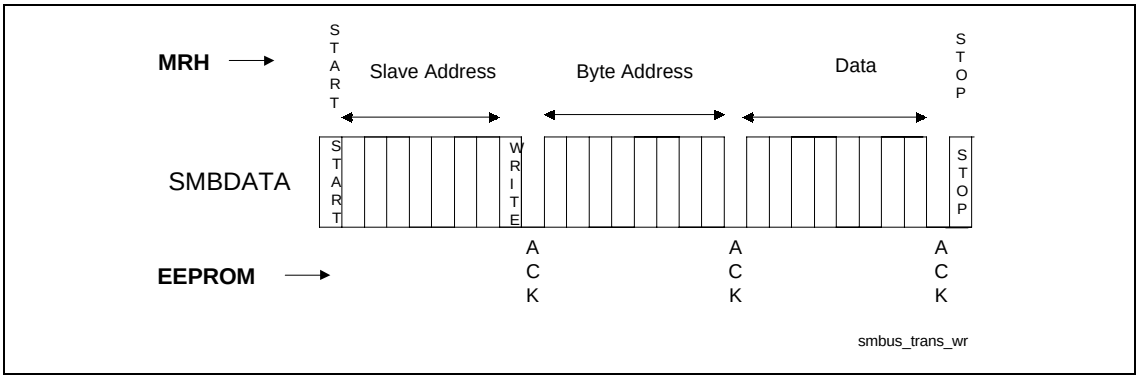


Figure 18. SMBUS Transactions to Write to EEPROM

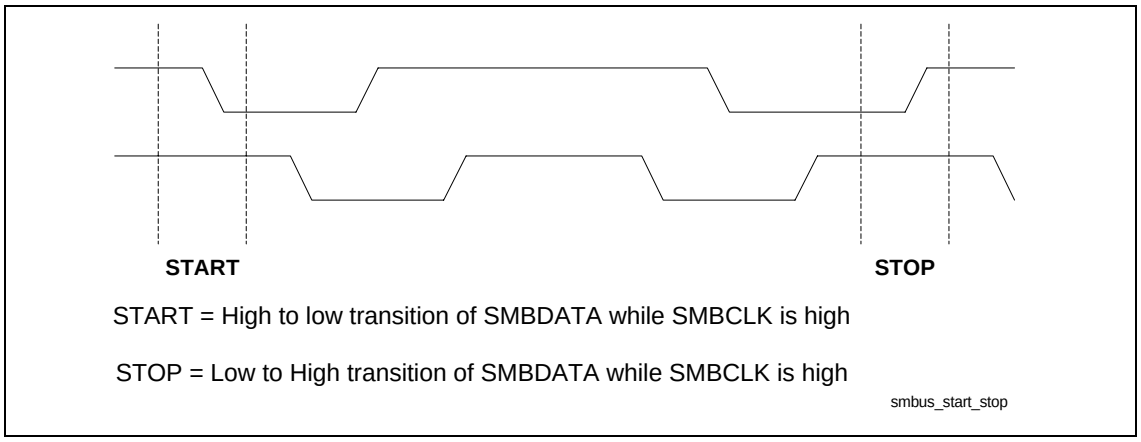


4.1.4.3. Command Protocol and Bus Timing

SMBUS Start and Stop protocol

The following diagram illustrates the start and stop protocol of SMBUS.

Figure 19. SMBUS Start and Stop Conditions



Read Byte

Reading data is accomplished by the MRH-R first writing the byte address to the EEPROM. The MRH-R then follows that write command with a repeated start condition to denote a read from that device's address. The EEPROM then returns 1 bytes of data.

Table 3. Read Byte Protocol

Bit	Description
1	Start
2-8	Slave (EEPROM) Address - 7 bits
9	Write
10	Acknowledge from slave (EEPROM)
11-18	Byte Address - 8 bits
19	Acknowledge from slave (EEPROM)
20	Repeated Start
21-27	Slave (EEPROM) Address - 7 bits
28	Read
29	Acknowledge from slave (EEPROM)
30-37	Data from slave (EEPROM) - 8 bits
38	NOT acknowledge
39	Stop

Bus Timings

The SMBus runs at between 10-80 KHz. Most of the timings associated with the SMBus are microseconds in length. SMBCLK is generated by dividing ExSCK by 16. Thus, when ExSCK is 1 MHz SMBCLK is 62.5 KHz.

Bus Time Out

If there is an error in the transaction, such that EEPROM does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction times out. The MRH-R discards the cycle, and sets bit 14 of the SPDRDR register to indicate the error. The time out minimum is 25 ms. The time-out counter inside the MRH-R starts after the last bit of data is transferred by the MRH-R and it is waiting for a response.

4.2. Reset

After assertion of the MRH-R's RST# input, all internal configuration registers are reset to their default states. The 'expansion' and 'stick' channel RACs are forced to a powered down state and remain there until a RAC initialization command is issued via the CMOS serial bus. All DRCGs are disabled and powered down. RST# should not be deasserted until the 'expansion' channel clocks are running stable. RST# should be prevented from being asserted during a system STR resume sequence to allow the MRH-R internal registers to be preserved. This allows serial channel device ID setup and RSL levelization phases in the Initialization sequence to be skipped, preventing any read or write accesses to RDRAM devices with valid data.

4.3. Power Management

There are two bits specified in EXCC register (Offset 02h) to turn off the logic associated with a 'stick' channel A/B when there are no devices connected to specified 'stick' channel.

4.4. STR Support

The 82803AA MRH-R should be powered down and it's registers saved to memory when supporting the S3, suspend to RAM, sleep state.

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5. Ballout and Package Information

5.1. MRH-R Ballout

Figure 20. MRH-R Ballout (Top View, Left Side)

	1	2	3	4	5	6	7	8	9	10
A	VSS	Reserved	Reserved	Reserved	Reserved	PCLKMB	Reserved	SYNCLKNB	VSS	VSS
B	VCC1_8	VSS	Reserved	Reserved	Reserved	Reserved	VCC1_8	VSS	Reserved	STOPB#
C	VSS	Reserved	VSS	RST#	VCC1_8	REFCLKB	Reserved	VSS	Reserved	PWRDNB#
D	CHB_DQA8	VSS	CHB_DQA7	VSS	Reserved	VSS	VCC1_8	VSS	Reserved	VSS
E	CHB_DQA6	VSS	CHB_DQA5	VSS	VSS	VCC1_8	VSS	VCC1_8	VSS	VCC1_8
F	CHB_DQA2	CHB_DQA4	CHB_DQA3	VSS	VCC1_8	VCC1_8				
G	CHB_DQA0	VSS	CHB_DQA1	VSS	VCC1_8	VCC1_8				
H	CHB_CFM	CHB_CFM#	VSS	VSS	VCC1_8					
J	CHB_CTM#	CHB_CTM	VSS	VCC1_8	CHB_VREFA				VSS	VSS
K	CHB_RQ6	VSS	CHB_RQ7	VSS	CHB_VREFB				VSS	VSS
L	CHB_RQ5	CHB_RQ4	CHB_RQ3	VSS	VCC1_8				VSS	VSS
M	CHB_RQ2	VSS	CHB_RQ1	VSS	VCC				VSS	VSS
N	CHB_RQ0	CHB_DQB1	CHB_DQB0	VSS	VCC1_8					
P	CHB_DQB3	VSS	CHB_DQB2	VSS	VCC1_8					
R	CHB_DQB5	CHB_DQB6	CHB_DQB4	VSS	VCC	VCC1_8	VCC1_8			
T	CHB_DQB7	VSS	CHB_DQB8	VCC1_8	VCC1_8	VCC1_8	VCC1_8	VCC1_8	VCC	VCC1_8
U	VSS	CHB_SIO	VSS	VCC1_8	VSS	VSS	VSS	VSS	VSS	VSS
V	CHB_CMD	VSS	VSS	EXDQB8	EXDQB4	EXDQB2	EXDQB0	EXRQ1	EXRQ3	EXP1
W	CHB_SCK	EXSCK	EXSIO	VSS	EXDQB6	VSS	EXDQB1	VSS	EXRQ4	VSS
Y	VSS	EXCMD	VSS	EXDQB7	EXDQB5	EXDQB3	EXRQ0	EXRQ2	EXP0	EXRQ5
	1	2	3	4	5	6	7	8	9	10

Figure 21. MRH-R Ballout (Top View, Right Side)

11	12	13	14	15	16	17	18	19	20	
REFCLKA	VSS	PCLKMA	VSS	SYNCLKNA	VSS	Reserved	Reserved	VCC1_8	VSS	A
Reserved	TESTN#	STOPA#	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	B
Reserved	VSSP	PWRDNA#	Reserved	Reserved	Reserved	Reserved	VCC1_8	VSS	VSS	C
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VSS	CHA_DQA7	VSS	CHA_DQA8	D
VCC1_8	VCC1_8	Reserved	Reserved	Reserved	Reserved	VSS	CHA_DQA5	VSS	CHA_DQA6	E
			VCC1_8	VCC1_8	VCC1_8	VSS	CHA_DQA3	CHA_DQA4	CHA_DQA2	F
					VCC1_8	VSS	CHA_DQA1	VSS	CHA_DQA0	G
					VCC1_8	VSS	VSS	CHA_CFM#	CHA_CFM	H
VSS	VSS				CHA_VREFA	VCC1_8	VSS	CHA_CTM	CHA_CTM#	J
VSS	VSS				CHA_VREFB	VSS	CHA_RQ7	VSS	CHA_RQ6	K
VSS	VSS				VCC1_8	VSS	CHA_RQ3	CHA_RQ4	CHA_RQ5	L
VSS	VSS				VCC1_8	VSS	CHA_RQ1	VSS	CHA_RQ2	M
					VCC1_8	VSS	CHA_DQB0	CHA_DQB1	CHA_RQ0	N
				VCC1_8	VCC1_8	VSS	CHA_DQB2	VSS	CHA_DQB3	P
				VCC1_8	VCC1_8	VSS	CHA_DQB4	CHA_DQB6	CHA_DQB5	R
EXVREFB	EXVREFA	VCC1_8	VCC1_8	VCC1_8	VCC1_8	VCC1_8	CHA_DQB8	VSS	CHA_DQB7	T
VSS	VCC1_8	VSS	VSS	VSS	VSS	VSS	VSS	CHA_SIO	VSSP	U
EXRQ7	VSS	VSS	EXDQA1	EXDQA3	EXDQA5	EXDQA7	VSS	CHA_SCK	CHA_CMD	V
VSS	EXCTM	EXCFM#	VSS	EXDQA4	VSS	VSS	VSS	SMBCLK	MRHSIO	W
EXRQ6	EXCTM#	EXCFM	EXDQA0	EXDQA2	EXDQA6	EXDQA8	VSS	SMBDATA	VSS	Y
11	12	13	14	15	16	17	18	19	20	

Table 4. MRH-R Alphabetical Ball Assignment

Signal	Ball #
CHA_CFM	H20
CHA_CFM#	H19
CHA_CMD	V20
CHA_CTM	J19
CHA_CTM#	J20
CHA_DQA0	G20
CHA_DQA1	G18
CHA_DQA2	F20
CHA_DQA3	F18
CHA_DQA4	F19
CHA_DQA5	E18
CHA_DQA6	E20
CHA_DQA7	D18
CHA_DQA8	D20
CHA_DQB0	N18
CHA_DQB1	N19
CHA_DQB2	P18
CHA_DQB3	P20
CHA_DQB4	R18
CHA_DQB5	R20
CHA_DQB6	R19
CHA_DQB7	T20
CHA_DQB8	T18
CHA_RQ0	N20
CHA_RQ1	M18
CHA_RQ2	M20
CHA_RQ3	L18
CHA_RQ4	L19
CHA_RQ5	L20
CHA_RQ6	K20
CHA_RQ7	K18
CHA_SCK	V19
CHA_SIO	U19
CHA_VREFA	J16
CHA_VREFB	K16
CHB_CFM	H1
CHB_CFM#	H2
CHB_CMD	V1
CHB_CTM	J2
CHB_CTM#	J1

Signal	Ball #
CHB_DQA0	G1
CHB_DQA1	G3
CHB_DQA2	F1
CHB_DQA3	F3
CHB_DQA4	F2
CHB_DQA5	E3
CHB_DQA6	E1
CHB_DQA7	D3
CHB_DQA8	D1
CHB_DQB0	N3
CHB_DQB1	N2
CHB_DQB2	P3
CHB_DQB3	P1
CHB_DQB4	R3
CHB_DQB5	R1
CHB_DQB6	R2
CHB_DQB7	T1
CHB_DQB8	T3
CHB_RQ0	N1
CHB_RQ1	M3
CHB_RQ2	M1
CHB_RQ3	L3
CHB_RQ4	L2
CHB_RQ5	L1
CHB_RQ6	K1
CHB_RQ7	K3
CHB_SCK	W1
CHB_SIO	U2
CHB_VREFA	J5
CHB_VREFB	K5
Reserved	A4
EXCFM	Y13
EXCFM#	W13
EXCMD	Y2
EXCTM	W12
EXCTM#	Y12
EXDQA0	Y14
EXDQA1	V14
EXDQA2	Y15
EXDQA3	V15

Signal	Ball #
EXDQA4	W15
EXDQA5	V16
EXDQA6	Y16
EXDQA7	V17
EXDQA8	Y17
EXDQB0	V7
EXDQB1	W7
EXDQB2	V6
EXDQB3	Y6
EXDQB4	V5
EXDQB5	Y5
EXDQB6	W5
EXDQB7	Y4
EXDQB8	V4
EXP0	Y9
EXP1	V10
EXRQ0	Y7
EXRQ1	V8
EXRQ2	Y8
EXRQ3	V9
EXRQ4	W9
EXRQ5	Y10
EXRQ6	Y11
EXRQ7	V11
EXSCK	W2
EXSIO	W3
EXVREFA	T12
EXVREFB	T11
MRHSIO	W20
PCLKMA	A13
PCLKMB	A6
PWRDNA#	C13
PWRDNB#	C10
REFCLKA	A11
REFCLKB	C6
Reserved	A17
Reserved	A18
Reserved	A3
Reserved	B17
Reserved	B4

Signal	Ball #
Reserved	D13
Reserved	E14
Reserved	D14
Reserved	E15
Reserved	D15
Reserved	E16
Reserved	D16
Reserved	C17
Reserved	D9
Reserved	C9
Reserved	D11
Reserved	B11
Reserved	C11
Reserved	B9
Reserved	D12
Reserved	E13
Reserved	B20
Reserved	D5
Reserved	C14
Reserved	C7
Reserved	B3
Reserved	B6
Reserved	B15
Reserved	B19
Reserved	B16
Reserved	C2
Reserved	C15
Reserved	A7
Reserved	A5
Reserved	B5
Reserved	B14
Reserved	B18
Reserved	A2
Reserved	C16
RST#	C4
SMBCLK	W19
SMBDATA	Y19
STOPA#	B13
STOPB#	B10
SYNCLKNA	A15

Signal	Ball #
SYNCLKNB	A8
TESTN#	B12
VCC1_8	C18
VCC1_8	E11
VCC1_8	F14
VCC1_8	M5
VCC1_8	M16
VCC1_8	R5
VCC1_8	R15
VCC1_8	T9
VCC1_8	U12
VCC1_8	A19
VCC1_8	B1
VCC1_8	B7
VCC1_8	C5
VCC1_8	D7
VCC1_8	E6
VCC1_8	E8
VCC1_8	E10
VCC1_8	E12
VCC1_8	T4
VCC1_8	U4
VCC1_8	F5
VCC1_8	F6
VCC1_8	F15
VCC1_8	F16
VCC1_8	G5
VCC1_8	G6
VCC1_8	G16
VCC1_8	H5
VCC1_8	H16
VCC1_8	J4
VCC1_8	J17
VCC1_8	N5
VCC1_8	N16
VCC1_8	P5
VCC1_8	P15
VCC1_8	P16
VCC1_8	R6
VCC1_8	R7
VCC1_8	R16

Signal	Ball #
VCC1_8	T5
VCC1_8	T6
VCC1_8	T7
VCC1_8	T8
VCC1_8	T13
VCC1_8	T14
VCC1_8	T15
VCC1_8	T16
VCC1_8	T17
VCC1_8	L16
VCC1_8	L5
VCC1_8	T10
VSS	A1
VSS	A12
VSS	A20
VSS	C3
VSS	C8
VSS	C19
VSS	C20
VSS	D8
VSS	H4
VSS	J9
VSS	J10
VSS	J11
VSS	J12
VSS	K9
VSS	K10
VSS	K11
VSS	K12
VSS	L9
VSS	L10
VSS	L11
VSS	L12
VSS	M9
VSS	M10
VSS	M11
VSS	M12
VSS	U3
VSS	U13
VSS	U18
VSS	V2

Signal	Ball #
VSS	V3
VSS	V18
VSS	W18
VSS	Y1
VSS	Y20
VSS	A9
VSS	A10
VSS	A14
VSS	A16
VSS	B2
VSS	B8
VSS	C1
VSS	C12
VSS	D6
VSS	D10
VSS	E5
VSS	E7
VSS	E9
VSS	U1
VSS	U20
VSS	Y3
VSS	D2
VSS	D4
VSS	D17
VSS	D19
VSS	E2
VSS	E4
VSS	E17
VSS	E19
VSS	F4
VSS	F17
VSS	G2
VSS	G4
VSS	G17
VSS	G19
VSS	H3
VSS	H17
VSS	H18
VSS	J3
VSS	J18
VSS	K2

Signal	Ball #
VSS	K4
VSS	K17
VSS	K19
VSS	L4
VSS	L17
VSS	M2
VSS	M4
VSS	M17
VSS	M19
VSS	N4
VSS	N17
VSS	P2
VSS	P4
VSS	P17
VSS	P19
VSS	R4
VSS	R17
VSS	T2
VSS	T19
VSS	U5
VSS	U6
VSS	U7
VSS	U8
VSS	U9
VSS	U10
VSS	U11
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	V12
VSS	V13
VSS	W4
VSS	W6
VSS	W8
VSS	W10
VSS	W11
VSS	W14
VSS	W16
VSS	W17
VSS	Y18

5.2. Package Specifications

This section shows the mechanical dimensions for the MRH-R device. The package is a 324 Ball Grid Array (BGA).

Figure 22. Package Dimensions (324 BGA) – Top and Side Views

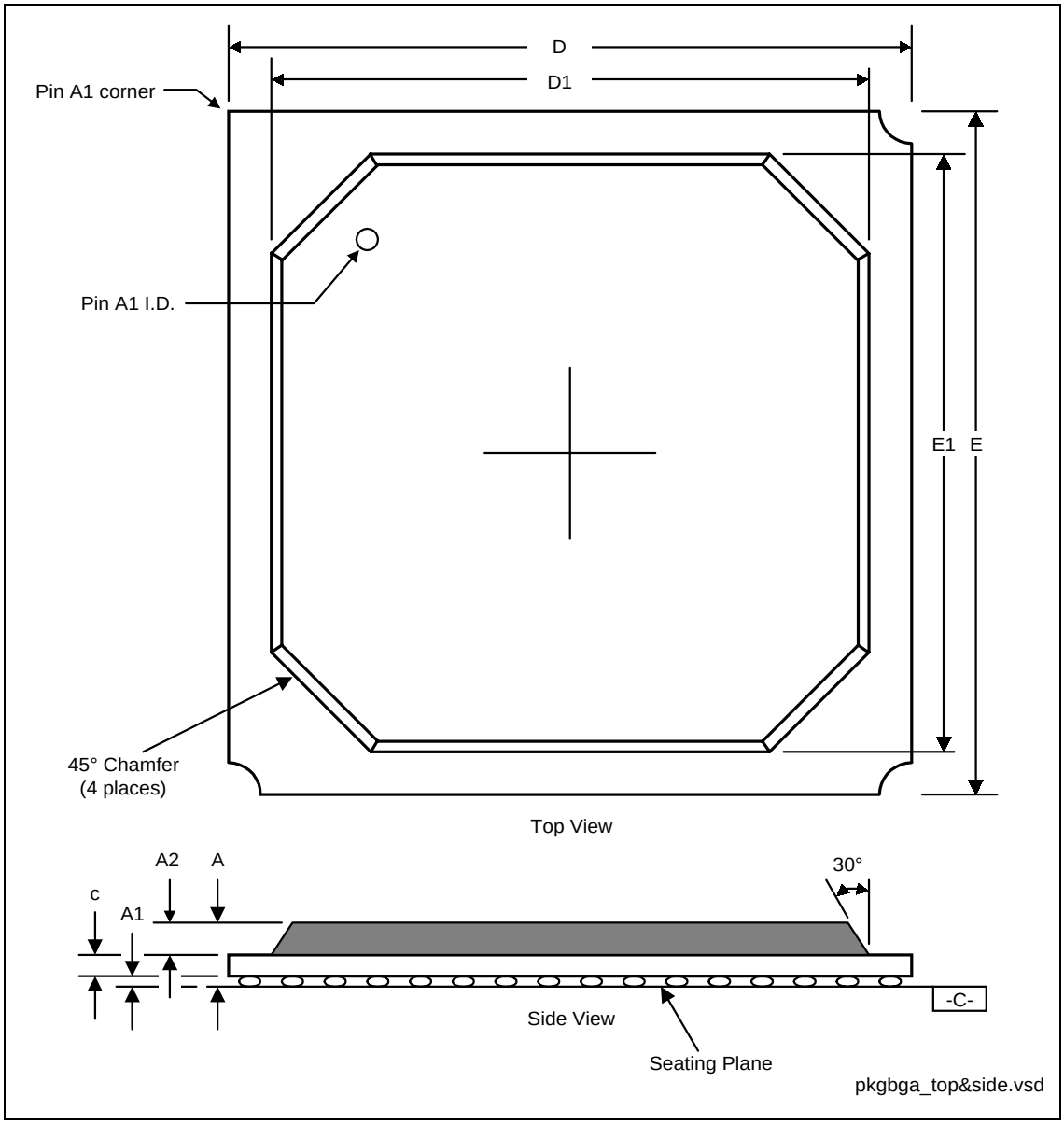

Figure 23. Package Dimensions (324 BGA) – Bottom View

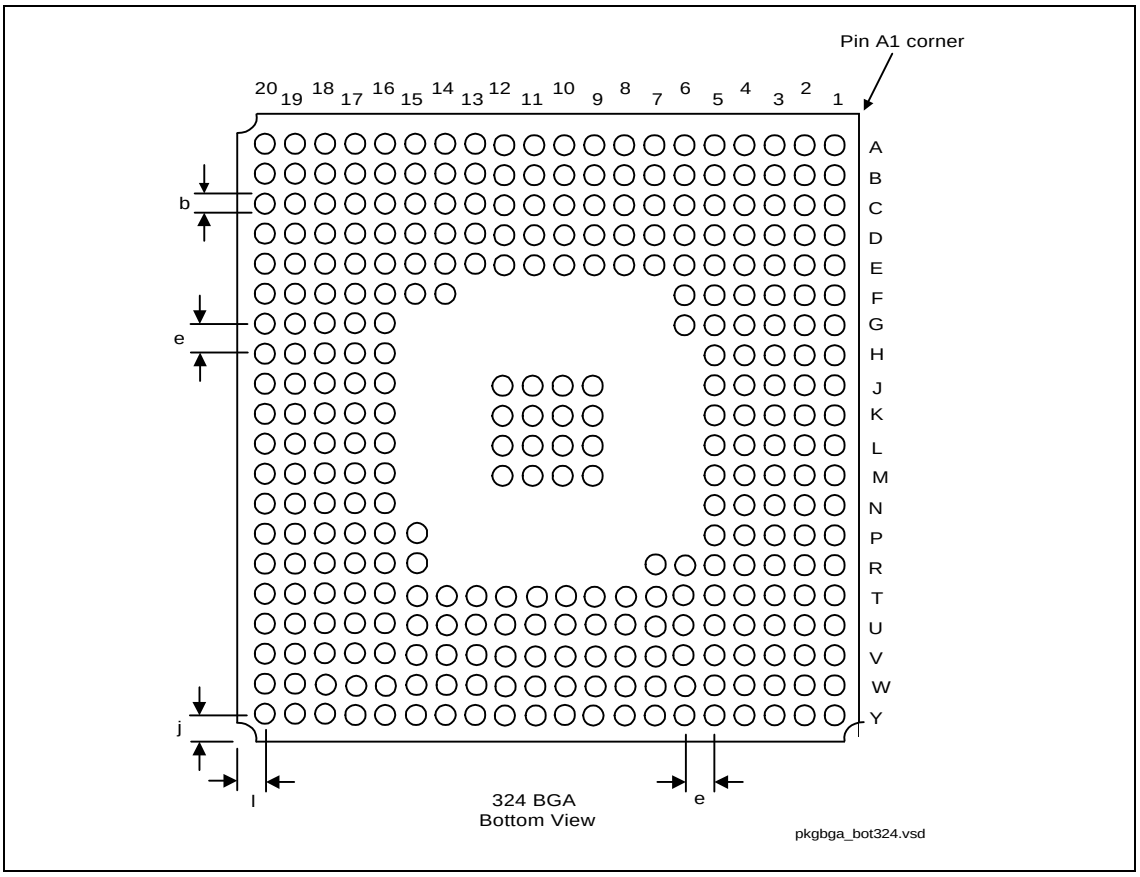

Table 5. BGA Package Dimensions (324 BGA)

Symbol	Min	Nominal	Max	Units	Note
A	2.17	2.38	2.59	mm	
A1	0.50	0.60	0.70	mm	
A2	1.12	1.17	1.22	mm	
D	26.80	27.00	27.20	mm	
D1	23.80	24.00	24.70	mm	
E	26.90	27.00	27.10	mm	
E1	23.80	24.00	24.20	mm	
e	1.27 (solder ball pitch)			mm	
l	1.44 REF.			mm	
J	1.44 REF.			mm	
M	20 x 20 Matrix			mm	
b^2	0.60	0.75	0.90	mm	
c	0.55	0.61	0.67	mm	

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5-1982
2. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-)
3. Primary Datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

5.3. MRH-R RSL Normalized Trace Length Data

These lengths must be considered when matching trace lengths as described in the design guide. Note that these lengths in Table 6 are normalized to 0 with the longest trace on the package. They do not represent the actual lengths from pad to ball.

The following formula is used to determine ΔL_{PCB}

$$\Delta L_{PCB} = (\Delta L_{pkg} * V_{pkg}) / V_{PCB}$$

ΔL_{PCB} is the nominal Δ PCB trace length to be added on the PCB

ΔL_{Pkg} is the nominal Δ package trace length

V_{pkg} is the package trace velocity, and the nominal value is 180 ps/in

V_{PCB} is the PCB trace velocity

The data given can be renormalized to start routing from a different ball. If a different RSL signal (other than longest trace) is used for nominalization, simply use the following equation:

$$\text{New } \Delta L_{pkg}' = \Delta L_{pkg} - \Delta L_{RSL}$$

For example: For the MCH, if MCH CHA_CFM trace length is used for nominalization, then:

Signal	ΔL_{PKG} (mils)	New ΔL_{PKG} (mils)
CHA_CFM	102.756	0.000
CHA_CFM#	118.897	16.142
CHA_CTM	130.315	27.559
:	:	:
:	:	:
CHA_RQ6	124.409	21.653
CHA_RQ7	175.984	73.228

Table 6. MRH-R RSL Normalized Trace Length Data

Stick Channel A (ΔL_{Pkg} Normalized to CHA_DQB7)		
Signal	**Ball**	**ΔLPKG (mils)**
CHA_CFM	H20	82.894
CHA_CFM#	H19	84.842
CHA_CTM	J19	88.012
CHA_CTM#	J20	98.870
CHA_DQA0	G20	36.720
CHA_DQA1	G18	123.334
CHA_DQA2	F20	53.642
CHA_DQA3	F18	150.862
CHA_DQA4	F19	105.830
CHA_DQA5	E18	122.409
CHA_DQA6	E20	43.421
CHA_DQA7	D18	99.968
CHA_DQA8	D20	20.142
CHA_DQB0	N18	138.826
CHA_DQB1	N19	119.094
CHA_DQB2	P18	138.456
CHA_DQB3	P20	49.177
CHA_DQB4	R18	140.145
CHA_DQB5	R20	19.417
CHA_DQB6	R19	89.212
CHA_DQB7	T20	0.000
CHA_DQB8	T18	74.252
CHA_RQ0	N20	74.086
CHA_RQ1	M18	183.972
CHA_RQ2	M20	92.366
CHA_RQ3	L18	179.114
CHA_RQ4	L19	150.244
CHA_RQ5	L20	94.268
CHA_RQ6	K20	92.897
CHA_RQ7	K18	150.779

Stick Channel B (ΔL_{Pkg} Normalized to CHB_DQB7)		
Signal	**Ball**	**ΔLPKG (mils)**
CHB_CFM	H1	84.563
CHB_CFM#	H2	86.216
CHB_CTFM	J2	88.342
CHB_CTM#	J1	95.705
CHB_DQA0	G1	77.468
CHB_DQA1	G3	125.827
CHB_DQA2	F1	55.697
CHB_DQA3	F3	153.067
CHB_DQA4	F2	108.004
CHB_DQA5	E3	124.114
CHB_DQA6	E1	49.992
CHB_DQA7	D3	100.893
CHB_DQA8	D1	20.626
CHB_DQB0	N3	181.637
CHB_DQB1	N2	119.110
CHB_DQB2	P3	141.716
CHB_DQB3	P1	56.236
CHB_DQB4	R3	137.606
CHB_DQB5	R1	25.590
CHB_DQB6	R2	96.397
CHB_DQB7	T1	0.000
CHB_DQB8	T3	94.543
CHB_RQ0	N1	81.094
CHB_RQ1	M3	186.909
CHB_RQ2	M1	91.319
CHB_RQ3	L3	183.633
CHB_RQ4	L2	148.590
CHB _RQ5	L1	93.929
CHB _RQ6	K1	95.295
CHB _RQ7	K3	151.212

Expansion Channel (ΔL_{Pkg} Normalized to EXDQB3)		
Signal	**Ball**	**ΔLPKG (mils)**
EXP0	Y9	103.968
CHB_CFM	Y13	112.852
CHB_CFM#	W13	112.649
CHB_CTFM	W12	116.543
CHB_CTM#	Y12	119.141
CHB_DQA0	Y14	101.905
CHB_DQA1	V14	149.193
CHB_DQA2	Y15	79.370
CHB_DQA3	V15	174.787
CHB_DQA4	W15	135.519
CHB_DQA5	V16	148.389
CHB_DQA6	Y16	65.901
CHB_DQA7	V17	120.508
CHB_DQA8	Y17	40.894
CHB_DQB0	V7	153.697
CHB_DQB1	W7	122.338
CHB_DQB2	V6	148.854
CHB_DQB3	Y6	0.000
CHB_DQB4	V5	101.649
CHB_DQB5	Y5	36.807
CHB_DQB6	W5	62.712
CHB_DQB7	Y4	12.807
CHB_DQB8	V4	98.382
EXP1	V10	218.665
CHB_RQ0	Y7	89.964
CHB_RQ1	V8	159.933
CHB_RQ2	Y8	103.795
CHB_RQ3	V9	171.783
CHB_RQ4	W9	124.803
CHB _RQ5	Y10	108.547
CHB _RQ6	Y11	113.972
CHB _RQ7	V11	205.712

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6. Testability

The MRH-R supports the following test modes.

Table 7. MRH-R Test Modes

Number of Clocks TEST# Driven Low	Test Mode
< 4	No Test Mode Selected
5	Reserved. Do Not Attempt
6	All 'Z'
7-8	Reserved. Do Not Attempt
9	XOR Chain
10-63	Reserved. Do Not Attempt

Note: The ExSCK clock on the MRH-R should be referenced when asserting the signal TEST# low for activation of the supported test features of the MRH-R.

6.1. Tri-state Mode

The Tri-state test mode is activated by asserting the TEST# signal low for 6 clocks. All outputs and bi-directional pins are tri-stated, including the XOR tree outputs.

6.2. XOR Chain Mode

The MRH-R has 4 XOR chains. This test mode activates by asserting the TEST# signals low for 7 clocks. This test mode can be used to check the connectivity of the pins. The individual XOR chains can be observed with the XOROUT pins defined in the following table.

XOR Output Pin	XOR Chain #
Reserved (pin D9)	0
Reserved (pin D11)	2
Reserved (pin B11)	3
Reserved (pin C11)	4

Since the CFM and CFM# pins are connected directly to the CTM and CTM# pins, the CFM, and CFM# pins are not part of the XOR chain. We can test connectivity of the CFM, and CFM# pins by driving a value on the CFM and CFM# pins, and probing them on the CTM and CTM# pins.

Table 8. MRH-R XOR Chains

XOR Chain 0	XOR Chain 2	XOR Chain 3	XOR Chain 4	Not in XOR Chain
CHB_SIO	EXDQA8	CHA_DQA8	CHB_DQA8	EXCFM
CHB_CMD	EXDQA7	CHA_DQA7	CHB_DQA7	EXCFM#
CHB_SCK	EXDQA6	CHA_DQA6	CHB_DQA6	CHA_CFM
EXSIO	EXDQA5	CHA_DQA5	CHB_DQA5	CHA_CFM#
EXCMD	EXDQA4	CHA_DQA4	CHB_DQA4	CHB_CFM
MRHSIO	EXDQA3	CHA_DQA3	CHB_DQA3	CHB_CFM#
SMBDATA	EXDQA2	CHA_DQA2	CHB_DQA2	RST#
SMBCLK	EXDQA1	CHA_DQA1	CHB_DQA1	TEST#
CHA_CMD	EXDQA0	CHA_DQA0	CHB_DQA0	
CHA_SCK	EXCTM	CHA_CTM	CHB_CTM	
CHA_SIO	EXCTM#	CHA_CTM#	CHB_CTM#	
SYNCLKNA	EXRQ_7	CHA_RQ7	CHB_RQ7	
PWRDNA#	EXRQ_6	CHA_RQ6	CHB_RQ6	
STOPA#	EXRQ_5	CHA_RQ5	CHB_RQ5	
PCLKMA	EXP1	CHA_RQ4	CHB_RQ4	
REFCLKA	EXP0	CHA_RQ3	CHB_RQ3	
PWRDNB#	EXRQ_4	CHA_RQ2	CHB_RQ2	
STOPB#	EXRQ_3	CHA_RQ1	CHB_RQ1	
SYNCLKNB	EXRQ_2	CHA_RQ0	CHB_RQ0	
PCLKMB	EXRQ_1	CHA_DQB0	CHB_DQB0	
REFCLKB	EXRQ_0	CHA_DQB1	CHB_DQB1	
	EXDQB0	CHA_DQB2	CHB_DQB2	
	EXDQB1	CHA_DQB3	CHB_DQB3	
	EXDQB2	CHA_DQB4	CHB_DQB4	
	EXDQB3	CHA_DQB5	CHB_DQB5	
	EXDQB4	CHA_DQB6	CHB_DQB6	
	EXDQB5	CHA_DQB7	CHB_DQB7	
	EXDQB6	CHA_DQB8	CHB_DQB8	
	EXDQB7			
	EXDQB8			