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Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller

Hardware Reference Manual

Order Number: EC–QWC4D–TE

Revision/Update Information: This manual supersedes the *Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual* (EC–QWC4C–TE).

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Maynard, Massachusetts

http://www.digital.com/semiconductor

May 1997

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Purpose and Audience

The Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual describes the operation of the Digital Semiconductor 21143 10/100-Mb/s Ethernet LAN Controller (also referred to as the 21143). This manual is for designers who use the 21143.

Manual Organization

This manual contains eight chapters, six appendixes, and an index.

- Chapter 1, Introduction, includes a general description of the 21143. It also provides an overview of the 21143 hardware components.
- Chapter 2, Signal Descriptions, provides the physical layout of the 21143 and describes each of the input and output signals.
- Chapter 3, Registers, provides a complete bit description of the 21143 command and status registers (CSRs) and the configuration registers.
- Chapter 4, Host Communication, describes how the 21143 communicates with the host by using descriptor lists and data buffers. It also describes the transmit and receive processes.
- Chapter 5, Host Bus Operation, provides a description of the read, write, and termination cycles.
- Chapter 6, Network Interface Operation, describes the MII, 10BASE-T, and AUI ports. It includes a complete description of media access control (MAC) operations. It also provides detailed transmitting and receiving operation information.
- Chapter 7, External Ports, describes the interface and operation of the MicroWire serial ROM, the boot ROM, the general-purpose port, and the network activity LEDs.

- Chapter 8, Remotely Waking Up the LAN, describes how to remotely power up a sleeping workstation.[1]
- Appendix A, Joint Test Action Group—Test Logic, provides descriptions of testing, observing, and modifying circuit activity during normal operation.
- Appendix B, DNA CSMA/CD Counters and Events Support, describes features that support the driver in implementing and reporting the specified counters and events.
- Appendix C, Hash C Routine, provides an example of a C routine that generates a hash index for a given Ethernet address.
- Appendix D, Port Selection Procedure, provides information about selecting the MII, 10BASE-T, AUI, and BNC ports.
- Appendix E, General-Purpose Port and LED Programming, contains information about general-purpose port and LED programming.
- Appendix F, Support, Products, and Documentation, contains information about technical support and ordering information.

Document Conventions

Some tables use the values 1, 0, and X. An X signifies a don't care (1 or 0) convention, which can be determined by the system designer.

In Chapters 3, 4, and 8, all shaded bits in the figures are reserved and should be written by the driver as 0.

[1]This feature is not supported on the 21143–PA and the 21143–TA.

1
Introduction

This chapter provides a general description of the Digital Semiconductor 21143 10/100-Mb/s PCI/CardBus Ethernet LAN Controller (21143), its features, and an overview of the hardware.

1.1 General Description

The 21143 is an Ethernet LAN controller for both 100-Mb/s and 10-Mb/s data rates, which provides a direct interface to the peripheral component interconnect (PCI) local bus or the CardBus. The 21143 interfaces to the host processor by using onchip command and status registers (CSRs) and a shared host memory area, set up mainly during initialization. This minimizes processor involvement in the 21143 operation during normal reception and transmission.

Large FIFOs allow the 21143 to efficiently operate in systems with longer latency periods. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without a repeated fetch from the host memory. The 21143 provides an upgradable boot ROM interface.

The 21143 provides three network ports: a 10BASE-T 10-Mb/s port, an attachment unit interface (AUI) 10-Mb/s port, and a media-independent/symbol interface (MII/SYM) 10/100-Mb/s port. The 10BASE-T port provides a direct Ethernet connection to the twisted-pair (TP) interface. The AUI port provides a direct Ethernet connection to the AUI. The 10/100-Mb/s port supports two operational modes:

- MII mode—A full implementation of the MII standard
- SYM mode—Symbol interface to an external 10/100-Mb/s front-end decoder (ENDEC). In this mode the 21143 uses an onchip physical coding sublayer (PCS) and a scrambler/descrambler circuit to enable a low-cost 100BASE-T implementation.

The 21143 is capable of functioning in a full-duplex environment for the MII/SYM and 10BASE-T ports.

1.2 Features

The 21143 has the following features:

- Contains onchip PCS and scrambler/descrambler for 100BASE-TX
- Contains onchip integrated AUI port and a 10BASE-T transceiver
- Supports autodetection between 10BASE-T, AUI, and MII/SYM ports
- Supports IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex operation for 10 Mb/s and 100 Mb/s (NWAY)
- Contains large independent receive and transmit FIFOs
- Provides an upgradable boot ROM interface up to 256KB
- Supports PCI and CardBus interfaces
- Supports the advanced PCI read multiple, read line, and write and invalidate commands
- Includes a powerful onchip direct memory access (DMA) with programmable burst size, providing low CPU utilization
- Supports an unlimited PCI burst
- Supports early interrupt on transmit and receive
- Contains a variety of flexible address filtering modes
- Offers a unique, patented solution to Ethernet capture-effect problem
- Supports PCI clock speed frequency from dc to 33 MHz; network operation with PCI clock from 20 MHz to 33 MHz
- Supports automatic loading of subvendor ID and CardBus card information structure (CIS) pointer from serial ROM to configuration registers
- Supports big or little endian byte ordering for buffers and descriptors
- Supports full-duplex operation on both MII/SYM and 10BASE-T ports
- Implements power management with two power-saving modes (sleep and snooze)
  - Powers up in sleep mode
  - Requires less than 70 mA of supply current after power-up
- Provides internal and external loopback capability on all network ports

- Provides MicroWire interface for serial ROM (1K and 4K EEPROM)
- Provides LED support for various network activity indications
- Supports interrupts from two general-purpose pins
- Implements test-access port (JTAG-compatible) with boundary-scan pins
- Implements low-power, 3.3-V CMOS technology
- Enables automatic detection and correction of 10BASE-T receive polarity
- Implements unique, patent-pending intelligent arbitration between DMA channels to minimize underflow or overflow
- Supports three network ports: 10BASE-T (10 Mb/s), AUI (10 Mb/s), and MII/SYM (10/100 Mb/s)
- Contains a 4-bit, general-purpose programmable register and corresponding I/O pins
- Supports IEEE 802.3 and ANSI 8802-3 Ethernet standards
- Supports remote wake-up-LAN, which is a feature based upon Advanced Micro Device's Magic Packet technology that allows sleeping workstations to be remotely powered-up.[1]
- Supports SecureON,™ which is a security feature that can be added to the Advanced Micro Device's Magic Packet technology.[1]

1.3 Microarchitecture

The following list describes the 21143 hardware components, and Figure 1–1 shows a block diagram of the 21143:

- PCI/CardBus interface—Includes all interface functions to the PCI or CardBus bus, handles all interconnect control signals, and executes DMA and I/O transactions
- Boot ROM port—Provides an interface to perform read and write operations to the boot ROM, supports accesses to bytes or longwords (32-bit), and provides the ability to connect an external 8-bit register to the boot ROM port

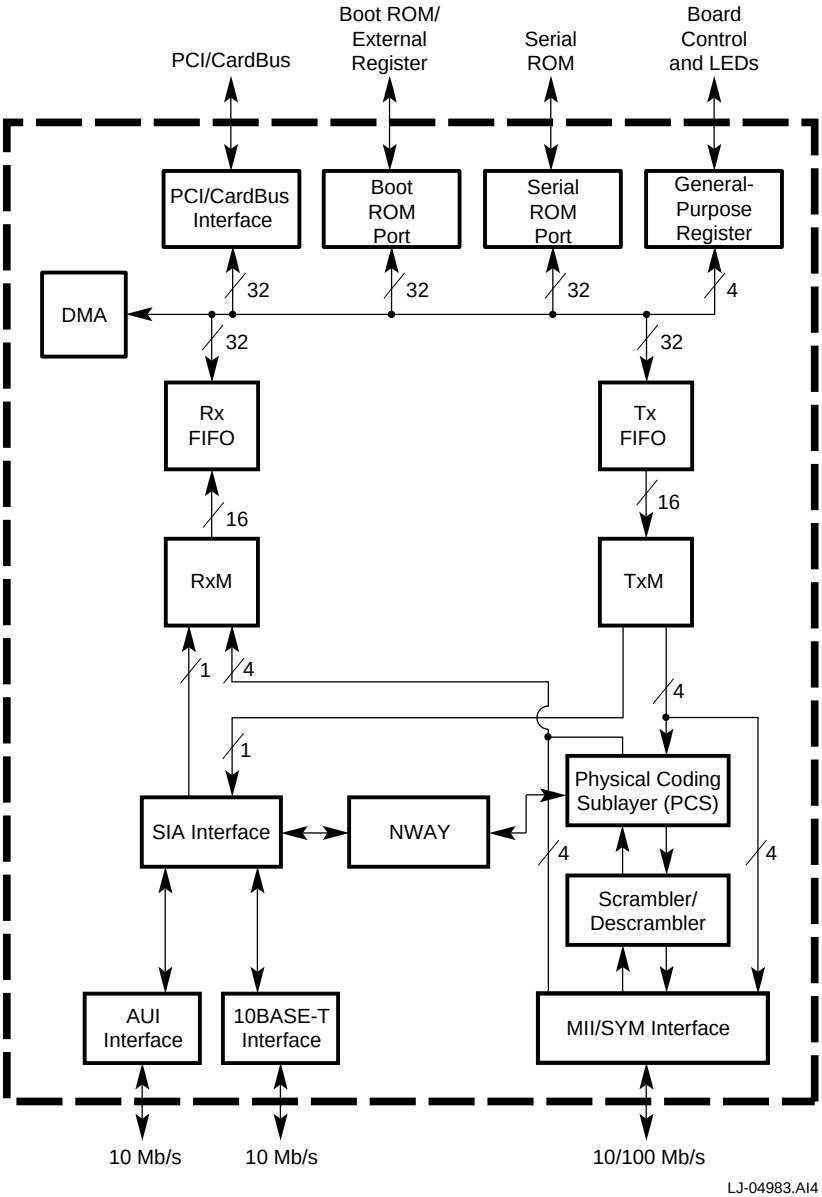
[1]This feature is not supported on the 21143–PA and the 21143–TA.

- Serial ROM port—Provides a direct interface to a MicroWire ROM for storage of the Ethernet address and system parameters
- General-purpose register—Enables software use for input or output functions and LEDs
- DMA—Contains independent receive and transmit controller and handles data transfers between CPU memory and onchip memory
- FIFOs—Contains independent FIFOs for receive and transmit and supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit
- RxM—Handles all CSMA/CD[1] receive operations and transfers the data from the ENDEC to the receive FIFO
- TxM—Handles all CSMA/CD MAC[2] transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission
- SIA interface—Performs 10-Mb/s physical layer network operations and implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions
- NWAY—Implements the IEEE 802.3 autonegotiation algorithm
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification, including the squelch feature
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme for 100BASE-TX
- Three network interfaces—An AUI interface, a 10BASE-T interface, and an MII/SYM interface provide a full MII signal interface and direct interface to the 100-Mb/s ENDEC for CAT5

[1]Carrier-sense multiple access with collision detection

[2]Media access control

Figure 1–1 21143 Block Diagram



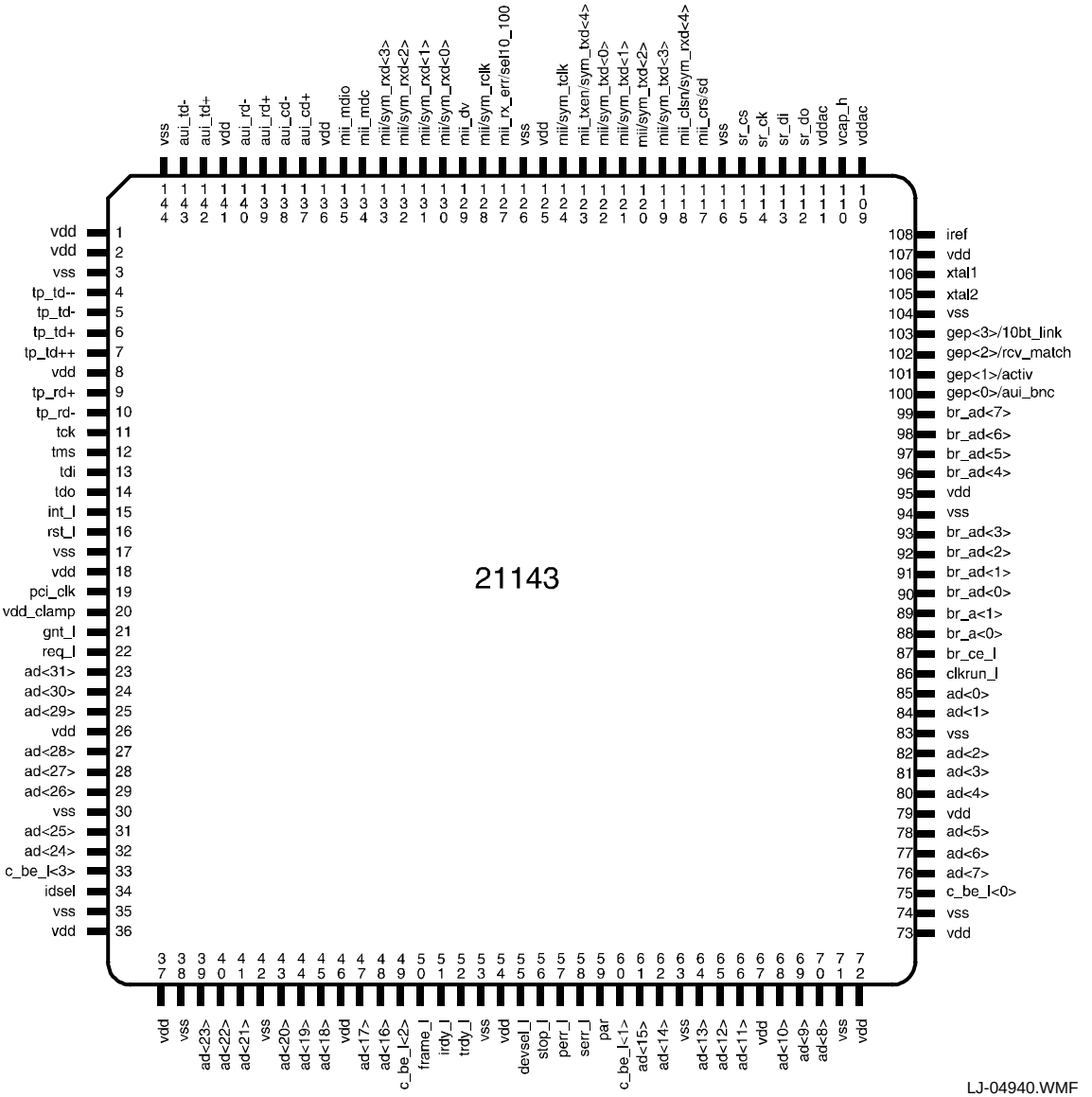
2
Signal Descriptions

This chapter describes the 21143 signals.

2.1 21143 Pinout

The 21143 is offered in two package styles: a 144-pin PQFP and a 144-pin TQFP. Figure 2–1 shows the 21143 pinout used by both package types.

Figure 2–1 21143 Pinout Diagram (Top View)



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2.2 Signal Descriptions

The following terms describe the 21143 pinout used in Table 2–1:

- **Address phase**

  Address and appropriate bus commands are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable codes are driven during this cycle.

- **_l**

  All pin names with the _l suffix are asserted low.

The following abbreviations are used in Table 2–1:

O = Output

I/O = Input/output

O/D = Open drain

P = Power

The following signals have an internal pull-up:

tms

tdi

br_ce_l

sr_do

mii/sym_tclk

Signal **sr_cs** has an internal pull-down.

Signal Descriptions

Table 2–1 provides a functional description of each of the 21143 signals. These signals are listed alphabetically.

Table 2–1 Functional Description of 21143 Signals *(Sheet 1 of 8)*

Signal	Type	Pin Number	Description
ad<31:0>	I/O	See Figure 2–1.	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain 32 bits of data. A 21143 bus transaction consists of an address phase followed by one or more data phases. The 21143 supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.
aui_cd–	I	138	Attachment unit interface receive collision differential negative data.
aui_cd+	I	137	Attachment unit interface receive collision differential positive data.
aui_rd–	I	140	Attachment unit interface receive differential negative data.
aui_rd+	I	139	Attachment unit interface receive differential positive data.
aui_td–	O	143	Attachment unit interface transmit differential negative data.
aui_td+	O	142	Attachment unit interface transmit differential positive data.
br_a<0>	O	88	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.
br_a<1>	O	89	Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.
br_ad<7:0>	I/O	See Figure 2–1.	Boot ROM address and data multiplexed lines bits 7 through 0. In two consecutive address cycles, these lines contain the boot ROM address pins 7 through 2, **oe_l** and **we_l** in the first cycle; and these lines contain boot ROM address pins 15 through 8 in the second cycle. During the data cycle, bits 7 through 0 contain data.
br_ce_l	O	87	Boot ROM or external register chip enable.

Table 2–1 Functional Description of 21143 Signals *(Sheet 2 of 8)*

Signal	Type	Pin Number	Description
c_be_l<3:0>	I/O	See Figure 2–1.	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these 4 bits provide the bus command. During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.
clkrun_l	I/O O/D	86	CardBus clock run indicates the clock status. The host system asserts this signal to indicate normal operation of the clock. The host system deasserts **clkrun_l** when the clock is going to be slowed down to a nonoperational frequency. The 21143 samples **clkrun_l** and when the signal is found deasserted, the 21143 asserts **clkrun_l**, requesting that normal clock operation be maintained.
devsel_l	I/O	55	Device select is asserted by the target of the current bus access. When the 21143 is the initiator of the current bus access, it expects the target to assert **devsel_l** within 5 bus cycles, confirming the access. If the target does not assert **devsel_l** within the required bus cycles, the 21143 aborts the cycle. To meet the timing requirements, the 21143 asserts this signal in a medium speed (within 2 bus cycles).
frame_l	I/O	50	The **frame_l** signal is driven by the 21143 (bus master) to indicate the beginning and duration of an access. The **frame_l** signal asserts to indicate the beginning of a bus transaction. While **frame_l** is asserted, data transfers continue. The **frame_l** signal deasserts to indicate that the next data phase is the final data phase transaction.
gep<0>/aui_bnc	I/O	100	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. It can provide an interrupt when it is an input pin. • A control pin that provides an AUI (10BASE5) or BNC (10BASE2) select line. This pin is mainly used to enable the external BNC transceiver in 10BASE2 mode. When set, the 10BASE5 mode is selected. When reset, the 10BASE2 mode is selected.

Table 2–1 Functional Description of 21143 Signals *(Sheet 3 of 8)*

Signal	Type	Pin Number	Description
gep<1>/activ	I/O	101	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. It can provide an interrupt when it is an input pin • A status pin that provides an LED that indicates either receive or transmit activity
gep<2>/ rcv_match	I/O	102	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED that indicates a receive packet has passed address recognition.
gep<3>/10bt_link	I/O	103	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED that indicates that the 10BASE-T link integrity test has completed successfully after the link was down.
gnt_l	I	21	Bus grant asserts to indicate to the 21143 that access to the bus is granted.
idsel	I	34	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21143.
int_l	O/D	15	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 21143 deasserts **int_l** for one cycle to support edge-triggered systems. This pin must be pulled up by an external resistor.
iref	I	108	Current reference input for the analog phase-locked loop logic.

Table 2–1 Functional Description of 21143 Signals *(Sheet 4 of 8)*

Signal	Type	Pin Number	Description
irdy_l	I/O	51	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both **irdy_l** and target ready **trdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21143 is the bus master, **irdy_l** is asserted during write operations to indicate that valid data is present on the 32-bit **ad** lines. During read operations, the 21143 asserts **irdy_l** to indicate that it is ready to accept data.
mii_clsn/ sym_rxd<4>	I	118	In MII mode (CSR6<18>=1, CSR6<23>=0), this pin functions as the collision detect. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. In SYM mode (CSR6<18>=1, CSR6<23>=1), this pin functions as receive data. This line along with the four receive lines (**sym_rxd<4:0>**) provides five parallel data lines in symbol form. This data is controlled by an external physical layer medium-dependent (PMD) device and should be synchronized to the **sym_rclk** signal.
mii_crs/sd	I	117	In MII mode this pin functions as the carrier sense and is asserted by the PHY when the media is active. In SYM mode this pin functions as the signal detect indication. It is controlled by an external PMD device.
mii_dv	I	129	Data valid is asserted by an external PHY when receive data is present on the **mii_rxd** lines and is deasserted at the end of the packet. This signal should be synchronized with the **mii_rclk** signal.
mii_mdc	O	134	MII management data clock is sourced by the 21143 to the PHY devices as a timing reference for the transfer of information on the **mii_mdio** signal.
mii_mdio	I/O	135	MII management data input/output transfers control information and status between the PHY and the 21143.
mii/sym_rclk	I	128	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.

Table 2–1 Functional Description of 21143 Signals *(Sheet 5 of 8)*

Signal	Type	Pin Number	Description
mii_rx_err/ sel10_100	I/O	127	In MII mode (CSR6<18>=1, CSR6<23>=0), this pin functions as receive error. It is asserted when a data decoding error is detected by an external PHY device. This signal is synchronized to **mii_rclk** and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0). In SYM mode (CSR6<23>=1), this pin functions as select 10/100. The signal **sel10_100** equals 1 when the 21143 is in 100-Mb/s SYM mode (CSR6<18>=1) and equals 0 when the 21143 is in 10BASE-T/AUI mode (CSR6<18>=0).
mii/sym_rxd<3:0>	I	See Figure 2–1.	Four parallel receive data lines. This data is driven by an external PHY that attached the media and should be synchronized with the **mii_rclk** signal.
mii/sym_tclk	I	124	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external PMD device. This clock should always be active.
mii/sym_txd<3:0>	O	See Figure 2–1.	Four parallel transmit data lines. This data is synchronized to the assertion of the **mii_tclk** signal and is latched by the external PHY on the rising edge of the **mii_tclk** signal.
mii_txen/ sym_txd<4>	O	123	In MII mode, this pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY device. In SYM mode, this pin functions as transmit data. This line along with the four data transmit lines (**sym_txd<3:0>**) provides five parallel data lines in symbol form. The data is synchronized to the rising edge of the **sym_tclk** signal.
par	I/O	59	Parity is calculated by the 21143 as an even parity bit for the 32-bit **ad** and 4-bit **c_be_l** lines. During address and data phases, parity is calculated on all the **ad** and **c_be_l** lines whether or not any of these lines carry meaningful information.
pci_clk	I	19	The clock provides the timing for the 21143 related PCI bus transactions. All the bus signals are sampled on the rising edge of **pci_clk**. The clock frequency range is between 20 MHz and 33 MHz.

Table 2–1 Functional Description of 21143 Signals *(Sheet 6 of 8)*

Signal	Type	Pin Number	Description
perr_l	I/O	57	Parity error asserts when a data parity error is detected. When the 21143 is the bus master and a parity error is detected, the 21143 asserts both CSR5 bit 13 (fatal bus error) and CFCS bit 24 (data parity report). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 21143 continues its operation. The 21143 asserts **perr_l** when a data parity error is detected in either a master-read or a slave-write operation. This pin must be pulled up by an external resistor.
req_l	O	22	Bus request is asserted by the 21143 to indicate to the bus arbiter that it wants to use the bus.
rst_l	I	16	Resets the 21143 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
serr_l	O/D	58	If an address parity error is detected and CFCS bit 8 (**serr_l** enable) is enabled, 21143 asserts both **serr_l** (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. This pin must be pulled up by an external resistor.
sr_ck	O	114	Serial ROM clock signal.
sr_cs	O	115	Serial ROM chip-select signal.
sr_di	O	113	Serial ROM data-in signal.
sr_do	I	112	Serial ROM data-out signal.
stop_l	I/O	56	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21143 responds to the assertion of **stop_l** when it is the bus master, either to disconnect, retry, or abort.
tck	I	11	JTAG clock shifts state information and test data into and out of the 21143 during JTAG test operations. This pin should not be left unconnected.
tdi	I	13	JTAG data in is used to serially shift test data and instructions into the 21143 during JTAG test operations. If the JTAG port is unused this pin may be left unconnected.

Table 2–1 Functional Description of 21143 Signals *(Sheet 7 of 8)*

Signal	Type	Pin Number	Description
tdo	O	14	JTAG data out is used to serially shift test data and instructions out of the 21143 during JTAG test operations.
tms	I	12	JTAG test mode select controls the state operation of JTAG testing in the 21143. If the JTAG port is unused this pin may be left unconnected.
tp_rd–	I	10	Twisted-pair negative differential receive data from the twisted-pair lines.
tp_rd+	I	9	Twisted-pair positive differential receive data from the twisted-pair lines.
tp_td– **tp_td– –**	O O	5 4	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ **tp_td+ +**	O O	6 7	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
trdy_l	I/O	52	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **trdy_l** and **irdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21143 is the bus master, target ready is asserted by the bus slave on the read operation, which indicates that valid data is present on the **ad** lines. During a write cycle, it indicates that the target is prepared to accept data.
vcap_h	I	110	Capacitor input for analog phase-locked loop logic.
vdd	P	See Figure 2–1.	3.3-V supply input voltage.
vddac	P	109, 111	Supplies +3.3-V input for analog phase-locked loop logic.
vdd_clamp	P	20	Supplies +5-V or +3.3-V reference for clamp logic.

Table 2–1 Functional Description of 21143 Signals *(Sheet 8 of 8)*

Signal	Type	Pin Number	Description
vss	P	See Figure 2–1.	Ground pins.
xtal1	I	106	20-MHz crystal input or crystal oscillator input.
xtal2	O	105	Crystal feedback output pin used for crystal connections only. If this pin is unused, then it should be unconnected

3
Registers

This chapter describes the configuration registers, and the command and status registers (CSRs) of the 21143. The 21143 uses 11 configuration registers for initialization and configuration, and 16 CSRs (CSR0 through CSR15) for host communication. Configuration registers are used to identify and query the 21143. The CSRs, which are mapped in the host I/O or memory address space, are used for initialization, pointers, commands, and status reporting.

Note: All shaded bits in the figures in this chapter are reserved and should be written by the driver as zero.

3.1 Configuration Operation

The 21143 enables a full software-driven initialization and configuration. This permits the software to identify and query the 21143.

The 21143 treats configuration space write operations to registers that are reserved as no-ops. That is, the access completes normally on the bus and the data is discarded. Read accesses, to reserved or unimplemented registers, complete normally and a data value of 0 is returned.

Software reset (CSR0<0>) has no effect on the configuration registers. Hardware reset sets the configuration registers to their default values.

The 21143 supports byte, word, and longword accesses to configuration registers.

3.1.1 Configuration Register Mapping

Table 3–1 lists the definitions and addresses for the configuration registers.

Table 3–1 Configuration Registers Mapping

Configuration Register	Identifier	I/O Address Offset
Identification	CFID	00H
Command and status	CFCS	04H
Revision	CFRV	08H
Latency timer	CFLT	0CH
Base I/O address	CBIO	10H
Base memory address	CBMA	14H
Reserved	—	18H–24H
Card information structure	CCIS	28H
Subsystem ID	CSID	2CH
Expansion ROM base address	CBER	30H
Reserved	—	34H–38H
Interrupt	CFIT	3CH
Device and Driver area	CFDD	40H

3.1.2 Configuration Registers

The 21143 implements 11 configuration registers. These registers are described in the following subsections.

3.1.2.1 Configuration ID Register (CFID–Offset 00H)

The CFID register identifies the 21143. Figure 3–1 shows the CFID register bit fields and Table 3–2 describes the bit fields.

Figure 3–1 CFID Register Bit Fields

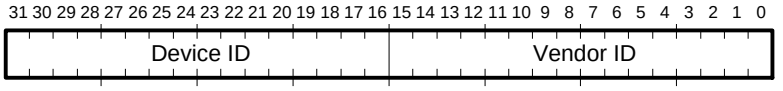

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Table 3–2 CFID Register Bit Fields Description

Field	Description
31:16	**Device ID**
	Provides the unique 21143 ID number (0019H).
15:0	**Vendor ID**
	Specifies the manufacturer of the 21143 (1011H).

Table 3–3 lists the access rules for the CFID register.

Table 3–3 CFID Register Access Rules

Category	Description
Value after hardware reset	00191011H
Read access rules	—
Write access rules	Writing has no effect.

3.1.2.2 Command and Status Configuration Register (CFCS–Offset 04H)

The CFCS register is divided into two sections: a command register (CFCS<15:0>) and a status register (CFCS<31:16>).

The command register provides control of the 21143's ability to generate and respond to PCI cycles. When 0 is written to this register, the 21143 logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for the PCI bus-related events. The CFCS status bits are not cleared when they are read. Writing 1 to these bits clears them; writing 0 has no effect.

Figure 3–2 shows the CFCS register bit fields.

Figure 3–2 CFCS Register Bit Fields

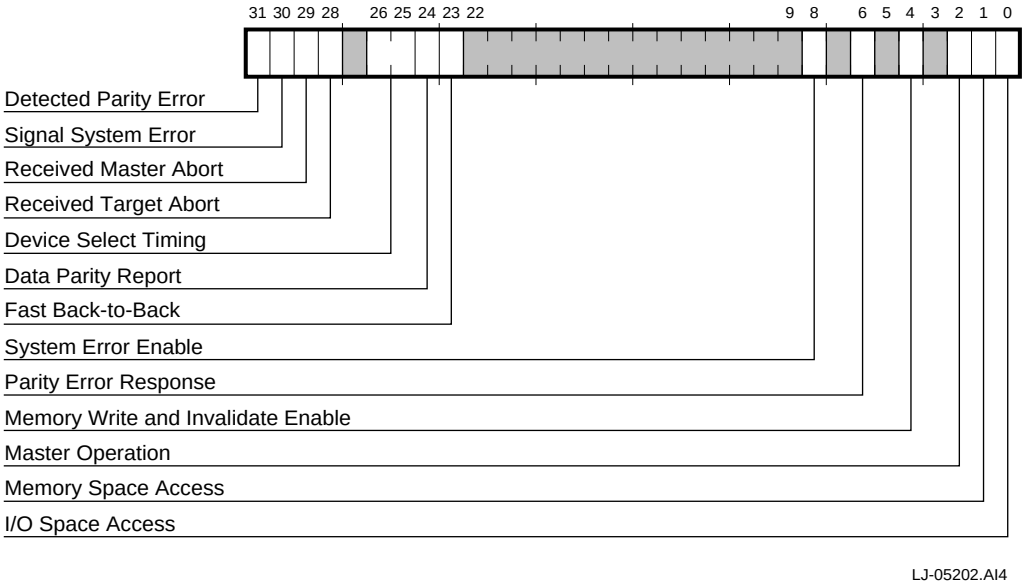

Table 3–4 describes the CFCS register bit fields.

Table 3–4 CFCS Register Bit Fields Description *(Sheet 1 of 2)*

Field	Bit Type	Description
31	**Status**	**Detected Parity Error** When set, indicates that the 21143 detected a parity error, even if parity error handling is disabled in parity error response (CFCS<6>).
30	**Status**	**Signal System Error** When set, indicates that the 21143 asserted the system error **serr_l** pin.
29	**Status**	**Received Master Abort** When set, indicates that the 21143 terminated a master transaction with master abort.
28	**Status**	**Received Target Abort** When set, indicates that the 21143 master transaction was terminated due to a target abort.
26:25	**Status**	**Device Select Timing** Indicates the timing of the assertion of device select (**devsel_l**). These bits are fixed at 01, which indicates a medium assertion of **devsel_l**.
24	**Status**	**Data Parity Report** This bit sets when the following conditions are met: • The 21143 asserts parity error **perr_l** or it senses the assertion of **perr_l** by another device. • The 21143 operates as a bus master for the operation that caused the error. • Parity error response (CFCS<6>) is set.
23	**Status**	**Fast Back-to-Back** Always set by the 21143. This indicates that the 21143 is capable of accepting fast back-to-back transactions that are not sent to the same bus device.
8	**Command**	**System Error Enable** When set, the 21143 asserts system error (**serr_l**) when it detects a parity error on the address phase (**ad<31:0>** and **c_be_l<3:0>**).

Table 3–4 CFCS Register Bit Fields Description *(Sheet 2 of 2)*

Field	Bit Type	Description
6	Command	**Parity Error Response** When set, the 21143 asserts fatal bus error (CSR5<13>) after it detects a parity error. When reset, any detected parity error is ignored and the 21143 continues normal operation. Parity checking is disabled after a hardware reset.
4	Command	**Memory Write and Invalidate Enable** When set, the 21143 is allowed to generate the memory write and invalidate command. When reset, the 21143 capability to generate the memory write and invalidate command is disabled.
2	Command	**Master Operation** When set, the 21143 is capable of acting as a bus master. When reset, the 21143 capability to generate PCI accesses is disabled. For normal 21143 operation, this bit must be set.
1	Command	**Memory Space Access** When set, the 21143 responds to memory space accesses. When reset, the 21143 does not respond to memory space accesses.
0	Command	**I/O Space Access** When set, the 21143 responds to I/O space accesses. When reset, the 21143 does not respond to I/O space accesses.

Table 3–5 lists the access rules for the CFCS register.

Table 3–5 CFCS Register Access Rules

Category	Description
Value after hardware reset	02800000H
Read access rules	—
Write access rules	—

3.1.2.3 Configuration Revision Register (CFRV–Offset 08H)

The CFRV register contains the 21143 revision number. Figure 3–3 shows the CFRV register bit fields and Table 3–6 describes the bit fields.

Figure 3–3 CFRV Register Bit Fields

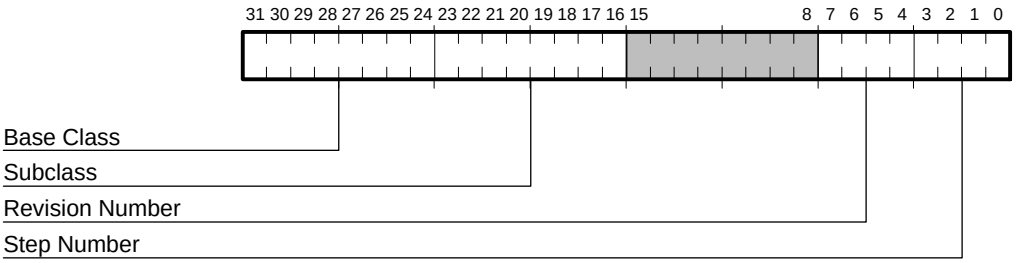

Table 3–6 CFRV Register Bit Fields Description

Field	Description
31:24	**Base Class**
	Indicates the network controller and is equal to 2H.
23:16	**Subclass**
	Indicates the fast Ethernet controller and is equal to 0H.
7:4	**Revision Number**
	Indicates the 21143 revision number and is equal to 2H. This number is incremented for subsequent 21143 revisions.
3:0	**Step Number**
	Indicates the 21143 step number and is equal to 1H (chip revision B). This number is incremented for subsequent 21143 steps within the current revision.

Table 3–7 lists the access rules for the CFRV register.

Table 3–7 CFRV Register Access Rules

Category	Description
Value after hardware reset	02000021H
Read access rules	—
Write access rules	Writing has no effect.

3.1.2.4 Configuration Latency Timer Register (CFLT–Offset 0CH)

This register configures the cache line size field and the 21143 latency timer. Figure 3–4 shows the CFLT bit field and Table 3–8 describes the CFLT bit field.

Figure 3–4 CFLT Configuration Latency Timer Register

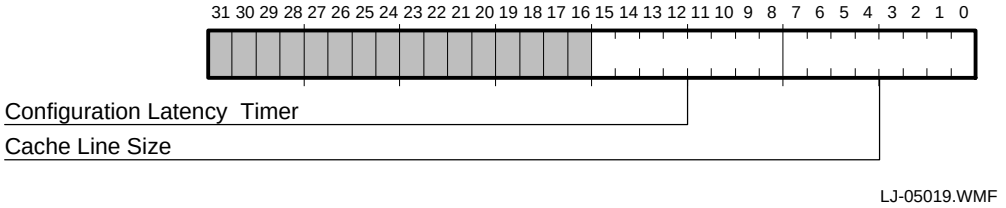

Table 3–8 CFLT Register Bit Fields Description

Field	Description
15:8	**Configuration Latency Timer** Specifies, in units of PCI bus clocks, the value of the latency timer of the 21143. When the 21143 asserts **frame_l**, it enables its latency timer to count. If the 21143 deasserts **frame_l** prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the 21143 initiates transaction termination as soon as its **gnt_l** is deasserted.
7:0	**Cache Line Size** Specifies, in units of 32-bit words, the system cache line size. The 21143 supports cache line sizes of 8, 16 and 32 longwords. If an attempt is made to write an unsupported value to this register, the 21143 behaves as if a value of zero was written. The driver should use the value of the cache line size to program the cache alignment bits (CSR0<15:14>). The 21143 uses the cache alignment bits for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple and memory-write-and-invalidate.

Table 3–9 lists the access rules for the CFLT register.

Table 3–9 CFLT Access Rules

Category	Description
Value after hardware reset	0H
Read access rules	—
Write access rules	—

3.1.2.5 Configuration Base I/O Address Register (CBIO–Offset 10H)

The CBIO register specifies the base I/O address for accessing the 21143 CSRs (CSR0–15). For example, if the CBIO register is programmed to 1000H, the I/O address of CSR15 is equal to CBIO + CSR15-offset for a value of 1078H (Table 3–24).

This register must be initialized prior to accessing any CSR with I/O access.

Figure 3–5 shows the CBIO register bit fields and Table 3–10 describes the bit fields.

Figure 3–5 CBIO Register Bit Fields

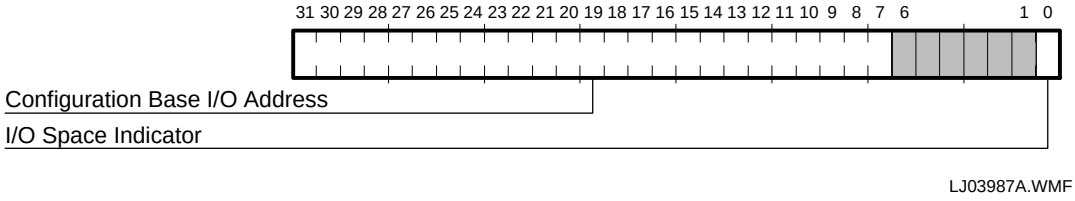

Table 3–10 CBIO Register Bit Fields Description

Field	Description
31:7	**Configuration Base I/O Address**
	Defines the base address assigned for mapping the 21143 CSRs.
6:1	**This field value is 0 when read**
0	**I/O Space Indicator**
	Determines that the register maps into the I/O space. The value in this field is 1. This is a read-only field.

Table 3–11 lists the access rules for the CBIO register.

Table 3–11 CBIO Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

3.1.2.6 Configuration Base Memory Address Register (CBMA–Offset 14H)

The CBMA register specifies the base memory address for memory accesses to the 21143 CSRs (CSR0–15).

This register must be initialized prior to accessing any CSR with memory access.

Figure 3–6 shows the CBMA register bit fields and Table 3–12 describes the bit fields.

Figure 3–6 CBMA Register Bit Fields

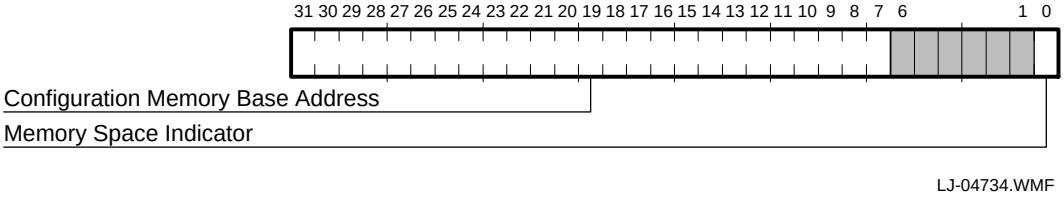

Table 3–12 CBMA Register Bit Fields Description

Field	Description
31:7	**Configuration Base Memory Address**
	Defines the base address assigned for mapping the 21143 CSRs.
6:1	**This field value is 0 when read.**
0	**Memory Space Indicator**
	Determines that the register maps into the memory space. The value in this field is 0. This is a read-only field.

Table 3–13 lists the access rules for the CBMA register.

Table 3–13 CBMA Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

3.1.2.7 Configuration Card Information Structure Register (CCIS–Offset 28H)

The CCIS register is a read-only 32-bit register. This register points to one of the possible address spaces where the card information structure (CIS) begins. The pointer is used in a CardBus PC card environment. The content of the CCIS is loaded from the serial ROM after a hardware reset. The loading period lasts 36,864 PCI cycles and starts 50 cycles after hardware reset deassertion. If the CCIS is accessed by the host before its content is loaded from the serial ROM, the 21143 responds with retry termination on the PCI bus. The value is 0 if the serial ROM data integrity check fails.

Figure 3–7 shows the CCIS register bit fields and Table 3–14 describes the bit fields.

Figure 3–7 CCIS Register Bit Fields

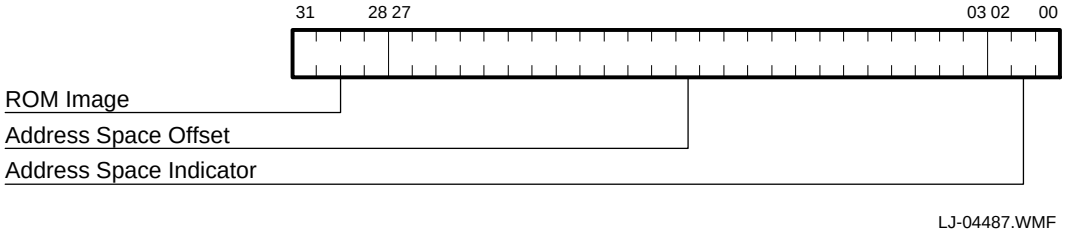

Table 3–14 CCIS Register Bit Fields Description

Field	Description
31:28	**ROM Image**
	The 4-bit ROM image field value when the CIS resides in an expansion ROM.
27:03	**Address Space Offset.**
	This field contains the address offset within the address space indicated by the address space indicator field (CCIS<2:0>).
2:0	**Address Space Indicator**
	This field indicates the location where the CIS address space begins. The 21143 supports only the value of 7 for this field, which means that the CIS begins in the expansion ROM space. Any other value in this field, causes the CCIS register to reset to 0.

Table 3–15 lists the access rules for the CCIS register.

Table 3–15 CCIS Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	Write has no effect on 21143.

3.1.2.8 Subsystem ID Register (CSID–Offset 2CH)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the serial ROM after a hardware reset. The loading period lasts 36,864 PCI cycles and starts 50 cycles after hardware reset deassertion. If the CSID is accessed by the host before its content is loaded from the serial ROM, the 21143 responds with retry termination on the PCI bus. The value is 0 if the serial ROM data integrity check fails.

Figure 3–8 shows the CSID register bit fields and Table 3–16 describes the bit fields.

Figure 3–8 CSID Register Bit Fields

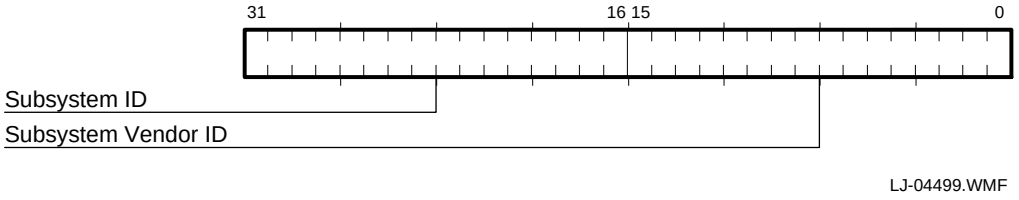

Table 3–16 CSID Register Bit Fields Description

Field	Description
31:16	**Subsystem ID**
	Indicates a 16-bit field containing the subsystem ID.
15:0	**Subsystem Vendor ID**
	Indicates a 16-bit field containing the subsystem vendor ID.

Table 3–17 lists the access rules for the CSID register.

Table 3–17 CSID Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	Write has no effect on 21143.

3.1.2.9 Expansion ROM Base Address Register (CBER–Offset 30H)

The CBER register specifies the base address and provides information about the expansion ROM size. This register must be initialized prior to accessing the expansion ROM.

Figure 3–9 shows the CBER register bit fields and Table 3–18 describes the bit fields.

Figure 3–9 CBER Register Bit Fields

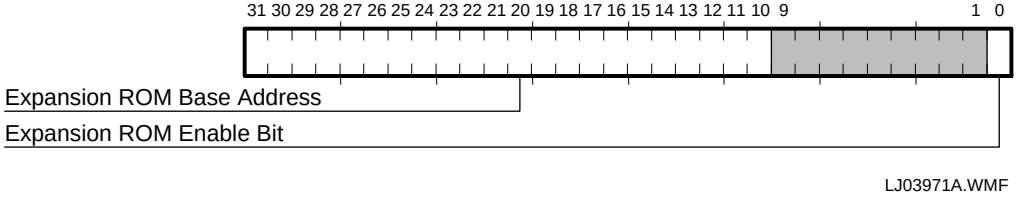

Table 3–18 CBER Register Bit Fields Description

Field	Description
31:10	**Expansion ROM Base Address**
	Defines the base address assigned for mapping the expansion ROM. It also provides information about the expansion ROM size. CBER<17:10> are hardwired to 0, indicating that the expansion ROM size is up to 256KB.
9:1	**This field value is 0 when read**
0	**Expansion ROM Enable Bit**
	The 21143 responds to its expansion ROM accesses only if the memory space access bit (CFCS<1>) and the expansion ROM enable bit are both set to 1.

Table 3–19 lists the access rules for the CBER register.

Table 3–19 CBER Register Access Rules

Category	Description
Value after hardware reset	XXXX0000H
Read access rules	—
Write access rules	—

3.1.2.10 Configuration Interrupt Register (CFIT–Offset 3CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin. CFIT configures both the system's interrupt line and the 21143 interrupt pin connection. Figure 3–10 shows the CFIT register bit fields.

Figure 3–10 CFIT Register Bit Fields

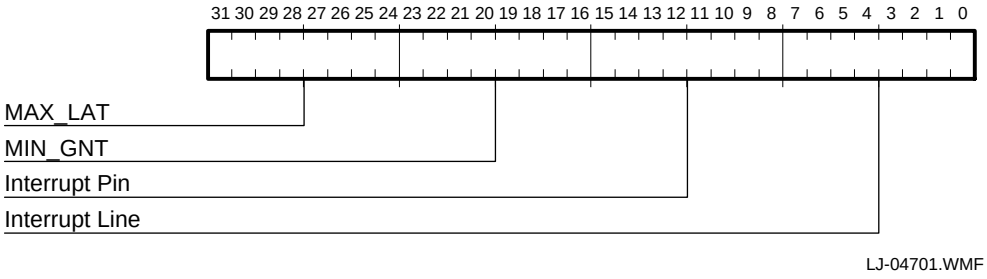

Table 3–20 describes the CFIT register bit fields.

Table 3–20 CFIT Register Bit Fields Description *(Sheet 1 of 2)*

Field	Description
31:24	**MAX_LAT** This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 28H (10 µs).
23:16	**MIN_GNT** This field indicates the burst period length that the device needs. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 14H (5 µs).

Table 3–20 CFIT Register Bit Fields Description *(Sheet 2 of 2)*

Field	Description
15:8	**Interrupt Pin**
	Indicates which interrupt pin the 21143 uses. The 21143 uses INTA# and the read value is 01H.
7:0	**Interrupt Line**
	Provides interrupt line routing information. The basic input/output system (BIOS) writes the routing information into this field when it initializes and configures the system.
	The value in this field indicates which input of the system interrupt controller is connected to the 21143's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.

Table 3–21 lists the access rules for the CFIT register.

Table 3–21 CFIT Register Access Rules

Category	Description
Value after hardware reset	281401XXH
Read access rules	—
Write access rules	—

3.1.2.11 Configuration Device and Driver Area Register (CFDD–Offset 40H)

The CFDD register can be used to store driver-specific information during initialization.

Figure 3–11 shows the CFDD register bit fields.

Figure 3–11 CFDD Register Bit Fields

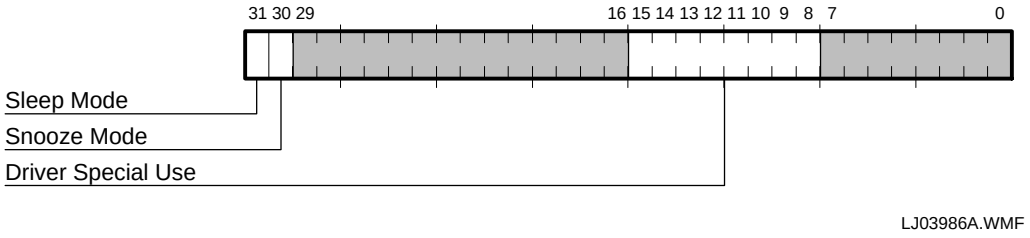

Table 3–22 describes the CFFD register bit.

Table 3–22 CFDD Register Bit Fields Description

Field	Description
31	**Sleep Mode**[1] When this bit is set, the 21143 enters sleep mode and most of its internal clocks are disconnected. While in sleep mode, the 21143 can only be accessed through its configuration space. The 21143 temporarily exits sleep mode upon hardware reset. When this bit is reset, a permanent exit from sleep mode is accomplished. Note that this bit should *not* be asserted together with bit 30 (snooze mode) in this register.
30	**Snooze Mode**[1] When this bit is set, the following conditions exist. The 21143 enters snooze mode and most of its clocks are disconnected. The 21143 temporarily exits snooze mode to normal operation mode upon sensing network activity, transmission start, or when it is being accessed by the host. When the activity is completed, the 21143 reenters snooze mode. When this bit is reset, the 21143 exits snooze mode. Note that this bit should *not* be asserted together with bit 31 (sleep mode) in this register.
15:8	**Driver Special Use** Specifies read and write fields for the driver's special use.

[1]There is no need to perform a software reset when changing from sleep mode or snooze mode to normal mode.

Table 3–23 lists the access rules for the CFDD register.

Table 3–23 CFDD Register Access Rules

Category	Description
Value after hardware reset	8000XX00H
Read access rules	—
Write access rules	—

3.2 CSR Operation

The 21143 CSRs are located in the host I/O or memory address space. The CSRs are *quadword* aligned, 32 bits long, and must be accessed using *longword* instructions with quadword-aligned addresses only.

Note: Reserved bits should be written with 0. Failing to do this could cause incompatibility problems with a future version of the 21143. Reserved bits are **UNPREDICTABL**E on read access.

Retries on second data transactions occur in response to burst accesses.

CSRs are physically located in the chip. The host uses a single instruction to access a CSR.

3.2.1 Control and Status Register Mapping

Table 3–24 lists the definitions and addresses for the CSR registers.

Table 3–24 CSR Mapping

Register	Meaning	Offset from CSR Base Address (CBIO and CBMA)
CSR0	Bus mode	00H
CSR1	Transmit poll demand	08H
CSR2	Receive poll demand	10H
CSR3	Receive list base address	18H
CSR4	Transmit list base address	20H
CSR5	Status	28H
CSR6	Operation mode	30H
CSR7	Interrupt enable	38H
CSR8	Missed frames and overflow counter	40H
CSR9	Boot ROM, serial ROM, and MII management	48H
CSR10	Boot ROM programming address	50H
CSR11	General-purpose timer	58H
CSR12	SIA status	60H
CSR13	SIA connectivity	68H
CSR14	SIA transmit and receive	70H
CSR15	SIA and general-purpose port	78H

3.2.2 Host CSRs

The 21143 implements 16 CSRs (CSR0 through CSR15), which can be accessed by the host.

3.2.2.1 Bus Mode Register (CSR0–Offset 00H)

CSR0 establishes the bus operating modes. Figure 3–12 shows the CSR0 bit fields.

Figure 3–12 CSR0 Bus Mode Register

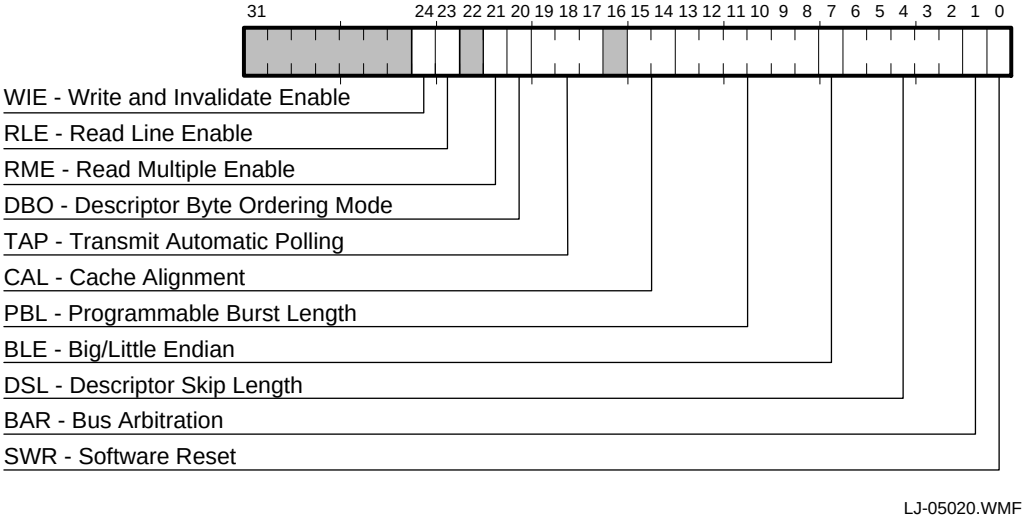

Table 3–25 describes the CSR0 bit fields.

Table 3–25 CSR0 Register Bit Fields Description *(Sheet 1 of 3)*

Field	Description
24	**WIE—Write and Invalidate Enable** When set, the 21143 supports the memory-write-and-invalidate command on the PCI bus. The 21143 uses the memory-write-and-invalidate command while writing full cache lines. While writing partial cache lines, the 21143 uses the memory-write command. Descriptors are also written using the memory-write command. When this field is reset, the memory-write command is used for write access. This bit is effective only if CFCS<4> is set.

Table 3–25 CSR0 Register Bit Fields Description *(Sheet 2 of 3)*

Field	Description
23	**RLE—Read Line Enable** When set, the 21143 supports the memory-read-line command on the PCI bus. Read access instructions that reach the cache-line boundary use the memory-read-line command. Read access instructions that do not reach the cache-line boundary use the memory-read command. This field operates in conjunction with the read multiple enable (CSR0<21>) field.
21	**RME—Read Multiple Enable** When set, the 21143 supports the memory-read-multiple command on the PCI bus. The 21143 uses the memory-read-multiple command while reading full cache lines. If the memory buffer is not cache aligned, the 21143 uses a memory-read command to read up to the cache line boundary. The 21143 then uses a memory-read-multiple command for reading an integer number of cache lines. If read line enable (CSR0<23>) is also set, the 21143 uses the memory-read-line command to align the memory buffer to the cache line. Read transactions that do not reach the cache line boundary use the memory-read command. The memory-read command is used to read descriptors.
20	**DBO—Descriptor Byte Ordering Mode** When set, the 21143 operates in big endian ordering mode for descriptors only. When reset, the 21143 operates in little endian mode.
19:17	**TAP—Transmit Automatic Polling** When set and the 21143 is in a suspended state because a transmit buffer is unavailable, the 21143 performs a transmit automatic poll demand (Table 3–26). This feature is not active in snooze mode.
15:14	**CAL—Cache Alignment** Programmable address boundaries for data burst stop (Table 3–28). If the buffer is not aligned, the 21143 executes the first transfer up to the address boundary. Then, all transfers are aligned to the specified boundary. When read line enable (CSR0<23>) is set, this field should be equal to the system cache line size (CFLT<7:0>). When write and invalidate enable (CSR0<24>) is set and read line enable (CSR0<23>) is reset, the cache alignment field should be equal to or a multiple of the system cache line size.

Table 3–25 CSR0 Register Bit Fields Description *(Sheet 3 of 3)*

Field	Description
13:8	**PBL—Programmable Burst Length** Indicates the maximum number of longwords to be transferred in one DMA transaction. If reset, the 21143 burst is limited only by the amount of data stored in the receive FIFO (at least 16 longwords), or by the amount of free space in the transmit FIFO (at least 16 longwords) before issuing a bus request. When read line enable (CSR0<23>) or write and invalidate enable (CSR0<24>) are set, the programmable burst length (CSR0<13:8>) should be greater than or equal to the system cache line size (CFLT<7:0>). The PBL can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the PBL default value is 0.
7	**BLE—Big/Little Endian** When set, the 21143 operates in big endian byte ordering mode. When reset, the 21143 operates in little endian byte ordering mode. Big endian is only applicable for data buffers. For example, the byte order in little endian of a data buffer is 12345678H, with each digit representing a nibble. In big endian, the byte orientation is 78563412H.
6:2	**DSL—Descriptor Skip Length** Specifies the number of longwords to skip between two unchained descriptors.
1	**BAR—Bus Arbitration** Selects the internal bus arbitration between the receive and transmit processes. When set, a round-robin arbitration scheme is applied resulting in equal sharing between processes. When reset, the receive process has priority over the transmit process, unless the 21143 is currently transmitting (Section 4.3.3).
0	**SWR—Software Reset** When set, the 21143 resets all internal hardware with the exception of the configuration area; it does not change the port select setting (CSR6<18>).

Table 3–26 defines the transmit automatic polling bits and lists the automatic polling intervals for MII 10/100-Mb/s and SRL modes.

Table 3–26 Transmit Automatic Polling Intervals

CSR0<19:17>	Polling Interval		
	10BASE-T/AUI	10-Mb/s MII/SYM	100-Mb/s MII/SYM
000	TAP Disabled	TAP Disabled	TAP Disabled
001	200 µs	800 µs	80 µs
010	800 µs	3.2 ms	320 µs
011	1.6 ms	6.4 ms	640 µs
100	12.8 µs	51.2 µs	5.12 µs
101	25.6 µs	102.4 µs	10.24 µs
110	51.2 µs	204.8 µs	20.48 µs
111	102.4 µs	409.6 µs	40.96 µs

Table 3–27 lists the CSR0 read and write access rules.

Table 3–27 CSR0 Access Rules

Category	Description
Value after reset	FE000000H
Read access rules	—
Write access rules	To write, the transmit and receive processes must be stopped. If one or both of the processes is not stopped, the result is **UNPREDICTABLE**.

Table 3–28 defines the cache address alignment bits.

Table 3–28 Cache Alignment Bits

CSR0<15:14>	Address Alignment
00	No cache alignment
01	8-longword boundary alignment
10	16-longword boundary alignment
11	32-longword boundary alignment

3.2.2.2 Transmit Poll Demand Register (CSR1–Offset 08H)

Figure 3–13 shows the CSR1 register bit field and Table 3–29 describes the bit field.

Figure 3–13 CSR1 Register Bit Field

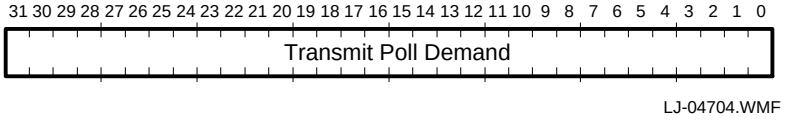

Table 3–29 CSR1 Register Bit Field Description

Field	Description
31:0	**TPD–Transmit Poll Demand (Write Only)**
	When written with any value, the 21143 checks for frames to be transmitted. If no descriptor is available, the transmit process returns to the suspended state and CSR5<2> is not asserted. If the descriptor is available, the transmit process resumes.

Table 3–30 lists the CSR1 read and write access rules.

Table 3–30 CSR1 Register Access Rules

Category	Description
Value after reset	FFFFFFFFH
Read access rules	—
Write access rules	Effective only if the transmit process is in the suspended state.

3.2.2.3 Receive Poll Demand Register (CSR2–Offset 10H)

Figure 3–14 shows the CSR2 bit field and Table 3–31 describes the bit field.

Figure 3–14 CSR2 Register Bit Field

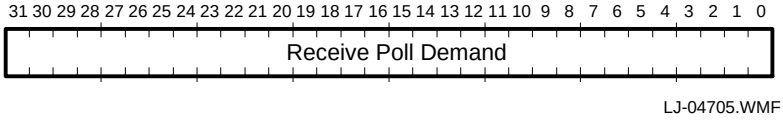

Table 3–31 CSR2 Register Bit Field Description

Field	Description
31:0	**RPD–Receive Poll Demand (Write Only)** When written with any value, the 21143 checks for receive descriptors to be acquired. If no descriptor is available, the receive process returns to the suspended state and CSR5<7> is not asserted. If the descriptor is available, the receive process resumes.

Table 3–32 lists the access rules for the CSR2 register.

Table 3–32 CSR2 Register Access Rules

Category	Description
Value after reset	FFFFFFFFH
Read access rules	—
Write access rules	Effective only if the receive process is in the suspended state.

3.2.2.4 Descriptor List Base Address Registers (CSR3–Offset 18H and CSR4–Offset 20H)

The CSR3 descriptor list base address register is used for receive buffer descriptors, and the CSR4 descriptor list base address register is used for transmit buffer descriptors. In both cases, the registers are used to point the 21143 to the start of the appropriate descriptor list.

Figure 3–15 shows the CSR3 register bit field and Table 3–33 describes the bit field.

Note: The descriptor lists reside in *physical* memory space and must be *longword* aligned. The 21143 behavior is **UNPREDICTABLE** when the lists are not longword aligned.

Writing to either CSR3 or CSR4 is permitted only when its respective process is in the stopped state. When stopped, the CSR3 and CSR4 registers must be written *before* the respective START command is given (Section 3.2.2.6).

Figure 3–15 CSR3 Register Bit Field

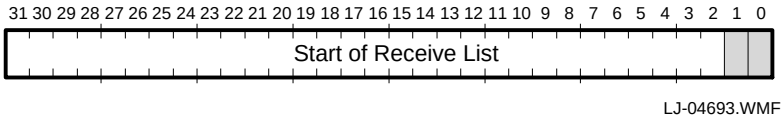

Table 3–33 CSR3 Register Bit Fields Description

Field	Description
31:2	**Start of Receive List**
1:0	**Must be 00 for longword alignment.**

Table 3–34 lists the access rules for the CSR3 register.

Table 3–34 CSR3 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	—
Write access rules	Receive process stopped

Figure 3–16 shows the CSR4 register bit field and Table 3–35 describes the bit field.

Figure 3–16 CSR4 Register Bit Field

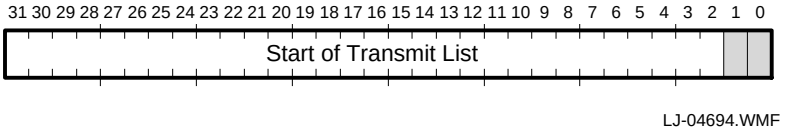

Table 3–35 CSR4 Register Bit Fields Description

Field	Description
31:2	**Start of Transmit List**
1:0	**Must be 00 for longword alignment.**

Table 3–36 lists the access rules for the CSR4 register.

Table 3–36 CSR4 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	—
Write access rules	Transmit process stopped

3.2.2.5 Status Register (CSR5–Offset 28H)

The status register (CSR5) contains all the status bits that the 21143 reports to the host. CSR5 is usually read by the driver during interrupt service routine or polling. Most of the fields in this register cause the host to be interrupted. CSR5 bits are not cleared when read. Writing 1 to these bits clears them; writing 0 has no effect. Each field can be masked (Section 3.2.2.7).

Figure 3–17 shows the CSR5 register bit fields.

Figure 3–17 CSR5 Register Bit Fields

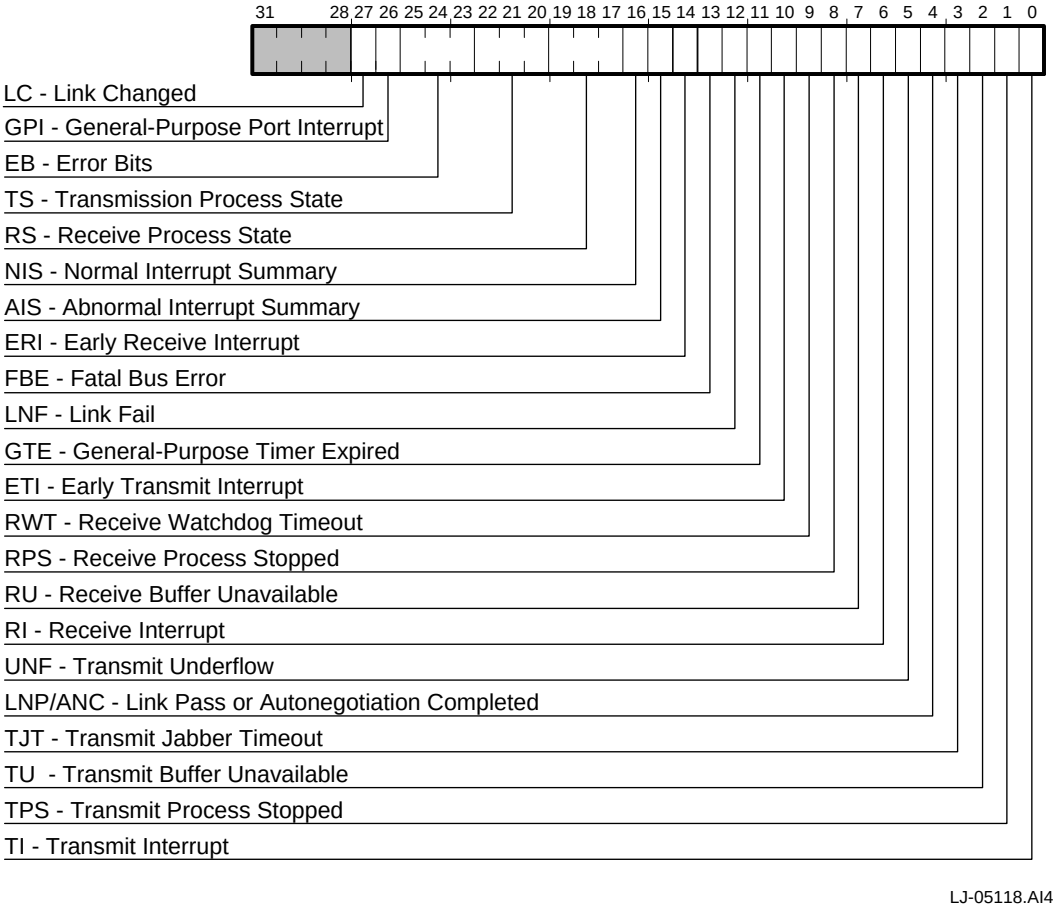

Table 3–37 describes the CSR5 register bit fields.

Table 3–37 CSR5 Register Bit Fields Description *(Sheet 1 of 4)*

Field	Description
27	**LC—Link Changed** Indicates that the 100BASE-T link status has changed from link pass to link fail or from link fail to link pass. The new status can be read from CSR12<1>, 100BASE-T link status.
26	**GPI—General-Purpose Port Interrupt** Indicates an interrupt from the general-purpose port (CSR15<30:28>; Table 3–65 provides a description of these bits).
25:23	**EB—Error Bits (Read Only)** Indicates the type of error that caused bus error. Valid only when fatal bus error CSR5<13> is set (Table 3–38). This field does not generate an interrupt.
22:20	**TS—Transmission Process State (Read Only)** Indicates the state of the transmit process (Table 3–39). This field does not generate an interrupt.
19:17	**RS—Receive Process State (Read Only)** Indicates the state of the receive process (Table 3–40). This field does not generate an interrupt.
16	**NIS—Normal Interrupt Summary** Normal interrupt summary bit. Its value is the logical OR of: CSR5<0>—Transmit interrupt CSR5<2>—Transmit buffer unavailable CSR5<6>—Receive interrupt CSR5<11>—General-purpose timer expired CSR5<14>—Early receive interrupt Only unmasked bits affect the normal interrupt summary CSR5<16> bit.

Table 3–37 CSR5 Register Bit Fields Description *(Sheet 2 of 4)*

Field	Description
15	**AIS—Abnormal Interrupt Summary** Abnormal interrupt summary bits. Its value is the logical OR of: CSR5<1>—Transmit process stopped CSR5<3>—Transmit jabber timeout CSR5<4>—Link pass or autonegotiation completed CSR5<5>—Transmit underflow CSR5<7>—Receive buffer unavailable CSR5<8>—Receive process stopped CSR5<9>—Receive watchdog timeout CSR5<10>—Early transmit interrupt CSR5<12>—Link fail CSR5<13>—Fatal bus error CSR5<26>—General-purpose port interrupt CSR5<27>—Link changed Only unmasked bits affect the abnormal interrupt summary CSR5<15> bit.
14	**ERI—Early Receive Interrupt** Indicates that the 21143 has filled the first data buffer of the packet. Receive interrupt (CSR5<6>) automatically clears this bit.
13	**FBE—Fatal Bus Error** Indicates that a bus error occurred (Table 3–38). When this bit is set, the 21143 disables all of its bus access operations.
12	**LNF—Link Fail** Indicates a transition to the link fail state in the twisted-pair port. See link fail status CSR12<2>. This bit is valid only when CSR6<18>, Port Select, is reset; CSR14<8>, Receive Squelch Enable, is set; and CSR13<3>, 10BASE-T or AUI, is 0 (10BASE-T mode). This bit is also set as a result of setting CSR15<10>, Force Link Fail. Link pass CSR5<4> automatically clears this bit.
11	**GTE—General-Purpose Timer Expired** Indicates that the general-purpose timer (CSR11) counter has expired. This timer is mainly used by the software driver.
10	**ETI—Early Transmit Interrupt** Indicates that the packet to be transmitted was fully transferred into the chip's internal transmit FIFOs. Transmit interrupt (CSR5<0>) automatically clears this bit.

Table 3–37 CSR5 Register Bit Fields Description *(Sheet 3 of 4)*

Field	Description
9	**RWT—Receive Watchdog Timeout** This bit reflects the line status and indicates that the receive watchdog timer has expired while another node is still active on the network. In case of overflow, the long packets may not be received.
8	**RPS—Receive Process Stopped** Asserts when the receive process enters the stopped state.
7	**RU—Receive Buffer Unavailable** Indicates that the next descriptor in the receive list is owned by the host and cannot be acquired by the 21143. The reception process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive poll demand command. If no receive poll demand is issued, the reception process resumes when the next recognized incoming frame is received. After the first assertion, CSR5<7> is not asserted for any subsequent not owned receive descriptors fetches. CSR5<7> asserts only when the previous receive descriptor was owned by the 21143.
6	**RI—Receive Interrupt** Indicates the completion of a frame reception. Specific frame status information has been posted in the descriptor. The reception process remains in the running state.
5	**UNF—Transmit Underflow** Indicates that the transmit FIFO had an underflow condition during the packet transmission. The transmit process is placed in the suspended state and underflow error TDES0<1> is set.
4	**LNP/ANC—Link Pass or Autonegotiation Completed** When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10BASE-T Link Integrity Test has completed successfully, after the link was down. This bit is also set as a result of writing 0 to CSR14<12>, Link Test Enable. When autonegotiation is enabled (CSR14<7>=1), this bit indicates that the autonegotiation has completed (CSR12<14:12>=5H). CSR12 should then be read for a link status report. This bit is valid only when port select (CSR6<18>) is reset, and receive squelch enable (CSR14<8>) is set. Link fail interrupt (CSR5<12>) automatically clears this bit.
3	**TJT—Transmit Jabber Timeout** Indicates that the transmit jabber timer expired, meaning that the 21143 transmitter had been excessively active. The transmission process is *aborted* and placed in the stopped state. This event causes the transmit jabber timeout TDES0<14> flag to assert.

Table 3–37 CSR5 Register Bit Fields Description *(Sheet 4 of 4)*

Field	Description
2	**TU—Transmit Buffer Unavailable** Indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the 21143. The transmission process is suspended. Table 4–14 explains the transmit process state transitions. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit poll demand command, unless transmit automatic polling (Table 3–26) is enabled.
1	**TPS—Transmit Process Stopped** Asserts when the transmit process enters the stopped state.
0	**TI—Transmit Interrupt** Indicates that a frame transmission was completed and TDES1<31> is asserted in the first descriptor of the frame.

Table 3–38 lists the bit codes for the fatal bus error bits.

Table 3–38 Fatal Bus Error Bits

CSR5<25:23>	Error Type
000	Parity error[1]
001	Master abort
010	Target abort
011	Reserved
1xx	Reserved

[1]The only way to recover from a parity error is by setting software reset (CSR0<0>=1).

Table 3–39 lists the bit codes for the transmit process state.

Table 3–39 Transmit Process State

CSR5<22:20>	Process State
000	Stopped—RESET command or transmit jabber expired
001	Running—Fetching transmit descriptor
010	Running—Waiting for end of transmission
011	Running—Reading buffer from memory and queuing the data into the transmit FIFO
100	Reserved
101	Running—Setup packet
110	Suspended—Transmit FIFO underflow, or an unavailable transmit descriptor
111	Running—Closing transmit descriptor

Table 3–40 lists the bit codes for the receive process state.

Table 3–40 Receive Process State

CSR5<19:17>	Process State
000	Stopped—RESET or STOP RECEIVE command
001	Running—Fetching receive descriptor
010	Running—Checking for end of receive packet before prefetch of next descriptor
011	Running—Waiting for receive packet
100	Suspended—Unavailable receive buffer
101	Running—Closing receive descriptor
110	Running—Flushing the current frame from the receive FIFO because of unavailable receive buffer
111	Running—Queuing the receive frame from the receive FIFO into the receive buffer

Table 3–41 lists the access rules for the CSR5 register.

Table 3–41 CSR5 Register Access Rules

Category	Description
Value after reset	F0000000H
Read access rules	—
Write access rules	CSR5 bits 0 through 16, bit 26, and bit 27 are cleared by writing 1. Writing 0 to these bits has no effect. Writing to CSR5 bits 17 through 25 has no effect.

3.2.2.6 Operation Mode Register (CSR6–Offset 30H)

The operation mode register (CSR6) establishes the receive and transmit operating modes and commands. CSR6 should be the last CSR to be written as part of initialization. Figure 3–18 shows the CSR6 register bit fields.

Figure 3–18 CSR6 Register Bit Fields

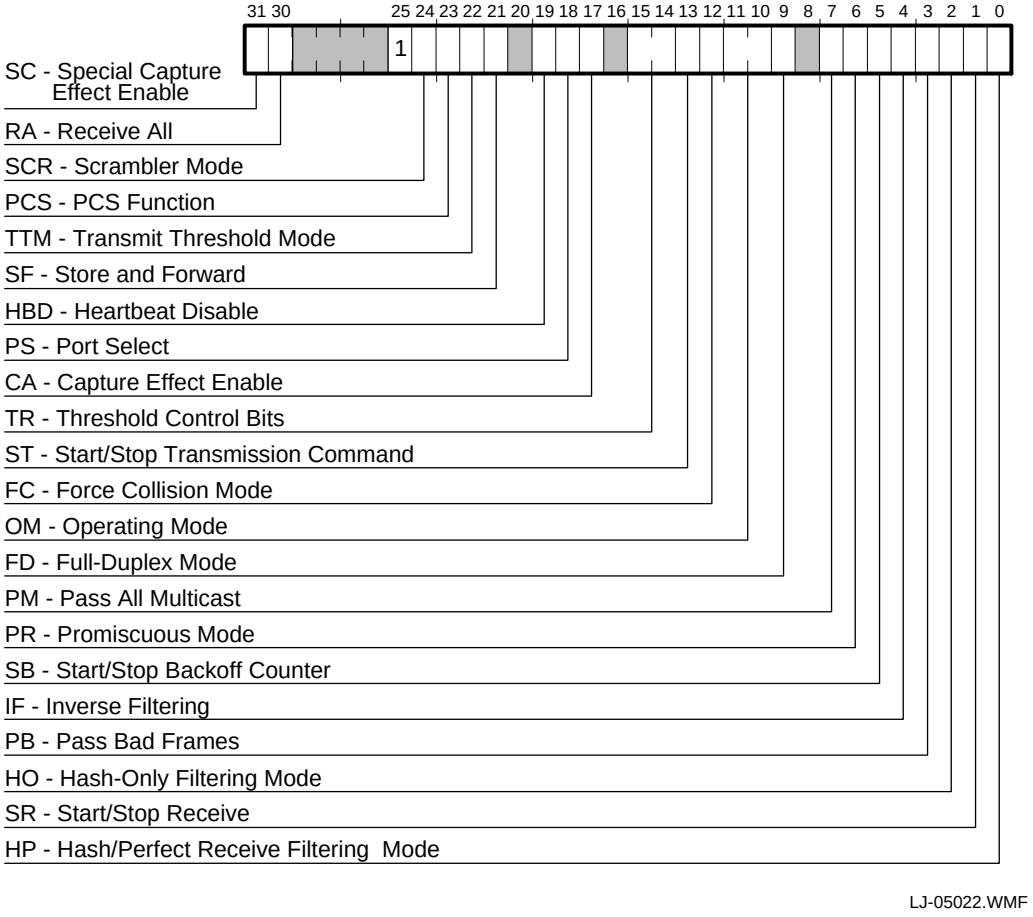

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Table 3–42 describes the CSR6 register bit fields.

Table 3–42 CSR6 Register Bit Fields Description *(Sheet 1 of 4)*

Field	Description
31	**SC—Special Capture Effect Enable** When set, enables the enhanced resolution of capture effect on the network (Table 6–7). Digital recommends that this bit be set together with CSR6<17>. When clear, the 21143 disables the enhanced resolution of capture effect on the network.
30	**RA—Receive All** When set, all incoming packets will be received, regardless of the destination address. The address match is checked according to Table 3–46, and is reported in RDES0<30>.
25	**MBO—Must Be One** This bit should always be programmed to one.
24	**SCR—Scrambler Mode** When set, the scrambler function is active and the MII/SYM port transmits and receives scrambled signals. Changing this bit during operation may cause **UNPREDICTABLE** behavior.
23	**PCS—PCS Function** When set, the PCS functions are active and the MII/SYM port operates in symbol mode. All MII/SYM port control signals are generated internally. When reset, the PCS functions are not active, and the MII/SYM port operates in MII mode. Changing this bit during operation may cause **UNPREDICTABLE** behavior.
22	**TTM—Transmit Threshold Mode** Selects the transmit FIFO threshold to be either 10 Mb/s or 100 Mb/s (Table 3–43). When set, the threshold is 10 Mb/s. When reset, the threshold is 100 Mb/s. The transmit process must be in the stopped state to change this bit.
21	**SF—Store and Forward** When set, transmission starts when a full packet resides in the FIFO. When this occurs, the threshold values specified in CSR6<15:14> are ignored. The transmit process must be in the stopped state to change this bit.
19	**HBD—Heartbeat Disable** When set, the heartbeat signal quality (SQE) generator function is disabled. This bit should be set in the MII/SYM 100-Mb/s mode. In the MII 10-Mb/s mode this bit should be set according to the PHY device configuration.

Table 3–42 CSR6 Register Bit Fields Description *(Sheet 2 of 4)*

Field	Description
18	**PS—Port Select**
	When reset, the 10BASE-T or AUI port is selected according to the CSR13<3> value. When set, the MII/SYM port is selected (Table 3–44).
	During a hardware reset, this bit automatically resets.
	A software reset does not affect this bit.
17	**CA—Capture Effect Enable**
	When set, enables the 21143 feature that solves the capture effect problem on the network (Section 6.7).
	When reset, this 21143 feature is disabled.
15:14	**TR—Threshold Control Bits**
	Controls the selected threshold level for the 21143 transmit FIFO. Four threshold levels are allowed (Table 3–43).
	The threshold value has a direct impact on the 21143 bus arbitration scheme (Section 4.3.3).
	Transmission starts when the frame size within the transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted.
	The transmit process must be in the stopped state to change these bits (CSR6<15:14).
13	**ST—Start/Stop Transmission Command**
	When set, the transmission process is placed in the running state, and the 21143 checks the transmit list at the *current* position for a frame to be transmitted.
	Descriptor acquisition is attempted either from the *current* position in the list, which is the transmit list base address set by *CSR4*, or from the position retained when the transmit process was previously stopped.
	If the current descriptor is not owned by the 21143, the transmission process enters the suspended state and transmit buffer unavailable (CSR5<2>) is set. The start transmission command is effective only when the transmission process is stopped. If the command is issued before setting CSR4, the 21143 behavior will be **UNPREDICTABLE**.
	When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The next descriptor position in the transmit list is saved, and becomes the current position when transmission is restarted.
	The stop transmission command is effective only when the transmission process is in either the running or suspended state (Table 4–14).
12	**FC—Force Collision Mode**
	Allows the collision logic to be tested. Meaningful only in internal loopback mode. When set, a collision is forced during the next transmission attempt. This results in 16 transmission attempts with excessive collision reported in the transmit descriptor (TDES0<8>).

Table 3–42 CSR6 Register Bit Fields Description *(Sheet 3 of 4)*

Field	Description
11:10	**OM—Operating Mode** Selects the 21143 loopback operation modes (Table 3–45).
9	**FD—Full-Duplex Mode** When autonegotiation is disabled (CSR14<7> = 0), this bit selects the 21143 half-duplex or full-duplex operation mode. A 0 selects half-duplex operation while a 1 selects full-duplex operation. When autonegotiation is enabled (CSR14<7> = 1) and the 21143 is operating in 10BASE-T mode (CSR6<18> = 0 and CSR13<3> = 0), this bit controls the advertisement of 10BASE-T full-duplex capability (bit 6) in the transmitted code word. The 21143 will operate in 10BASE-T full-duplex mode *only* if both link partners are advertising this bit set. This bit has no meaning in AUI mode (CSR6<18> = 0 and CSR13<3> = 1). Changing the full-duplex bit is permitted only if the transmit and receive processes are in the stopped state. While in full-duplex mode, heartbeat check is disabled, heartbeat fail (TDES0<7>) should be ignored, and internal loopback is not allowed.
7	**PM—Pass All Multicast** When set, indicates that all the incoming frames with a multicast destination address (first bit in the destination address field is 1) are received. Incoming frames with physical address destinations are filtered according to the CSR6<0> bit.
6	**PR—Promiscuous Mode** When set, indicates that any incoming valid frame is received, regardless of its destination address.
5	**SB—Start/Stop Backoff Counter** When set, indicates that the internal backoff counter stops counting when any carrier activity is detected. The 21143 backoff counter resumes when the carrier drops. The earliest the 21143 starts its transmission after carrier deassertion is 9.6 µs for 10-Mb/s data rate or 0.96 µs for 100-Mb/s data rate. When reset, the internal backoff counter is not affected by the carrier activity.
4	**IF—Inverse Filtering (Read Only)** When set, the 21143 operates in an inverse filtering mode. This is valid only during perfect filtering mode (Table 3–46 and Table 4–8).

Table 3–42 CSR6 Register Bit Fields Description *(Sheet 4 of 4)*

Field	Description
3	**PB—Pass Bad Frames** When set, the 21143 operates in pass bad frame mode. All incoming frames that passed the address filtering are received, including runt frames, collided fragments, or truncated frames caused by FIFO overflow. If any received bad frames are required, promiscuous mode (CSR6<6>) should be set to 1.
2	**HO—Hash-Only Filtering Mode (Read Only)** When set, the 21143 operates in an imperfect address filtering mode for both physical and multicast addresses (Table 4–8).
1	**SR—Start/Stop Receive** When set, the receive process is placed in the running state. The 21143 attempts to acquire a descriptor from the receive list and processes incoming frames. Descriptor acquisition is attempted from the *current* position in the list, which is the address set by *CSR3* or the position retained when the receive process was previously stopped. If no descriptor is owned by the 21143, the receive process enters the suspended state and receive buffer unavailable (CSR5<7>) sets. The start reception command is effective only when the reception process has stopped. If the command was issued before setting CSR3, the 21143 behavior is **UNPREDICTABLE**. When cleared, the receive process enters the stopped state after completing the reception of the current frame. The next descriptor position in the receive list is saved, and becomes the *current* position after the receive process is restarted. The stop reception command is effective only when the receive process is in running or suspended state (Table 4–13).
0	**HP—Hash/Perfect Receive Filtering Mode (Read Only)** When reset, the 21143 does a perfect address filter of incoming frames according to the addresses specified in the setup frame (Table 4–8). When set, the 21143 does imperfect address filtering of multicast incoming frames according to the hash table specified in the setup frame. If CSR6<2> is set, then physical addresses are imperfect address filtered too. If CSR6<2> is reset, physical addresses are perfect address filtered, according to a single physical address, as specified in the setup frame.

Table 3–43 lists the threshold values in bytes.

Table 3–43 Transmit Threshold

CSR6<21>	CSR6<15:14>	CSR6<18> = 0 CSR6<22> = X	CSR6<18> = 1 CSR6<22> = 1	CSR6<18> = 1 CSR6<22> = 0
0	00	72	72	128
0	01	96	96	256
0	10	128	128	512
0	11	160	160	1024
1	XX	Store and forward	Store and forward	Store and forward

Table 3–44 lists the port and data rate selection.

Table 3–44 Port and Data Rate Selection

CSR6 <18>	CSR6 <22>	CSR6 <23>	CSR6 <24>	Active Port	Data Rate	Function
0	0	X	X	10BASE-T/ AUI	10 Mb/s	10BASE-T or AUI interface
1	1	0	0	MII/SYM	10 Mb/s	MII with transmit FIFO thresholds appropriate for 10 Mb/s
1	0	0	0	MII/SYM	100 Mb/s	MII with transmit FIFO thresholds appropriate for 100 Mb/s
1	0	1	0	MII/SYM	100 Mb/s	PCS function for 100BASE-FX
1	0	1	1	MII/SYM	100 Mb/s	PCS and scrambler functions for 100BASE-TX

Table 3–45 selects the 21143 loopback operation modes.

Table 3–45 Loopback Operation Mode

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback[1]
10	External loopback

[1]The selected port is placed in the internal loopback mode of operation. The PCS functions (CSR6<23>) and the scrambler function (CSR6<24>) are also tested. When the SYM port is in internal loopback mode, symbols appear on the network. When the MII port is in internal loopback mode, the signal **mii_txen** is disabled.

Table 3–46 lists the codes to determine the filtering mode.

Table 3–46 Filtering Mode

CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering
0	0	0	1	1	512-bit hash for multicast and physical addresses
0	0	1	0	0	Inverse filtering
X	1	0	0	X	Promiscuous
0	1	0	1	1	Promiscuous
1	0	0	0	X	Pass all multicast
1	0	0	1	1	Pass all multicast

Note: When CSR6<30> is set (receive all mode), this table is used to generate the address match status reported in RDES0<30>.

Table 3–47 describes the only conditions that permit change to a field when modifying values to the CSR6 register.

Table 3–47 CSR6 Register Access Rules

Category	Description
Value after reset	32000040H
Read access rules	—
Write access rules	
* CSR6<22>	Receive and transmit processes stopped
* CSR6<21>	Receive and transmit processes stopped
* CSR6<17>	Receive and transmit processes stopped
* CSR6<16>	Receive and transmit processes stopped
* CSR6<15:14>	Transmit process stopped
* CSR6<12>	Receive and transmit processes stopped
* CSR6<11:10>	Receive and transmit processes stopped
* CSR6<9>	Receive and transmit processes stopped
* CSR6<8>	Transmit process stopped
* CSR6<5>	Receive and transmit processes stopped
* CSR6<3>	Receive process stopped
* Start_Transmit CSR6<13>=1	CSR4 initialized
* Stop_Transmit CSR6<13>=0	Transmit running or suspended
* Start_Receive CSR6<1>=1	CSR3 initialized
* Stop_Receive CSR6<1>=0	Receive running or suspended

3.2.2.7 Interrupt Enable Register (CSR7–Offset 38H)

The interrupt enable register (CSR7) enables the interrupts reported by CSR5 (Section 3.2.2.5). Setting a bit to 1 enables a corresponding interrupt. After a hardware or software reset, all interrupts are disabled. Figure 3–19 shows the CSR7 register bit fields.

Figure 3–19 CSR7 Register Bit Fields

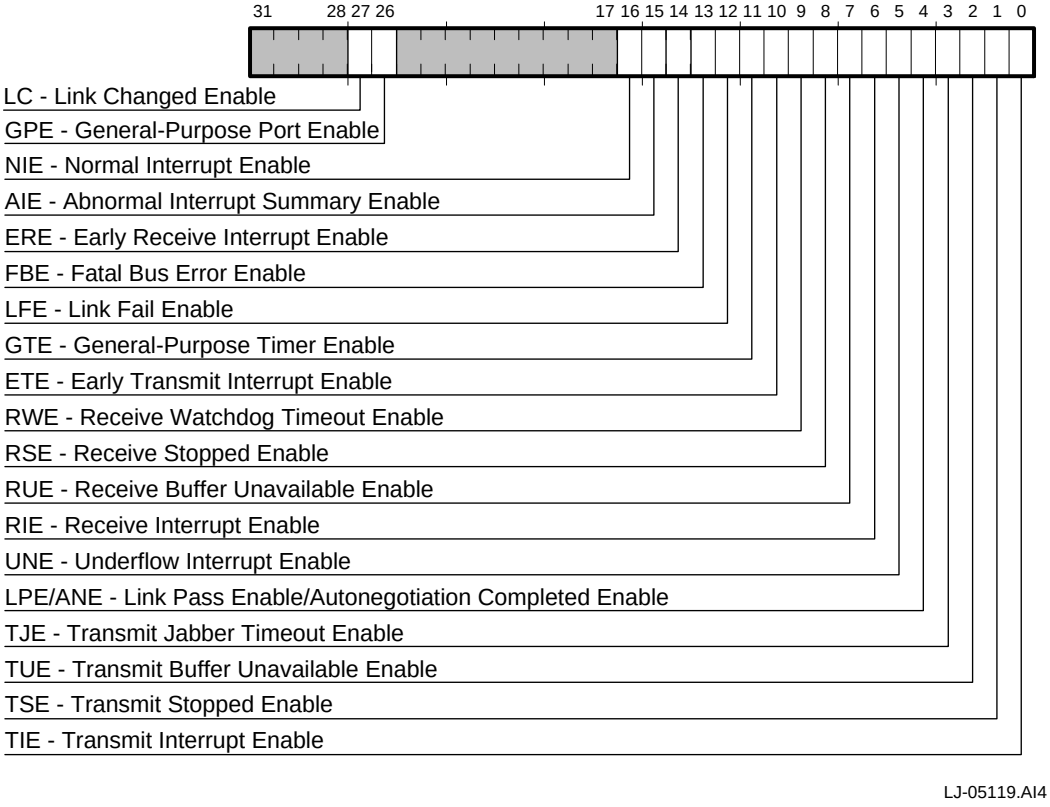

Table 3–48 describes the CSR7 register bit fields.

Table 3–48 CSR7 Register Bit Fields Description *(Sheet 1 of 4)*

Field	Description
27	**LCE—Link Changed Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link changed interrupt (CSR5<27>) is enabled. When this bit is reset, the link changed interrupt (CSR5<27>) is disabled.
26	**GPE—General-Purpose Port Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the general-purpose port interrupt (CSR5<26>) is enabled. When this bit is reset, the general-purpose port interrupt (CSR5<26>) is disabled.
16	**NIE—Normal Interrupt Summary Enable** When set, normal interrupt is enabled. When reset, no normal interrupt is enabled. This bit (CSR7<16>) enables the following bits: CSR5<0>—Transmit interrupt CSR5<2>—Transmit buffer unavailable CSR5<6>—Receive interrupt CSR5<11>—General-purpose timer expired CSR5<14>—Early receive interrupt
15	**AIE—Abnormal Interrupt Summary Enable** When set, abnormal interrupt is enabled. When reset, no abnormal interrupt is enabled. This bit (CSR7<15>) enables the following bits: CSR5<1>—Transmit process stopped CSR5<3>—Transmit jabber timeout CSR5<4>—Link pass or autonegotiation completed CSR5<5>—Transmit underflow CSR5<7>—Receive buffer unavailable CSR5<8>—Receive process stopped CSR5<9>—Receive watchdog timeout CSR5<10>—Early transmit interrupt CSR5<12>—Link fail CSR5<26>—General-purpose port interrupt CSR5<27>—Link changed

Table 3–48 CSR7 Register Bit Fields Description *(Sheet 2 of 4)*

Field	Description
14	**ERE—Early Receive Interrupt Enable** When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the early receive interrupt (CSR5<14>) is enabled. When this bit is reset, the early receive interrupt (CSR5<14>) is disabled.
13	**FBE—Fatal Bus Error Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the fatal bus error interrupt (CSR5<13>) is enabled. When this bit is reset, the fatal bus error interrupt (CSR5<13>) is disabled.
12	**LFE—Link Fail Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link fail interrupt (CSR5<12>) is enabled. When this bit is reset, the link fail interrupt (CSR5<12>) is disabled.
11	**GTE—General-Purpose Timer Enable** When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the general-purpose timer expired interrupt (CSR5<11>) is enabled. When this bit is reset, the general-purpose timer expired interrupt (CSR5<11>) is disabled.
10	**ETE—Early Transmit Interrupt Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the early transmit interrupt (CSR5<10>) is enabled. When this bit is reset, the early transmit interrupt (CSR5<10>) is disabled.
9	**RWE—Receive Watchdog Timeout Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive watchdog timeout interrupt (CSR5<9>) is enabled. When this bit is reset, the receive watchdog timeout interrupt (CSR5<9>) is disabled.
8	**RSE—Receive Stopped Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive stopped interrupt (CSR5<8>) is enabled. When this bit is reset, the receive stopped interrupt (CSR5<8>) is disabled.

Table 3–48 CSR7 Register Bit Fields Description *(Sheet 3 of 4)*

Field	Description
7	**RUE—Receive Buffer Unavailable Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive buffer unavailable interrupt (CSR5<7>) is enabled. When this bit is reset, the receive buffer unavailable interrupt (CSR5<7>) is disabled.
6	**RIE—Receive Interrupt Enable** When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the receive interrupt (CSR5<6>) is enabled. When this bit is reset, the receive interrupt (CSR5<6>) is disabled.
5	**UNE—Underflow Interrupt Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit underflow interrupt (CSR5<5>) is enabled. When this bit is reset, the transmit underflow bit (CSR5<5>) is disabled.
4	**LPE/ANE—Link Pass Enable/Autonegotiation Completed Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link pass/autonegotiation completed interrupt (CSR5<4>) is enabled. When this bit is reset, the link pass/autonegotiation completed bit (CSR5<4>) is disabled.
3	**TJE—Transmit Jabber Timeout Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit jabber timeout interrupt (CSR5<3>) is enabled. When this bit is reset, the transmit jabber timeout interrupt (CSR5<3>) is disabled.
2	**TUE—Transmit Buffer Unavailable Enable** When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the transmit buffer unavailable interrupt (CSR5<2>) is enabled. When this bit is reset, the transmit buffer unavailable interrupt (CSR5<2>) is disabled.

Table 3–48 CSR7 Register Bit Fields Description *(Sheet 4 of 4)*

Field	Description
1	**TSE—Transmit Stopped Enable** When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit process stopped interrupt (CSR5<1>) is enabled. When this bit is reset, the transmit process stopped interrupt (CSR5<1>) is disabled.
0	**TIE—Transmit Interrupt Enable** When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the transmit interrupt (CSR5<0>) is enabled. When this bit is reset, the transmit interrupt (CSR5<0>) is disabled.

Table 3–49 lists the access rules for the CSR7 register.

Table 3–49 CSR7 Register Access Rules

Category	Description
Value after reset	F3FE0000H
Read access rules	—
Write access rules	—

3.2.2.8 Missed Frames and Overflow Counter Register (CSR8–Offset 40H)

Figure 3–20 shows the CSR8 bit fields and Table 3–50 describes the bit fields.

Figure 3–20 CSR8 Missed Frames and Overflow Counter

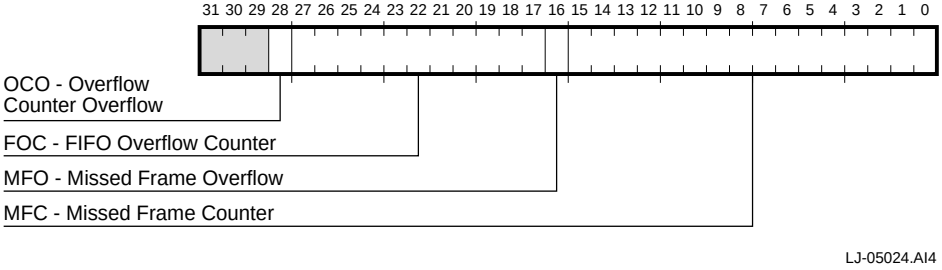

Table 3–50 CSR8 Register Bit Fields Description

Field	Description
28	**OCO—Overflow Counter Overflow (Read Only)**
	Sets when the FIFO overflow counter overflows; resets when CSR8 is read.
27:17	**FOC—FIFO Overflow Counter (Read Only)**
	Indicates the number of received frames discarded because of receive FIFO overflow. The counter clears when read.
16	**MFO—Missed Frame Overflow (Read Only)**
	Sets when the missed frame counter overflows; resets when CSR8 is read.
15:0	**MFC—Missed Frame Counter (Read Only)**
	Indicates the number of frames discarded because no host receive descriptors were available (CSR5<7>, RU – Receive Buffer Unavailable). The counter clears when read.

Table 3–51 lists the access rules for the CSR8 register.

Table 3–51 CSR8 Register Access Rules

Category	Description
Value after reset	E0000000H
Read access rules	—
Write access rules	Not possible

3.2.2.9 Boot ROM, Serial ROM, and MII Management Register (CSR9–Offset 48H)

The boot ROM, serial ROM, and MII management register (CSR9) provides an interface to the boot ROM, serial ROM, and MII management. It selects the device and contains both the commands and data to be read from and stored in the boot ROM and serial ROM. The MII management selects an operation mode for reading and writing the MII.

Figure 3–21 shows the CSR9 register bit fields.

Figure 3–21 CSR9 Register Bit Fields

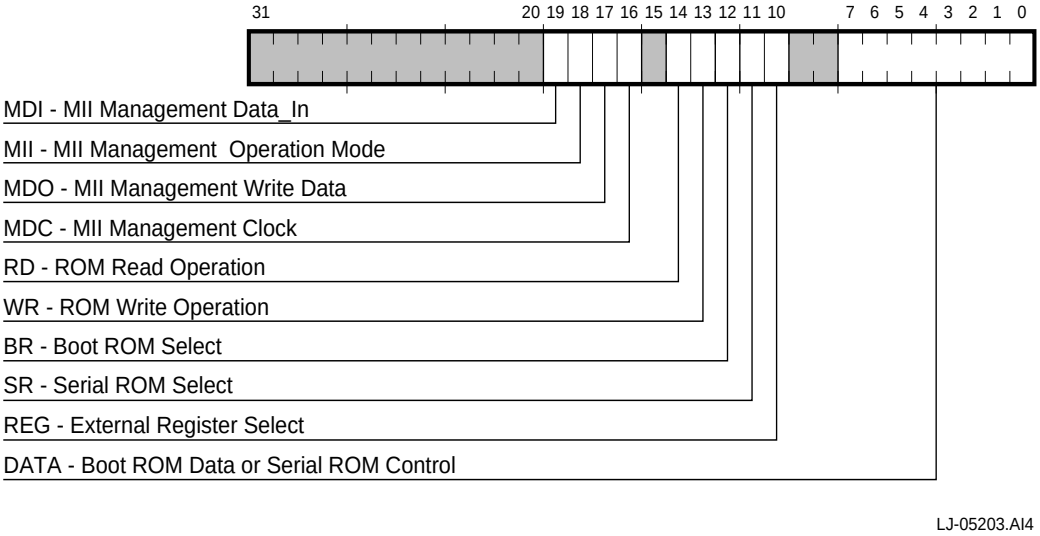

Table 3–52 describes the CSR9 register bit fields.

Table 3–52 CSR9 Register Bit Fields Description *(Sheet 1 of 2)*

Field	Description
19	**MDI—MII Management Data_In** Used by the 21143 to read data from the PHY by way of pin **mii_mdio**.
18	**MII—MII Management Operation Mode** Defines the operation mode (read or write) of the PHY. When set the PHY is in read operation mode. When clear the PHY is in write operation mode.
17	**MDO—MII Management Write Data** Specifies the value of the data that the 21143 writes to the PHY by way of pin **mii_mdio**.
16	**MDC—MII Management Clock** MII management data clock (**mii_mdc**) is an output signal to the PHY. It is used as a timing reference.

Table 3–52 CSR9 Register Bit Fields Description *(Sheet 2 of 2)*

Field	Description
14	**RD—ROM Read Operation** Read control bit. When set, together with either CSR9<12>, CSR9<11>, or CSR9<10>, the 21143 performs read cycles from the selected target (boot ROM, the serial ROM, or external register). Setting this bit together with CSR9<13> will cause **UNPREDICTABLE** behavior.
13	**WR—ROM Write Operation** Write control bit. When set, together with either CSR9<12>, CSR9<11>, or CSR9<10>, the 21143 performs write cycles to the selected target (boot ROM, the serial ROM, or external register). Setting this bit together with CSR9<14> will cause **UNPREDICTABLE** behavior.
12	**BR—Boot ROM Select** When set, the 21143 selects the boot ROM. Select only one of bits CSR9<12>, CSR9<11>, and CSR9<10>.
11	**SR—Serial ROM Select** When set, the 21143 selects the serial ROM. Select only one of bits CSR9<12>, CSR9<11>, and CSR9<10>.
10	**REG—External Register Select** When set, the 21143 selects an external register (Section 7.5). Select only one of bits CSR9<12>, CSR9<11>, and CSR9<10>.
7:0	**DATA—Boot ROM Data or Serial ROM Control** If the boot ROM is selected, this field contains the data to be read from and written to the boot ROM. If the serial ROM is selected, CSR9<3:0> bits are connected to the serial ROM control pins as follows: **Bit 3, Data Out**—This pin serially shifts the read data from the serial ROM device to the 21143. **Bit 2, Data In**—This pin serially shifts the write data from the 21143 to the serial ROM device. **Bit 1, Serial ROM Clock**—This pin provides a serial clock output to the serial ROM. **Bit 0, Serial ROM Chip Select**—This pin provides a serial ROM chip select to the serial ROM. If the external register is selected, this field contains the data to be read from and written to the external register.

Table 3–53 lists the access rules for the CSR9 register.

Table 3–53 CSR9 Register Access Rules

Category	Description
Value after reset	FFF483FFH
Read access rules	—
Write access rules	—

3.2.2.10 Boot ROM Programming Address Register (CSR10–Offset 50H)

The boot ROM programming address register (CSR10) contains the 18-bit boot ROM address.

Figure 3–22 shows the CSR10 register bit field and Table 3–54 describes the bit field.

Figure 3–22 CSR10 Register Bit Field

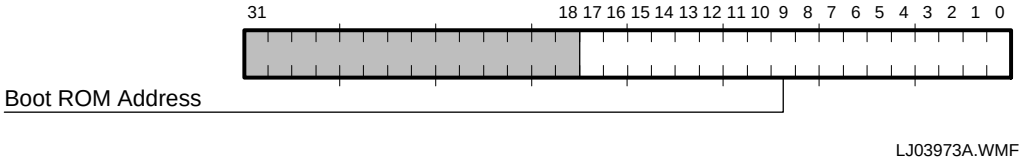

Table 3–54 CSR10 Register Bit Field Description

Field	Description
17:0	**Boot ROM Address**
	Contains a pointer to the boot ROM.

Table 3–55 lists the access rules for the CSR10 register.

Table 3–55 CSR10 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	—
Write access rules	—

3.2.2.11 General-Purpose Timer Register (CSR11–Offset 58H)

The general-purpose timer register (CSR11) contains a 16-bit general-purpose timer. It is used mainly by the software driver for timing functions not supplied by the operating system. After this timer is loaded, it starts counting down. The expiration of the timer causes an interrupt in CSR5<11>. If the timer expires and the CON bit is set, the timer will load itself automatically with the last value loaded. The value that is read by the host in this register is the current count value. The timer is not active in snooze mode. The timer reading accuracy is ±1 bit.

The timer operation is based on the existing serial clock. The cycle time of the timer depends on the port that is selected. The timer is not active in snooze mode (Section 4.3.2).

Figure 3–23 shows the CSR11 register bit fields and Table 3–56 describes the bit fields.

Figure 3–23 CSR11 Register Bit Fields

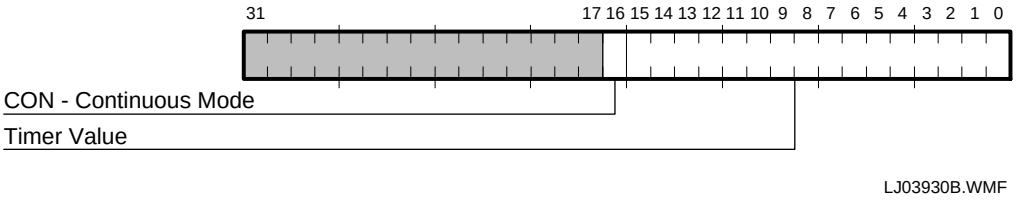

Table 3–56 CSR11 Register Bit Fields Description

Field	Description
16	**CON—Continuous Mode** When set, the general-purpose timer is in continuous operating mode. When reset, the general-purpose timer is in one-shot operating mode.
15:0	**Timer Value** Contains the number of iterations of the general-purpose timer. Each iteration duration is: 10BASE-T /AUI mode – 204.8 µs. MII/SYM 100-Mb/s mode – 81.92 µs. MII 10-Mb/s mode – 819.2 µs.

Table 3–57 lists the access rules for the CSR11 register.

Table 3–57 CSR11 Register Access Rules

Category	Description
Value after reset	FFFE0000H
Read access rules	—
Write access rules	—

3.2.2.12 SIA Status Register (CSR12–Offset 60H)

Figure 3–24 shows the CSR12 register bit fields.

Figure 3–24 CSR12 Register Bit Fields

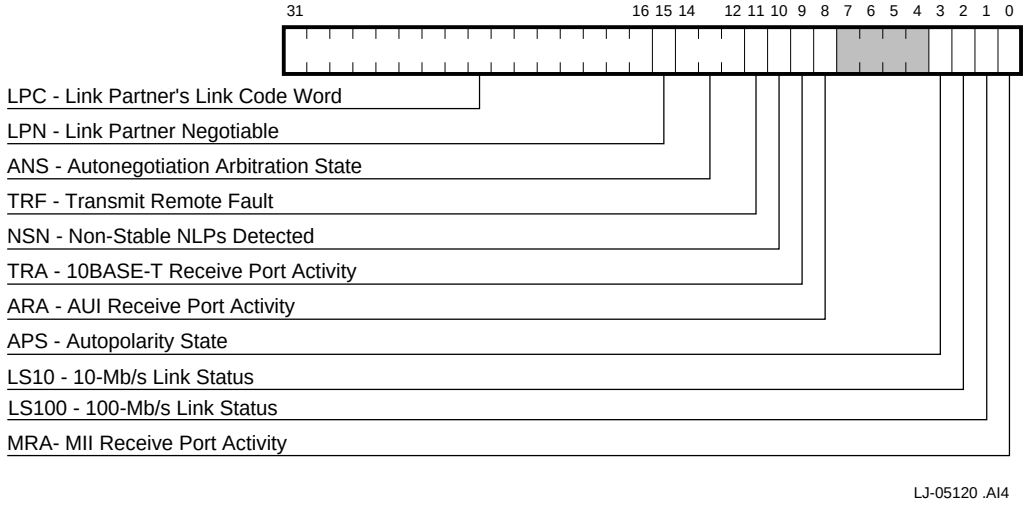

Table 3–58 describes the CSR12 register bit fields.

Table 3–58 CSR12 Register Bit Fields Description *(Sheet 1 of 3)*

Field	Description
31:16	**LPC—Link Partner's Link Code Word** These bits contain the link partner's link code word, where bit 16 is S0 (selector field bit 0) and bit 31 is NP (Next Page). Effective only when CSR12<15> is read as a logical 1.

Table 3–58 CSR12 Register Bit Fields Description *(Sheet 2 of 3)*

Field	Description
15	**LPN—Link Partner Negotiable** This bit is set when the link partner is recognized to be a device that implements the autonegotiation algorithm. Effective only when CSR14<7> is set.
14:12	**ANS—Autonegotiation Arbitration State** The CSR12<14:12> bits reflect the current autonegotiation arbitration state as follows: 000—Autonegotiation disable 001—Transmit disable 010—Ability detect 011—Acknowledge detect 100—Complete acknowledge 101—FLP link good; autonegotiation complete 110—Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated. These bits can also be used to restart the autonegotiation sequence. This is done by writing a pattern of 001 into this field, provided that autonegotiation enable (CSR14<7>) is set. Otherwise, these bits should be written as 0.
11	**TRF—Transmit Remote Fault** When set, the 21143 sets bit 13 (remote fault bit) in the transmitted link code words. This can be used to inform the link partner that some fault has occurred.
10	**NSN—Non-Stable NLPs Detected** When set, indicates that the 10BASE-T normal link pulse (NLP) is not stable. The Link Integrity Test passed for a while, but failed later during negotiation. This means that NLPs were recognized on the line, but were not stable enough to cause autonegotiation completion. This bit is cleared by a read transaction. Effective only when CSR14<7> is set.
9	**TRA—10BASE-T Receive Port Activity** Sets when there is receive activity on the 10BASE-T port. This bit is valid only if port select CSR6<18> is reset. This bit is cleared by writing 1.
8	**ARA—AUI Receive Port Activity** Sets when there is receive activity on the AUI port. This bit is valid only if port select CSR6<18> is reset. This bit is cleared by writing 1.
3	**APS—Autopolarity State** When set, the 10BASE-T polarity is positive. When reset, the 10BASE-T polarity is negative. The received bit stream is inverted by the receiver. (Refer to auto polarity enable CSR14<13> and set polarity plus CSR14<14>).

Table 3–58 CSR12 Register Bit Fields Description *(Sheet 3 of 3)*

Field	Description
2	**LS10—10-Mb/s Link Status** This bit continuously reflects the 10BASE-T link test status. When set, the 10BASE-T link test is in fail state. When reset, the 10BASE-T link test is in pass state. This bit is effective only in 10BASE-T mode, and only when CSR14<8>, Receive Squelch Enable, is set. During link fail, when in 10BASE-T mode, the 21143 does not transmit any packet to the media. However, any queued packets in the transmit list can be closed by the 21143 with the following set: TDES0<2>—Link fail TDES0<10>—No carrier TDES0<11>—Loss of carrier The 21143 moves from the link fail state to the link pass state when it receives a legal link pulse stream or two consecutive packets. The driver receives no indication about these packets. During link fail, when in 10BASE-T mode, the 21143 does not receive any packet from the media. When autonegotiation (CSR14<7>) is set, the LS10 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101 (autonegotiation completed).
1	**LS100—100-Mb/s Link Status** This bit continuously reflects the 100BASE-TX link test status. When set, the 100BASE-TX link test is in fail state. When reset, the 100BASE-TX link test is in pass state. This status is derived from the **sd** pin and is effective only when CSR6<23> (PCS function) is set. This bit is effective regardless of the status of CSR6<18> (Port Select) and CSR14<7> (Autonegotiation Enable). During link fail, when in 100BASE-TX SYM mode, the 21143 does not receive any packet from the media. When autonegotiation (CSR14<7>) is set, the LS100 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101 (autonegotiation completed).
0	**MRA—MII Receive Port Activity** Sets when there is receive activity on the MII port. This bit is cleared by writing 1.

Table 3–59 lists the access rules for the CSR12 register.

Table 3–59 CSR12 Register Access Rules

Category	Description
Value after reset	000000C6H
Read access rules	—
Write access rules	CSR12<0>, CSR12<8>, and CSR12<9> are cleared by writing 1. Writing 0 to these same bits has no effect. Writing to the remainder of the CSR12 bits (except bits 14:11) has no effect.

3.2.2.13 SIA Connectivity Register (CSR13–Offset 68H)

The SIA connectivity register (CSR13) contains the SIA connectivity control bits that permit the interconnection of different sections within the SIA. This allows coverage of the required operation and test options.

Figure 3–25 shows the CSR13 register bit fields, and Table 3–60 describes the bit fields.

Figure 3–25 CSR13 Register Bit Fields

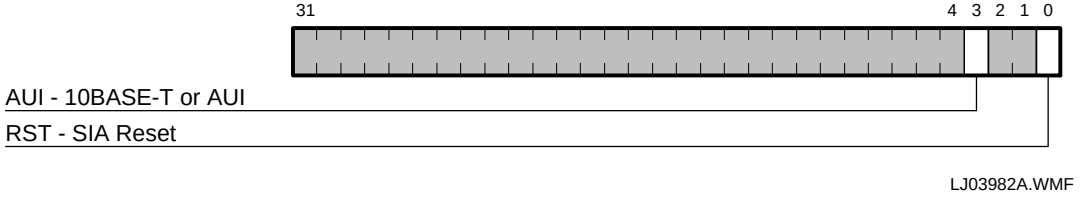

Table 3–60 CSR13 Register Bit Fields Description

Field	Description
3	**AUI—10BASE-T or AUI** When reset, forces the 21143 to select the 10BASE-T interface. When set to 1, forces the 21143 to select the AUI interface. The selection between 10BASE5 (AUI) and 10BASE2 (BNC) is done by CSR15<3>.
0	**RST—SIA Reset** When reset, resets all the SIA functions and machines.

Table 3–61 lists the access rules for the CSR13 register.

Table 3–61 CSR13 Register Access Rules

Category	Description
Value after reset	FFFF0000H
Read access rules	If CSR autoconfiguration CSR13<2>) is set, the value of CSR13 reflects the internal states rather than the values written into the CSR.
Write access rules	CSR13 should be reset to 00000000H before writing to any SIA CSR and released with or after the last CSR write transaction.

3.2.2.14 SIA Transmit and Receive Register (CSR14–Offset 70H)

The SIA transmit and receive register (CSR14) configures the SIA transmitter and receiver operating modes. Figure 3–26 shows the CSR14 register bit fields.

Figure 3–26 CSR14 Register Bit Fields

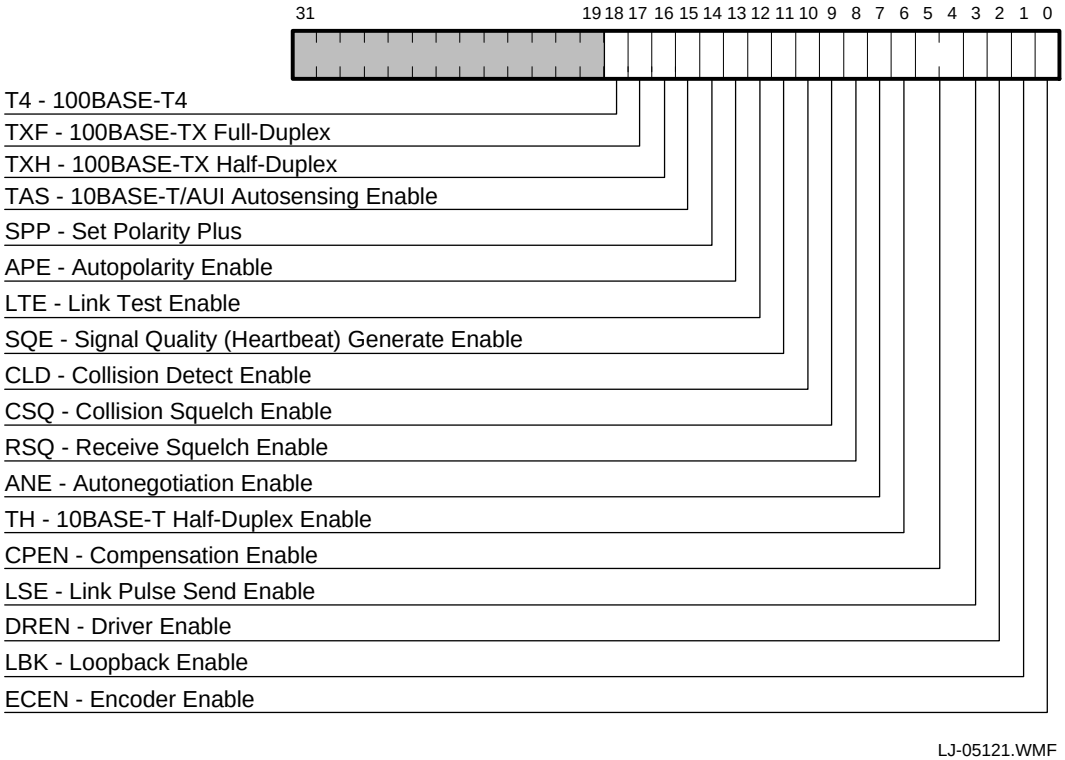

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Table 3–62 describes the bit CSR14 register bit fields.

Table 3–62 CSR14 Register Bit Fields Description *(Sheet 1 of 3)*

Field	Description
18	**T4—100BASE-T4**
	This bit controls the value of bit 9 in the transmitted link code word.
	When set, the 21143 advertises its ability to work also in 100BASE-T4 mode. (Bit 9 in the link code word is set.)
	When clear, the 21143 advertises that no 100BASE-T4 operation is allowed. (Bit 9 in the link code word is cleared.)
	This bit is meaningful only if CSR14<7> is set.
17	**TXF—100BASE-TX Full-Duplex**
	This bit controls the value of bit 8 in the transmitted link code word.
	When set, the 21143 advertises its ability to work also in 100BASE-TX full-duplex mode. (Bit 8 in the link code word is set.)
	When clear, the 21143 advertises that no 100BASE-TX full-duplex operation is allowed. (Bit 8 in the link code word is cleared.)
	This bit is meaningful only if CSR14<7> is set.
16	**TXH—100BASE-TX Half-Duplex**
	This bit controls the value of bit 7 in the transmitted link code word.
	When set, the 21143 advertises its ability to work also in 100BASE-TX half-duplex mode. (Bit 7 in the link code word is set.)
	When clear, the 21143 advertises that no100BASE-TX half-duplex operation is allowed. (Bit 7 in the link code word is clear.)
	This bit is meaningful only if CSR14<7> is set.
15	**TAS—10BASE-T/AUI Autosensing Enable**
	When set, the 21143 monitors its 10BASE-T and AUI ports. The selected port operation is not affected. See Section 6.2.7.
	When cleared, the 21143 monitors only the port that is selected for operation AUI or 10BASE-T according to CSR13<3>.
14	**SPP—Set Polarity Plus**
	When reset and autopolarity enable (CSR14<13>) is reset, the polarity of the incoming data is switched. This feature can be used by the driver to reverse polarity of incoming packets; otherwise, this bit should be set. This bit is valid only in 10BASE-T mode.

Table 3–62 CSR14 Register Bit Fields Description *(Sheet 2 of 3)*

Field	Description
13	**APE—Autopolarity Enable** When set and link test enable CSR14<12> is also set, the autopolarity function logic is enabled (Section 6.2.7). When reset, the polarity is determined by set polarity plus (CSR14<14>). When link test enable (CSR14<12>) is reset, this bit (CSR14<13>) should be also reset. This bit is valid only in 10BASE-T mode.
12	**LTE—Link Test Enable** This bit is meaningful only for the 10BASE-T port. When set, the link test function logic is enabled. Resetting this bit forces the link test function to link pass state.
11	**SQE—Signal Quality (Heartbeat) Generate Enable** Controls the signal quality (SQE) generator ability to imitate external medium attachment unit (MAU) behavior. When set, a short heartbeat signal is generated after the conclusion of a transmitted packet. In 10BASE-T mode, SQE (CSR14<11>) should be set; otherwise, a heartbeat fail (TDES0<7>) is set. In AUI mode, SQE (CSR14<11>) should be reset.
10	**CLD—Collision Detect Enable** When set, the collision detect logic is enabled.
9	**CSQ—Collision Squelch Enable** When set, the AUI collision receivers are active. This bit is valid only when AUI is selected.
8	**RSQ—Receive Squelch Enable** When set, the AUI or 10BASE-T receivers are active in accordance with the selected mode. Note that when port autosensing is enabled, the AUI and 10BASE-T receivers are active simultaneously.
7	**ANE—Autonegotiation Enable** When set, the 21143 performs an autonegotiation with the link partner to determine the operation mode (Section 6.6). When reset, autonegotiation is disabled. Autonegotiation can be performed only when in 10BASE-T mode.

Table 3–62 CSR14 Register Bit Fields Description *(Sheet 3 of 3)*

Field	Description
6	**TH—10BASE-T Half-Duplex Enable** This bit controls the value of bit 5 in the transmitted link code word. When set, the 21143 advertises its ability to also work in half-duplex mode. (Bit 5 in the link code word is set.) When clear, the 21143 advertises that no half-duplex operation is allowed. (Bit 5 in the link code word is cleared.) 10BASE-T full-duplex ability advertisement (bit 6 in the transmitted link code word) is controlled by CSR6<9> Full Duplex Mode. This bit is meaningful only if CSR14<7> is set.
5:4	**CPEN—Compensation Enable** Table 3–64 defines twisted-pair compensation behavior. These bits are valid only in 10BASE-T mode.
3	**LSE—Link Pulse Send Enable** This bit is meaningful only for the 10BASE-T port. When set, the link pulse generator is enabled.
2	**DREN—Driver Enable** When set, the transmit SIA driver is enabled for AUI or 10BASE-T operation. When reset, the transmit driver is disabled, preventing the data and link pulse transmission to the external wires.
1	**LBK—Loopback Enable** Enables loopback operation in SIA (Table 3–68 and Section 6.4.3). In AUI mode, this bit should be reset.
0	**ECEN—Encoder Enable** When set, the transmit data encoder is enabled, and the encoded data is transferred to the output drivers. When reset, the transmit data encoder is disabled, and the encoded data is blocked from propagating to the output drivers.

Table 3–63 lists the access rules for the CSR14 register.

Table 3–63 CSR14 Register Access Rules

Category	Description
Value after reset	FFFFFFFFH
Read access rules	In SIA_auto_configuration mode, a CSR14 read operation reflects internal states, rather than the values written into the CSR.
Write access rules	CSR13 should be reset to 00000000H before writing any SIA CSR and should be released with or just after the last CSR write.

Table 3–64 lists the compensation field (CSR14<5:4>) definitions.

Table 3–64 Twisted-Pair Compensation Behavior

CSR14<5:4> Value	Transmitter Output
00, 01	Compensation disabled mode—Twisted-pair driver does not compensate for 10-MHz versus 5-MHz media attenuation. (Differential voltages are bound between 1.5 V and 2.1 V.)
10	High power mode—Twisted-pair driver drives only high-differential voltage (between 2.2 V and 2.8 V).
11	Normal compensation mode—Driver compensates for 10-MHz versus 5-MHz media attenuation by driving high-differential voltage for transients and by driving low if the signal is stable for more than 50 ns.

3.2.2.15 SIA and General-Purpose Port Register (CSR15–Offset 78H)

Figure 3–27 shows the CSR15 register bit fields. CSR15 is divided into two sections: the SIA general register (CSR15<15:0>) and the general-purpose port register (CSR15<31:16>). Appendix E describes the general-purpose port programming procedures.

Figure 3–27 CSR15 Register Bit Fields

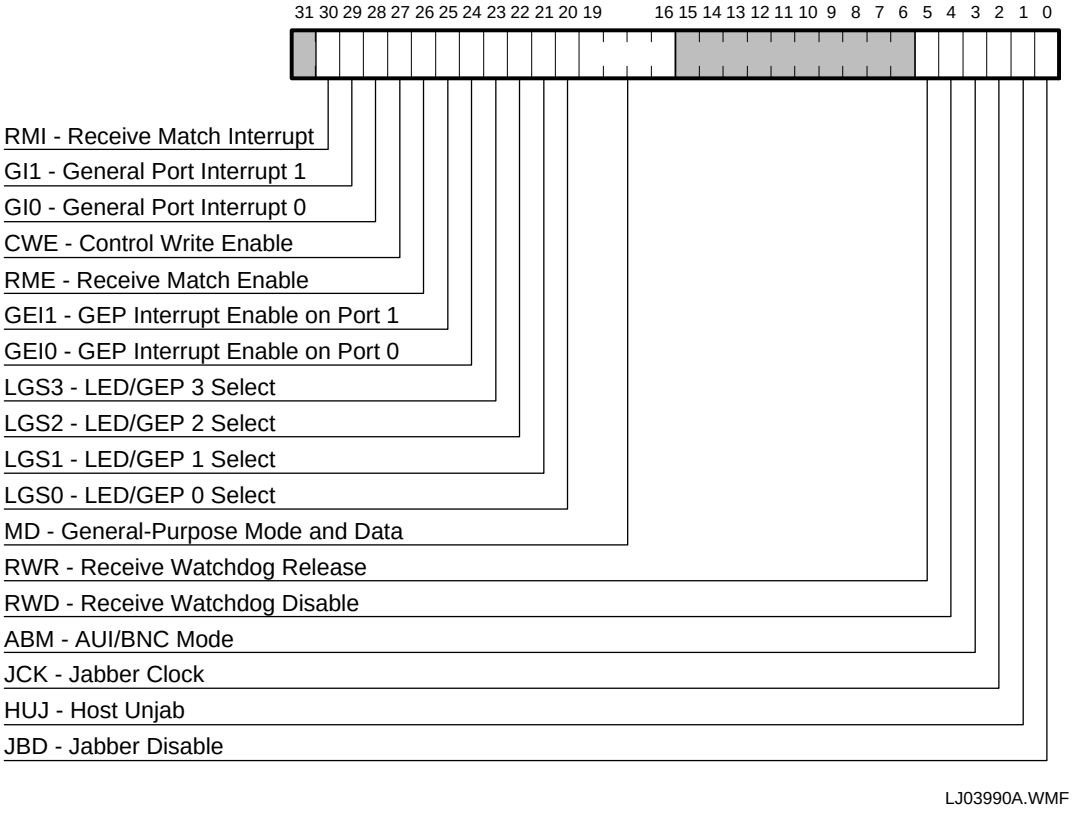

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Table 3–65 describes the bit fields.

Table 3–65 CSR15 Register Bit Fields Description *(Sheet 1 of 4)*

Field	Description
30	**RMI—Receive Match Interrupt** Indicates that a received packet has passed address filtering. This bit is cleared when reading CSR15. This bit is not automatically cleared when general purpose port interrupt (CSR5<26>) is cleared.
29	**GI1—General Port Interrupt 1** Indicates that **gep<1>** has changed state. This bit is set only when **gep<1>** is programmed to be a general-purpose input port. This bit is cleared when reading CSR15. This bit is not automatically cleared when general purpose port interrupt (CSR5<26>) is cleared.
28	**GI0—General Port Interrupt 0** Indicates that **gep<0>** has changed state. This bit is set only when **gep<0>** is programmed to be a general-purpose input port. This bit is cleared when reading CSR15. This bit is not automatically cleared when general purpose port interrupt (CSR5<26>) is cleared.
27	**CWE—Control Write Enable** When CSR15 is written and CSR15<27> value is 1, the general-purpose control bits will be written. The general-purpose control bits include interrupt enables (CSR15<26:24>), LED/GEP selects (CSR15<23:20>), and general-purpose pin directions (CSR15<19:16>). When CSR15 is written and CSR15<27> value is 0, only general-purpose data (CSR15<19:16>) will be written.
26	**RME—Receive Match Enable** When this bit is set, receive match interrupt (CSR15<30>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
25	**GEI1—GEP Interrupt Enable on Port 1** When this bit is set, the interrupt from pin **gep<1>** (CSR15<29>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.

Table 3–65 CSR15 Register Bit Fields Description *(Sheet 2 of 4)*

Field	Description
24	**GEI0—GEP Interrupt Enable on Port 0** When this bit is set, the interrupt from **gep<0>** (CSR15<28>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
23	**LGS3—LED/GEP 3 Select** This bit selects either the **10bt_link** or **gep<3>** function for 21143 pin number 103. When this bit is set, the **10bt_link** function is selected, which provides an LED indicating the status of the 10BASE-T port link integrity test (sets when the test completes successfully). When this bit is reset, the **gep<3>** function is selected. The **gep<3>** pin is a general-purpose port. After a hardware or software reset, the **gep<3>** function is selected.
22	**LGS2—LED/GEP 2 Select** This bit selects either the **rcv_match** or **gep<2>** function for 21143 pin number 102. When this bit is set, the **rcv_match** function is selected, which provides an LED indicating the status of the address recognition (sets when a packet passes address recognition). When this bit is reset, the **gep<2>** function is selected. The **gep<2>** pin is a general-purpose port. After a hardware or software reset, the **gep<2>** function is selected.
21	**LGS1—LED/GEP 1 Select** This bit selects either the **activ** or **gep<1>** function for 21143 pin number 101. When this bit is set, the **activ** function is selected, which provides an LED indicating receive or transmit activity on the selected port (sets when there is receive or transmit activity on the selected port). When this bit is reset, the **gep<1>** function is selected. The **gep<1>** pin is a general-purpose port. After a hardware or software reset, the **gep<1>** function is selected.
20	**LGS0—LED/GEP 0 Select** This bit selects either the **aui_bnc** or **gep<0>** function for 21143 pin number 100. When this bit is set, the **aui_bnc** function is selected, which provides a control line to select either 10BASE5 (AUI) or 10BASE2 (BNC) as programmed by CSR15<3>. When this bit is reset, the **gep<0>** function is selected. The **gep<0>** pin is a general-purpose port. After a hardware or software reset, the **gep<0>** function is selected.

Table 3–65 CSR15 Register Bit Fields Description *(Sheet 3 of 4)*

Field	Description
19:16	**MD—General-Purpose Mode and Data** When CSR15<27> is set, the value that is written by the host to CSR15<19:16> directs pins **gep<3:0>** to act as input or output pins (CSR15<19> controls pin **gep<3>** and so on.). A one directs the pin to be an output while a zero directs the pin to be an input. When CSR15<27> is reset, the values written to CSR15<19:16> are the values that will be driven on pins **gep<3:0>**, respectively. This is only true for the pins that are configured as output pins. After the 21143 is reset, all **gep** pins become input pins. If **gep<1:0>** pins are selected as input pins, an interrupt occurs when either of these bits change state from 1 to 0 or 0 to 1 (provided that the interrupt CSR15<25:24> is enabled). The application of the general-purpose pins in board design should be correlated with the way the port driver software is using it. Reading CSR15<19:16> returns the values of pins **gep<3:0>**.
5	**RWR—Receive Watchdog Release** Defines the time interval from receive watchdog expiration until reenabling the receive channel (*no carrier)*. When set, the receive watchdog is released 40- to 48-bit-times from the last carrier deassertion. When reset, the receive watchdog is released 16- to 24-bit-times from the last carrier deassertion.
4	**RWD—Receive Watchdog Disable** When set, the receive watchdog counter is disabled. When clear, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog counter to timeout. Packets shorter than 2048 bytes are guaranteed to pass.
3	**ABM—AUI/BNC Mode** This bit is used by the driver to select either AUI or BNC mode. When set, AUI (10BASE5) is selected. When clear, BNC (10BASE2) is selected. The value programmed to this bit is the value that is driven in the **gep<0>/aui_bnc** pin when it is set to **aui_bnc**. This pin is used mainly to enable the external BNC transceiver in 10BASE2 mode.
2	**JCK—Jabber Clock** When set, transmission is cut after 2048 bytes to 2560 bytes are transmitted (1.6 ms to 2.0 ms). When reset, transmission is cut after 26 ms to 33 ms in 10BASE-T/AUI mode or after 2.6 ms to 3.3 ms in 100-Mb/s MII/SYM mode.

Table 3–65 CSR15 Register Bit Fields Description *(Sheet 4 of 4)*

Field	Description
1	**HUJ—Host Unjab** Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the transmit jabber is released 365 ms to 420 ms after jabber expiration in 10BASE-T/AUI mode or 36.5 ms to 42 ms after jabber expiration in 100-Mb/s MII/SYM mode.
0	**JBD—Jabber Disable** When set, the transmit jabber function is disabled.

Table 3–66 lists the access rules for the CSR15 register.

Table 3–66 CSR15 Register Access Rules

Category	Description
Value after reset	8FFX0000H
Read access rules	CSR15<27:20> are write-only bits.
Write access rules	CSR13 should be reset to 00000000H before writing CSR15 bits 0 through 5 and should be released with or just after writing those bits.

3.2.2.16 SIA and MII Operating Modes

Table 3–67 and Table 3–68 list the programming of the different operating modes in the 21143 using CSR6, CSR13, CSR14, and CSR15. The states of operating mode CSR6<11:10>, full-duplex mode CSR6<9>, and port select CSR6<18> are also identified. Appendix D describes the port selection procedure.

Table 3–67 is presented here.

Table 3–67 Programming MII/SYM Operating Modes

Mode	CSR13	CSR14	CSR15<15:0>	CSR6<PS,FD>	CSR6<OM>
Half-duplex	0000	0000	0008	1,0	00
Full-duplex	0000	0000	0008	1,1	00
Internal loopback	0000	0000	0008	1,0	01
External loopback	0000	0000	0008	1,0	10

Table 3–68 is presented here.

Table 3–68 Programming 10BASE-T, AUI, and BNC Operating Modes *(Sheet 1 of 2)*

Mode	CSR13	CSR14	CSR15	AUI_BNC Pin	CSR6<PS,FD>	CSR6<OM>
Autosensing Disabled, Autonegotiation Disabled						
10BASE-T forced to half-duplex	0001	7F3F	0008	High (AUI)	0,0	00
10BASE-T forced to full-duplex	0001	7F3D	0008	High (AUI)	0,1	00
10BASE-T internal loopback	0001	7A3F	0008	High (AUI)	0,0	10
10BASE-T external loopback	0001	7B3D	0008	High (AUI)	0,0	10
BNC (10BASE2)	0009	0705	0006	Low (BNC)	0,0	00
BNC (10BASE2) external loopback	0009	0705	0006	Low (BNC)	0,0	10
AUI (10BASE5)	0009	0705	000E	High (AUI)	0,0	00
AUI (10BASE5) external loopback	0009	0705	000E	High (AUI)	0,0	10
Internal loopback in MAC level	0009	0000	0019	High (AUI)	0,0	01
Autosensing Enabled, Autonegotiation Disabled						
10BASE-T forced to half-duplex	0001	FF3F	0008	High (AUI)	0,0	00
10BASE-T forced to full-duplex	0001	FF3D	0008	High (AUI)	0,1	00
BNC (10BASE2)	0009	F73D	0006	Low (BNC)	0,0	00
AUI (10BASE5)	0009	F73D	000E	High (AUI)	0,0	00

Table 3–68 Programming 10BASE-T, AUI, and BNC Operating Modes *(Sheet 2 of 2)*

Mode	CSR13	CSR14	CSR15	AUI_BNC Pin	CSR6<PS,FD>	CSR6<OM>
Autosensing Disabled, Autonegotiation Enabled						
10BASE-T advertising half- and full-duplex	0001	7FFF	0008	High (AUI)	0,1	00
10BASE-T advertising full-duplex	0001	7FBF	0008	High (AUI)	0,1	00
10BASE-T advertising half-duplex	0001	7FFF	0008	High (AUI)	0,0	00
Autosensing Enabled, Autonegotiation Enabled						
10BASE-T advertising half- and full-duplex	0001	FFFF	0008	High (AUI)	0,1	00
10BASE-T advertising full-duplex	0001	FFBF	0008	High (AUI)	0,1	00
10BASE-T advertising half-duplex	0001	FFFF	0008	High (AUI)	0,0	00
BNC (10BASE2) advertising half- and full-duplex on TP	0009	F7FD	0006	Low (BNC)	0,1	00
BNC (10BASE2) advertising full-duplex only on TP	0009	F7BD	0006	Low (BNC)	0,1	00
BNC (10BASE2) advertising half-duplex only on TP	0009	F7FD	0006	Low (BNC)	0,0	00
AUI (10BASE5) advertising half- and full-duplex on TP	0009	F7FD	000E	High (AUI)	0,1	00
AUI (10BASE5) advertising full-duplex only on TP	0009	F7BD	000E	High (AUI)	0,1	00
AUI (10BASE5) advertising half-duplex only on TP	0009	F7FD	000E	High (AUI)	0,0	00

4
Host Communication

This chapter describes descriptor lists and data buffers, which are collectively called the host communication area, that manage the actions and status related to buffer management. Commands and signals that control the functional operation of the 21143 are also described.

Note: All shaded bits in the figures in this chapter are reserved and should be written by the driver as zero.

4.1 Data Communication

The 21143 and the driver communicate through the two following data structures:

- Control and status registers (CSRs), described in Chapter 3.
- Descriptor lists and data buffers, described in this chapter.

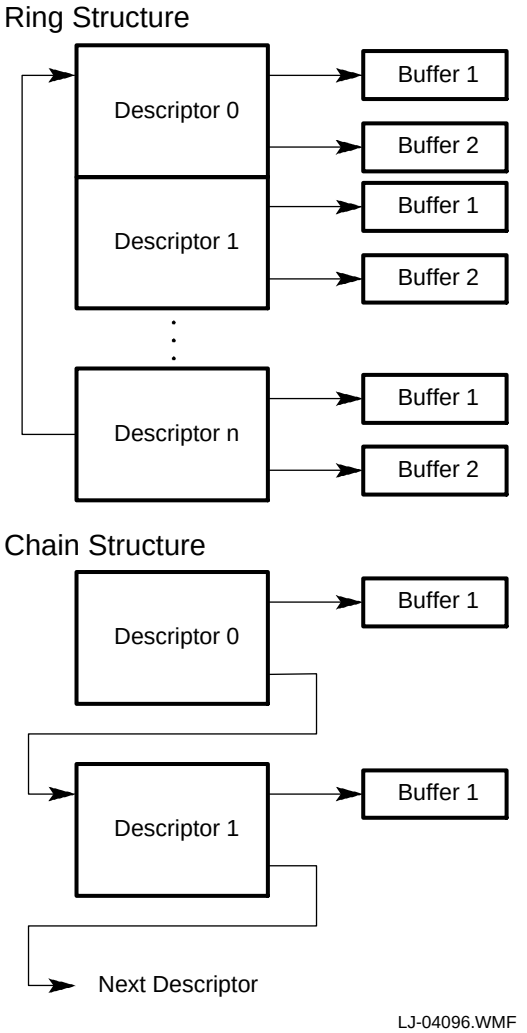
4.2 Descriptor Lists and Data Buffers

The 21143 transfers received data frames to the receive buffers in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists, one for receive and one for transmit. The base address of each list is written into CSR3 and CSR4, respectively. A descriptor list is forward linked (either implicitly or explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both the receive and transmit descriptors RDES1<24> and TDES1<24>. The descriptor lists reside in the host *physical* memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically addressed, and not contiguous in memory (Figure 4–1).

A data buffer consists of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host *physical* memory space.

Figure 4–1 Descriptor Ring and Chain Structure Examples



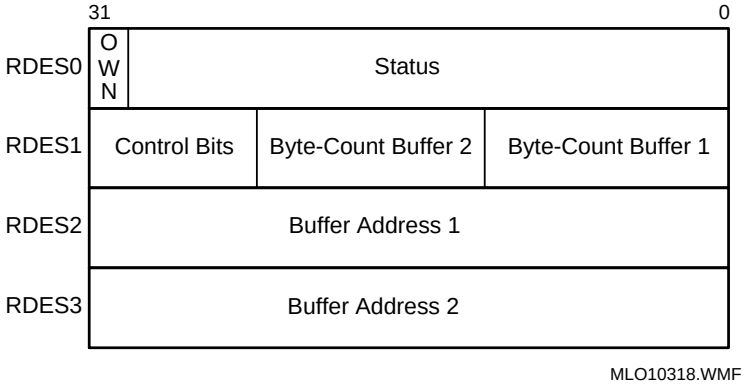
4.2.1 Receive Descriptors

Figure 4–2 shows the receive descriptor format.

Note: Descriptors and receive buffers addresses must be longword aligned.

Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory-management schemes.

Figure 4–2 Receive Descriptor Format



4.2.1.1 Receive Descriptor 0 (RDES0)

RDES0 contains the received frame status, the frame length, and the descriptor ownership information. Figure 4–3 shows the RDES0 bit fields.

Figure 4–3 RDES0 Bit Fields

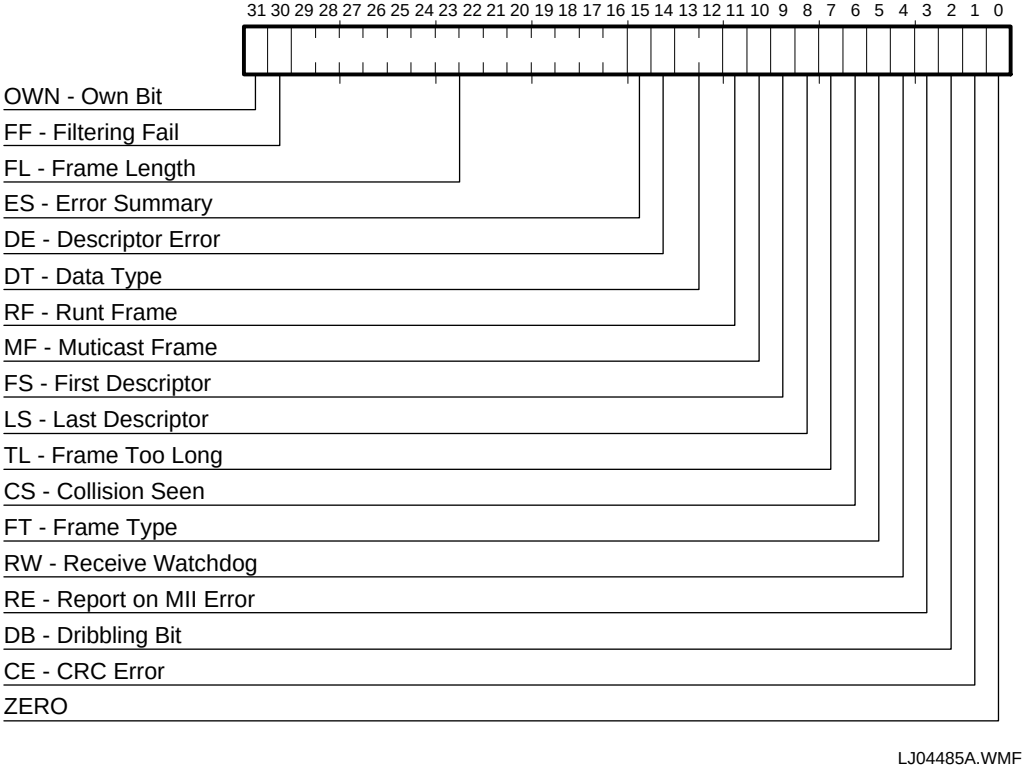


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Table 4–1 describes the bit fields.

Table 4–1 RDES0 Bit Fields Description *(Sheet 1 of 3)*

Field	Description
31	**OWN—Own Bit** When set, indicates that the descriptor is owned by the 21143. When reset, indicates that the descriptor is owned by the host. The 21143 clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	**FF—Filtering Fail** When set, indicates that the frame failed the address recognition filtering. This bit can be set only when receive all (CSR6<30>) is set. Otherwise, this bit is reset.
29:16	**FL—Frame Length** Indicates the length, in bytes, of the received frame, including the cyclic redundancy check (CRC). This field is valid only when last descriptor (RDES0<8>) is set and descriptor error (RDES0<14>) is reset.
15	**ES—Error Summary** Indicates the logical OR of the following RDES0 bits: RDES0<1>—CRC error RDES0<6>—Collision seen RDES0<7>—Frame too long RDES0<11>—Runt frame RDES0<14>—Descriptor error This bit is valid only when last descriptor (RDES0<8>) is set.
14	**DE—Descriptor Error** When set, indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the 21143 does not own the next descriptor. The frame is truncated. This bit is valid only when last descriptor (RDES0<8>) is set.

Table 4–1 RDES0 Bit Fields Description *(Sheet 2 of 3)*

Field	Description
13:12	**DT—Data Type** Indicates the type of frame the buffer contains: 00—Serial received frame. 01—Internal loopback frame. 10—External loopback frame or serial received frame. The 21143 does not differentiate between loopback and serial received frames; therefore, this information is global and reflects only the operating mode (CSR6<11:10>). 11—Reserved. This field is valid only when last descriptor (RDES0<8>) is set.
11	**RF—Runt Frame** When set, indicates that this frame was damaged by a collision or premature termination before the collision window had passed. Runt frames are passed on to the host only if the pass bad frames bit (CSR6<3>) is set. This bit is valid only when last descriptor (RDES0<8>) is set and overflow (RDES0<0>) is reset.
10	**MF—Multicast Frame** When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor (RDES0<8>) is set.
9	**FS—First Descriptor** When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the second buffer contains the beginning of the frame. If the buffer size of the second buffer is also 0, the second descriptor contains the beginning of the frame.
8	**LS—Last Descriptor** When set, indicates that the buffers pointed to by this descriptor are the last buffers of the frame.
7	**TL—Frame Too Long** When set, indicates that the frame length exceeds the maximum Ethernet-specified size of 1518 bytes. This bit is valid only when last descriptor (RDES0<8>) is set. **Note:** Frame too long is only a frame length indication and does not cause any frame truncation.

Table 4–1 RDES0 Bit Fields Description *(Sheet 3 of 3)*

Field	Description
6	**CS—Collision Seen** When set, indicates that the frame was damaged by a collision that occurred after the 64 bytes following the start frame delimiter (SFD). This is a late collision. This bit is valid only when last descriptor (RDES0<8>) is set.
5	**FT—Frame Type** When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames of less than 14 bytes. This bit is valid only when last descriptor (RDES0<8>) is set.
4	**RW—Receive Watchdog** When set, indicates that the receive watchdog timer expired while receiving the current packet with length greater than 2048 bytes through 2560 bytes. Receive watchdog timeout (CSR5<9>) is set. When RDES0<4> is set, the frame length field in RDES0<30:16> is not valid. This bit is valid only when last descriptor (RDES0<8>) is set.
3	**RE—Report on MII Error** When set, indicates that a receive error in the physical layer was reported during the frame reception.
2	**DB—Dribbling Bit** When set, indicates that the frame contained a noninteger multiple of 8 bits. This error is reported only if the number of dribbling bits in the last byte is 4 in MII operating mode, or at least 3 in 10-Mb/s serial operating mode. This bit is not valid if either collision seen (RDES0<6>) or runt frame (RDES0<11>) is set. If set, and the CRC error (RDES0<1>) is reset, then the packet is valid. This bit is valid only when last descriptor (RDES0<8>) is set.
1	**CE—CRC Error** When set, indicates that a cyclic redundancy check (CRC) error occurred on the received frame. This bit is also set when the **mii_err** pin is asserted during the reception of a receive packet even though the CRC may be correct. This bit is valid only when last descriptor (RDES0<8>) is set.
0	**ZERO** This bit is always zero for a packet with legal length.

4.2.1.2 Receive Descriptor 1 (RDES1)

Figure 4–4 shows the RDES1 bit fields.

Figure 4–4 RDES1 Bit Fields

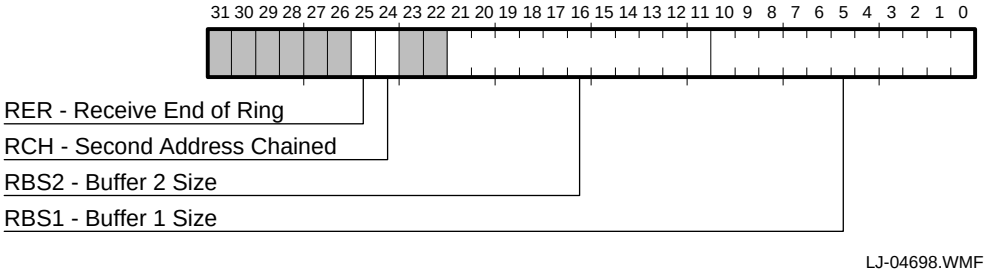


Table 4–2 describes the RDES1 bit fields.

Table 4–2 RDES1 Bit Fields Description

Field	Description
25	**RER—Receive End of Ring** When set, indicates that the descriptor list reached its final descriptor. The 21143 returns to the base address of the list (Section 3.2.2.4), creating a descriptor ring.
24	**RCH—Second Address Chained** When set, indicates that the second address in the descriptor is the next descriptor address, rather than the second buffer address. RDES1<25> takes precedence over RDES1<24>.
21:11	**RBS2—Buffer 2 Size** Indicates the size, in bytes, of the second data buffer. If this field is 0, the 21143 ignores this buffer and fetches the next descriptor. The buffer size must be a multiple of 4. This field is not valid if RDES1<24> is set.
10:0	**RBS1—Buffer 1 Size** Indicates the size, in bytes, of the first data buffer. If this field is 0, the 21143 ignores this buffer and uses buffer 2. The buffer size must be a multiple of 4.

4.2.1.3 Receive Descriptor 2 (RDES2)

Figure 4–5 shows the RDES2 bit field.

Figure 4–5 RDES2 Bit Field

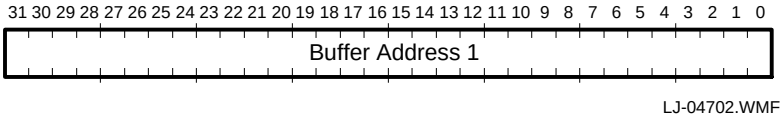


Table 4–3 describes the RDES2 bit field.

Table 4–3 RDES2 Bit Field Description

Field	Description
31:0	**Buffer Address 1** Indicates the physical address of buffer 1. The buffer must be longword aligned (RDES2<1:0> = 00).

4.2.1.4 Receive Descriptor 3 (RDES3)

Figure 4–6 shows the RDES3 bit field.

Figure 4–6 RDES3 Bit Field

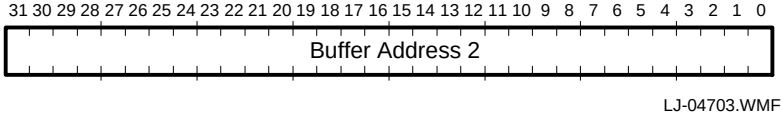


Table 4–4 describes the RDES3 bit field.

Table 4–4 RDES3 Bit Field Description

Field	Description
31:0	**Buffer Address 2** Indicates the physical address of buffer 2. The buffer must be longword aligned (RDES3<1:0> = 00).

4.2.1.5 Receive Descriptor Status Validity

Table 4–5 lists the validity of the receive descriptor status bits in relation to the reception completion status.

Table 4–5 Receive Descriptor Status Validity

Reception	Receive Status Report							
Status	**RF**	**CS**	**FT**	**FF**	**DB**	**CE**	**RE**	**(ES, DE, DT, FS, LS, FL, OF)**
Overflow	0	0	V	V	NV	NV	V	V
Collision after 512 bits	V	V	V	V	V	V	V	V
Runt frame	V	V	V	V	V	V	V	V
Runt frame less than 14 bytes	V	V	NV	NV	V	V	V	V
Watchdog timeout	0	V	V	V	NV	NV	V	V

List of table abbreviations

RF—Runt frame (RDES0<11>)
CS—Collision seen (RDES0<6>)
FT—Frame type (RDES0<5>)
FF—Filtering fail (RDES0<30>)
DB—Dribbling bit (RDES0<2>)
CE—CRC error (RDES0<1>)
RE—Report on MII error (RDES0<3>)
ES—Error summary (RDES0<15>)
DE—Descriptor error (RDES0<14>)
DT—Data type (RDES0<13:12>)
FS—First descriptor (RDES0<9>)
LS—Last descriptor (RDES0<8>)
FL—Frame length (RDES0<30:16>)
OF—Overflow (RDES0<0>)
V—Valid
NV—Not valid

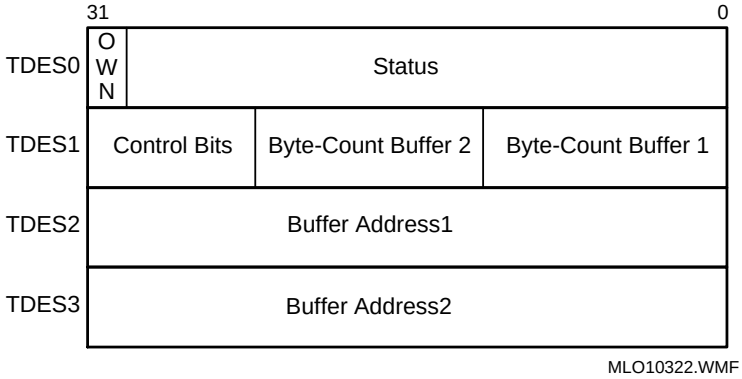
4.2.2 Transmit Descriptors

Figure 4–7 shows the transmit descriptor format.

Note: Descriptor addresses must be longword aligned.

Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory-management schemes.

Figure 4–7 Transmit Descriptor Format



4.2.2.1 Transmit Descriptor 0 (TDES0)

TDES0 contains transmitted frame status and descriptor ownership information. Figure 4–8 shows the TDES0 bit fields.

Figure 4–8 TDES0 Bit Fields

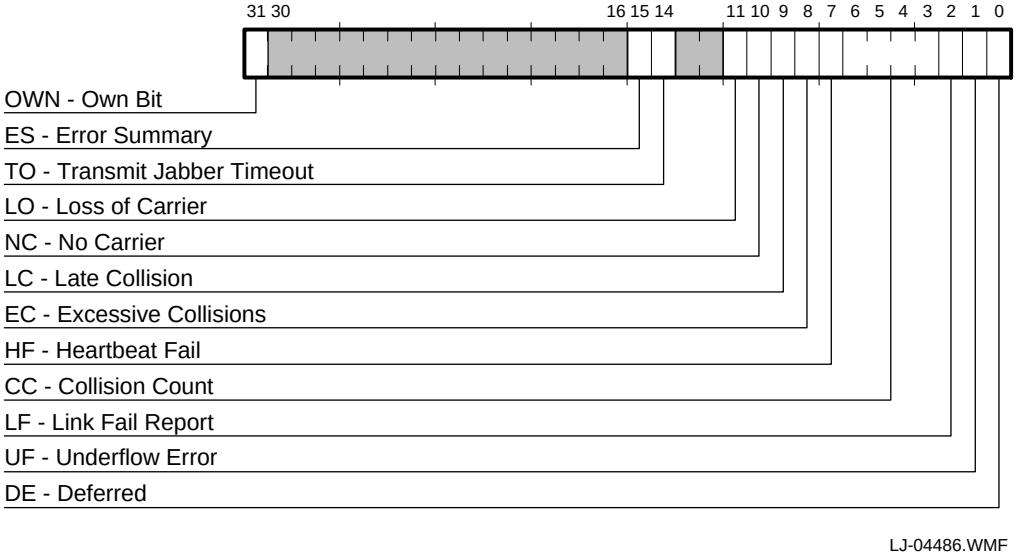


Table 4–6 describes the TDES0 bit fields.

Table 4–6 TDES0 Bit Fields Description *(Sheet 1 of 2)*

Field	Description
31	**OWN—Own Bit** When set, indicates that the descriptor is owned by the 21143. When cleared, indicates that the descriptor is owned by the host. The 21143 clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are empty. The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the 21143 fetching a descriptor and the driver setting an ownership bit.
15	**ES—Error Summary** Indicates the logical OR of the following bits: TDES0<1>—Underflow error TDES0<8>—Excessive collisions TDES0<9>—Late collision TDES0<10>—No carrier TDES0<11>—Loss of carrier TDES0<14>—Transmit jabber timeout summary
14	**TO—Transmit Jabber Timeout** When set, indicates that the transmit jabber timer timed out and that the 21143 transmitter was still active. The transmit jabber timeout interrupt CSR5<3> is set. The transmission process is *aborted* and placed in the STOPPED state. When TDES0<14> is set, any heartbeat fail indication (TDES0<7>) is not valid.
11	**LO—Loss of Carrier** When set, indicates loss of carrier during transmission. Not valid in internal loopback mode (CSR6<11:10>=01).
10	**NC—No Carrier** When set, indicates that the carrier signal from the transceiver was not present during transmission. Not valid in internal loopback mode (CSR6<11:10>=01).
9	**LC—Late Collision** When set, indicates that the frame transmission was aborted due to collision occurring after the collision window of 64 bytes. Not valid if underflow error (TDES0<1>) is set.
8	**EC—Excessive Collisions** When set, indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame.

Table 4–6 TDES0 Bit Fields Description *(Sheet 2 of 2)*

Field	Description
7	**HF—Heartbeat Fail** This bit is effective only in 10BASE-T/AUI operating mode. When set, this bit indicates a heartbeat collision check failure (the transceiver failed to return a collision pulse as a check after the transmission). For transceivers that do not support heartbeat collision check, heartbeat fail is set but is not valid. This bit is not valid if underflow error (TDES0<1>) is set. On the second transmission attempt, after the first transmission was aborted due to a collision, the 21143 does not check heartbeat fail (TDES0<7>) and is reset.
6:3	**CC—Collision Count** This 4-bit counter indicates the number of collisions that occurred before the frame was transmitted. Not valid when the excessive collisions bit (TDES0<8>) is also set.
2	**LF—Link Fail Report** When set, indicates that the link test failed before the frame was transmitted. This bit is only valid in 10BASE-T mode (CSR6<18> = 0, CSR13<3> = 0) and 100-Mb/s SYM mode (CSR6<18> = 1, CSR6<23> = 1).
1	**UF—Underflow Error** When set, indicates that the transmitter aborted the message because data arrived late from memory. Underflow error indicates that the 21143 encountered an empty transmit FIFO while transmitting a frame. The transmission process enters the suspended state and sets both transmit underflow (CSR5<5>) and transmit interrupt (CSR5<0>).
0	**DE—Deferred** When set, indicates that the 21143 had to defer while ready to transmit a frame because the carrier was asserted.

4.2.2.2 Transmit Descriptor 1 (TDES1)

Figure 4–9 shows the TDES1 bit fields

Figure 4–9 TDES1 Bit Fields

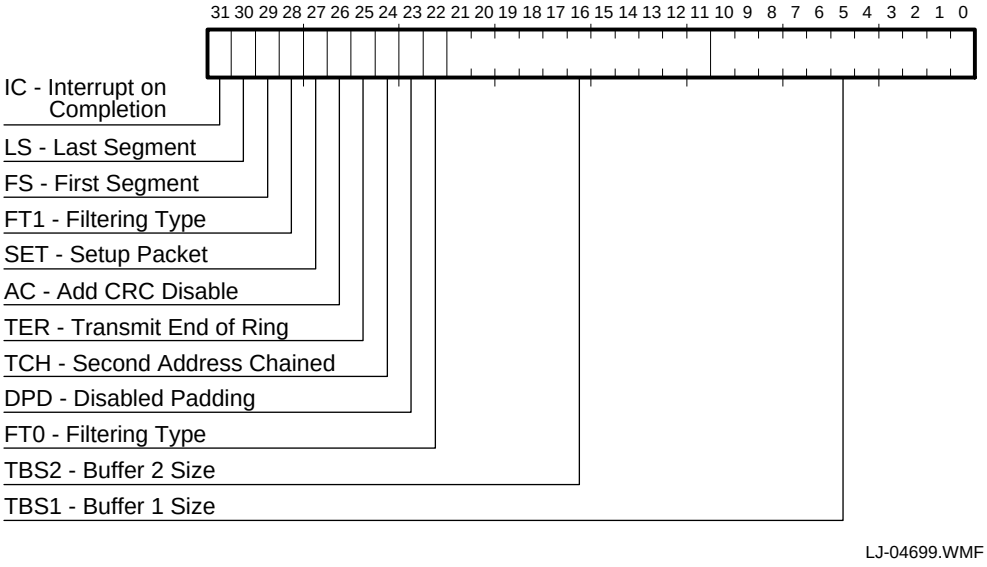


Table 4–7 describes the bit fields.

Table 4–7 TDES1 Bit Fields Description *(Sheet 1 of 2)*

Field	Description
31	**IC—Interrupt on Completion** When set, the 21143 sets transmit interrupt (CSR5<0>) after the present frame has been transmitted. It is valid only when last segment (TDES1<30>) is set or when it is a setup packet.
30	**LS—Last Segment** When set, indicates that the buffer contains the last segment of a frame.
29	**FS—First Segment** When set, indicates that the buffer contains the first segment of a frame.

Table 4–7 TDES1 Bit Fields Description *(Sheet 2 of 2)*

Field	Description
28	**FT1—Filtering Type** This bit is valid only when setup packet (TDES1<27>) is set. Table 4–8 lists the filtering types.
27	**SET—Setup Packet** When set, indicates that the current descriptor is a setup frame descriptor (Section 4.2.3).
26	**AC—Add CRC Disable** When set, the 21143 does not append the cyclic redundancy check (CRC) to the end of the transmitted frame. This field is valid only when first segment (TDES1<29>) is set.
25	**TER—Transmit End of Ring** When set, indicates that the descriptor pointer has reached its final descriptor. The 21143 returns to the root address of the list (Section 3.2.2.4). This creates a descriptor ring.
24	**TCH—Second Address Chained** When set, indicates that the second address in the descriptor is the next descriptor address, rather than the second buffer address. Transmit end of ring (TDES1<25>) takes precedence over second address chained (TDES1<24>).
23	**DPD—Disabled Padding** When set, the 21143 does not automatically add a padding field, to a packet shorter than 64 bytes. When reset, the 21143 automatically adds a padding field and also a CRC field to a packet shorter than 64 bytes. The CRC field is added despite the state of the add CRC disable (TDES1<26>) flag.
22	**FT0—Filtering Type** This bit is valid only when setup packet (TDES1<27>) is set. Table 4–8 lists the filtering types.
21:11	**TBS2—Buffer 2 Size** Indicates the size, in bytes, of the second data buffer. If this field is 0, the 21143 ignores this buffer and fetches the next descriptor. This field is not valid if second address chained (TDES1<24>) is set.
10:0	**TBS1—Buffer 1 Size** Indicates the size, in bytes, of the first data buffer. If this field is 0, the 21143 ignores this buffer and uses buffer 2.

Table 4–8 lists the filtering types. Table 3–46 provides additional information on filtering.

Table 4–8 Filtering Type

FT1	FT0	Description
0	0	**Perfect Filtering** The 21143 interprets the descriptor buffer as a setup perfect table of 16 addresses, and sets the 21143 filtering mode to perfect filtering.
0	1	**Hash Filtering** The 21143 interprets the descriptor buffer as a setup hash table of 512-bit-plus-one perfect address. If an incoming receive packet destination address is a multicast address, the 21143 executes an imperfect address filtering compared with the hash table. However, if the incoming receive packet destination address is a physical address, the 21143 executes a perfect filtering compared with the perfect address.
1	0	**Inverse Filtering** The 21143 interprets the descriptor buffer as a setup perfect table of 16 addresses and sets the 21143 filtering mode to inverse filtering. The 21143 receives the incoming frames with destination addresses not matching the perfect addresses and rejects the frames with destination addresses matching one of the perfect addresses.
1	1	**Hash-Only Filtering** The 21143 interprets the descriptor buffer as a setup 512-bit hash table. If an incoming receive packet destination address is multicast or physical, the 21143 executes an imperfect address filtering against the hash table.

4.2.2.3 Transmit Descriptor 2 (TDES2)

Figure 4–10 shows the TDES2 bit field.

Figure 4–10 TDES2 Bit Field

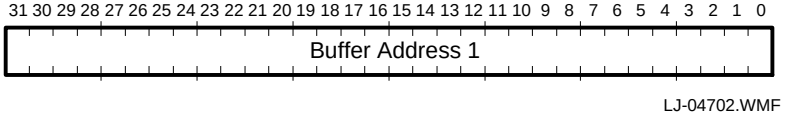


Table 4–9 describes the TDES2 bit field.

Table 4–9 TDES2 Bit Field Description

Field	Description
31:0	**Buffer Address 1** Physical address of buffer 1. There are no limitations on the buffer address alignment.

4.2.2.4 Transmit Descriptor 3 (TDES3)

Figure 4–11 shows the TDES3 bit field.

Figure 4–11 TDES3 Bit Field

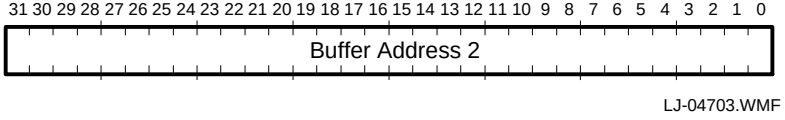


Table 4–10 describes the bit field.

Table 4–10 TDES3 Bit Field Description

Field	Description
31:0	**Buffer Address 2** Physical address of buffer 2. There are no limitations on the buffer address alignment.

4.2.2.5 Transmit Descriptor Status Validity

Table 4–11 lists the validity of the transmit descriptor status bits during transmission completion status.

Table 4–11 Transmit Descriptor Status Validity

	Transmit Status Report						
Transmission Status	**LO**	**NC**	**LC**	**EC**	**HF**	**CC**	**(ES, TO, UF, DE)**
Underflow	V	V	V	V	V	V	V
Excessive collisions	V	V	V	V	V	NV	V
Watchdog timeout	NV	V	NV	NV	NV	V	V
Internal loopback	NV	NV	V	V	NV	V	V

List of table abbreviations

LO—Loss of carrier (TDES0<11>)
NC—No carrier (TDES0<10>)
LC—Late collision (TDES0<9>)
EC—Excessive collisions (TDES0<8>)
HF—Heartbeat fail (TDES0<7>)
CC—Collision count (TDES0<6:3>)
ES—Error summary (TDES0<15>)
TO—Transmit jabber timeout (TDES0<14>)
UF—Underflow error (TDES0<1>)
DE—Deferred (TDES0<0>)
V—Valid
NV—Not valid

4.2.3 Setup Frame

A setup frame defines the 21143 Ethernet addresses that are used to filter all incoming frames. The setup frame is *never* transmitted on the Ethernet wire nor is it looped back to the receive list. When processing the setup frame, the receiver logic temporarily disengages from the Ethernet wire. The setup frame size must be *exactly* 192 bytes.

Note: The setup frame must be allocated in a single buffer that is longword aligned. First segment (TDES1<29>) and last segment (TDES1<30>) must both be 0.

When the setup frame load is completed, the 21143 closes the setup frame descriptor by clearing its ownership bit and by setting all other bits to 1.

4.2.3.1 First Setup Frame

A setup frame must be processed before the reception process is started, except when it operates in promiscuous filtering mode.

4.2.3.2 Subsequent Setup Frames

Subsequent setup frames may be queued to the 21143 despite the reception process state. To ensure correct setup frame processing, these packets may be queued at the beginning of the transmit descriptor's ring or following a descriptor with a zero-length buffer. For the descriptor with a zero-length buffer, it should contain the following information:

TDES0<31> = 1 (Adapter-owned descriptor)
TDES1<30> = 0 (Last segment bit 0)
TDES1<29> = 0 (First segment bit 0)
TDES1<21:11> = 0 (Transmit buffer 2 empty)
TDES1<10:0> = 0 (Transmit buffer 1 empty)

Setup packet (TDES1<27>) may also be set. If so, the address filtering bits (TDES1<22> and TDES1<28>) should be the same as in the previous packet. For setup frame processing, the transmission process must be running. The setup frame is processed after all preceding frames have been transmitted and the current frame reception, if any, is completed.

The setup frame does not affect the reception process state, but during setup frame processing, the 21143 is disengaged from the Ethernet wire.

4.2.3.3 Perfect Filtering Setup Frame Buffer

This section describes how the 21143 interprets a setup frame buffer in perfect filtering mode (CSR6<0> = 0).

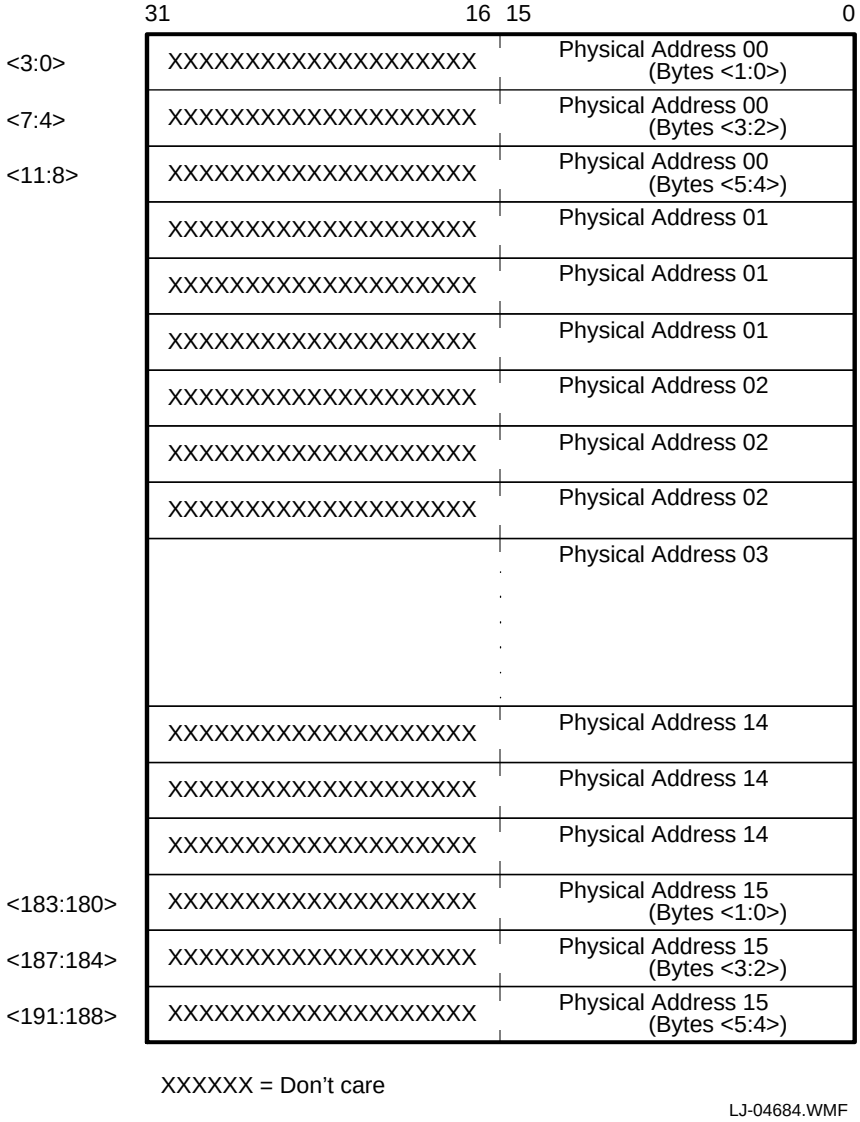
The 21143 can store 16 destination addresses (full 48-bit Ethernet addresses). The 21143 compares the addresses of any incoming frame to these addresses, and also tests the status of the inverse filtering (CSR6<4>). It rejects addresses that:

- Do not match if inverse filtering (CSR6<4>) is reset.
- Match if inverse filtering is set.

The setup frame must *always* supply all 16 addresses. Any mix of physical and multicast addresses can be used. Unused addresses should duplicate one of the valid addresses.

Figure 4–12 shows the perfect filtering setup frame buffer format of the addresses.

Figure 4–12 Perfect Filtering Setup Frame Buffer Format



The low-order bit of the low-order bytes is the multicast bit of the address.

Example 4–1 shows a perfect filtering setup buffer (fragment).

Example 4–1 Perfect Filtering Buffer

```
Ethernet addresses to be filtered:

  A8-09-65-12-34-76  ❶
  09-BC-87-DE-03-15
    .
    .
    .

Setup frame buffer fragment while in little endian
byte ordering:

  xxxx09A8  ❷
  xxxx1265
  xxxx7634
  xxxxBC09
  xxxxDE87
  xxxx1503
    .
    .
    .
Setup frame buffer fragment while in big endian byte ordering:

  A809xxxx  ❸
  6512xxxx
  3476xxxx
  09BCxxxx
  87DExxxx
  0315xxxx
    .
    .
    .
```

❶ Displays two Ethernet addresses written according to the Ethernet specification for address display.

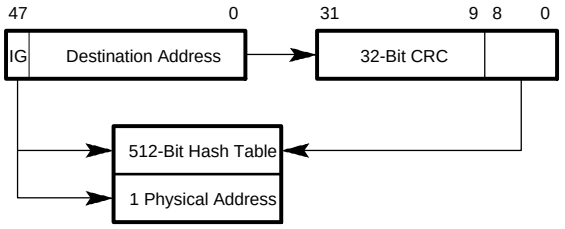
❷ Displays two addresses as they would appear in the buffer in little endian format.

❸ Displays two addresses as they would appear in the buffer in big endian format.

4.2.3.4 Imperfect Filtering Setup Frame Buffer

This section describes how the 21143 interprets a setup frame buffer in imperfect filtering mode (CSR6<0> is set). Figure 4–13 shows imperfect filtering.

Figure 4–13 Imperfect Filtering



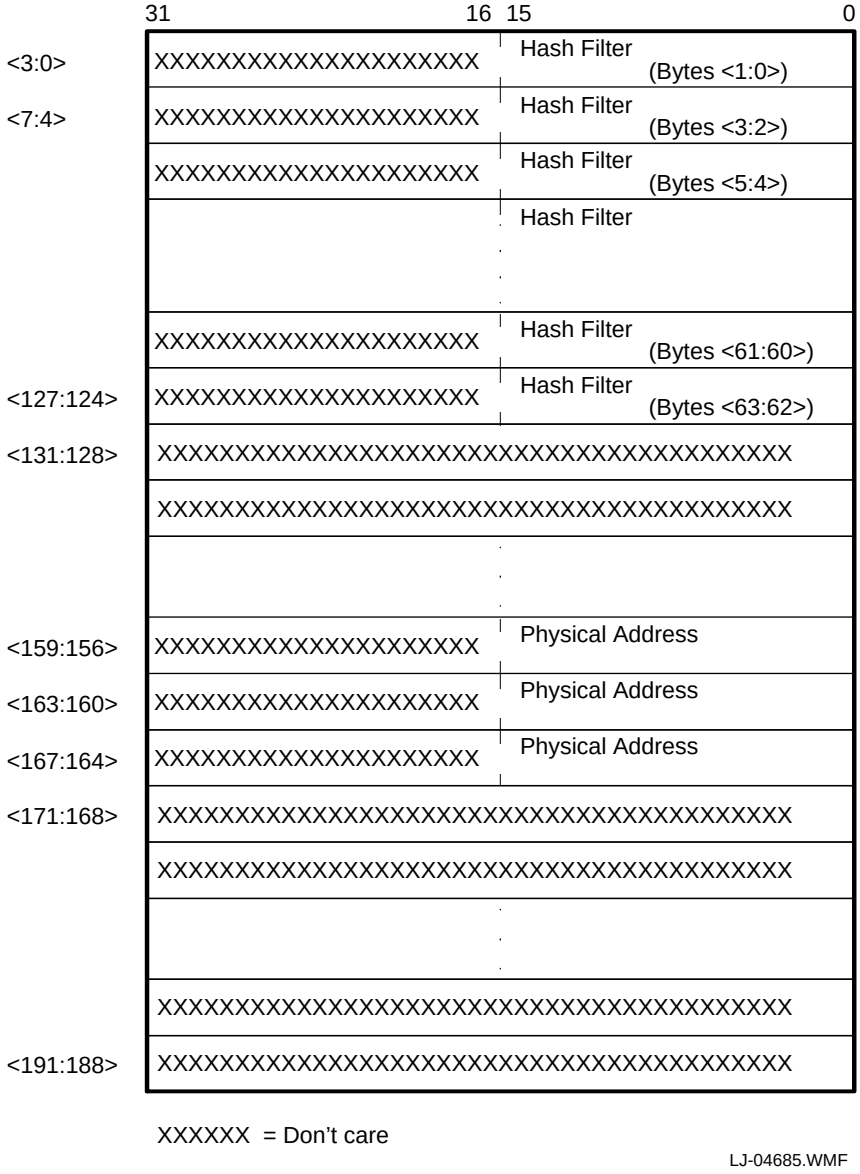
The 21143 can store 512 bits serving as hash bucket heads, and one *physical* 48-bit Ethernet address. Incoming frames with multicast destination addresses are subjected to imperfect filtering. Frames with physical destination addresses are checked against the single physical address.

For any incoming frame with a multicast destination address, the 21143 applies the standard Ethernet cyclic redundancy check (CRC) function to the first 6 bytes containing the destination address, then it uses the most significant 9 bits of the result as a bit index into the table. If the indexed bit is set, the frame is accepted. If the bit is cleared, the frame is rejected. (Appendix C provides an example of a hash index for a given Ethernet address.)

This filtering mode is called imperfect because multicast frames not addressed to this station may slip through, but it still decreases the number of frames that the host can receive.

Figure 4–14 shows the format for the hash table and the physical address.

Figure 4–14 Imperfect Filtering Setup Frame Buffer Format



Bits are sequentially numbered from right to left and down the hash table. For example, if the CRC (destination address) <8:0> = 33, the 21143 examines bit 1 in the third longword.

Example 4–2 shows an imperfect filtering setup frame buffer.

Example 4–2 Imperfect Filtering Buffer

```
Ethernet addresses to be filtered:
  25-00-25-00-27-00  ❶
  A3-C5-62-3F-25-87
  D9-C2-C0-99-0B-82
  7D-48-4D-FD-CC-0A
  E7-C1-96-36-89-DD
  61-CC-28-55-D3-C7
  6B-46-0A-55-2D-7E

  A8-12-34-35-76-08  ❷

Setup frame buffer while in little endian byte ordering:

  xxxx0000  ❸
  xxxx0000
  xxxx0000
  xxxx1000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx4000
  xxxx0080
  xxxx0000
  xxxx0000
  xxxx0010
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx1000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0000
  xxxx0001
  xxxx0000
```

Example 4-2 Imperfect Filtering Buffer (Cont.)

```
xxxx0000
xxxx0000
xxxx0040
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx

xxxx12A8  ❹
xxxx3534
xxxx0876
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx

Setup frame buffer while in big endian byte ordering:
0000xxxx  ❺
0000xxxx
0000xxxx
0010xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0040xxxx
8000xxxx
0000xxxx
0000xxxx
1000xxxx
0000xxxx
0000xxxx
0000xxxx
0010xxxx
0000xxxx
```

Example 4-2 Imperfect Filtering Buffer (Cont.)

```
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0000xxxx
0100xxxx
0000xxxx
0000xxxx
0000xxxx
4000xxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx

A812xxxx  ❻
3435xxxx
7608xxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
xxxxxxxx
```

❶ Displays Ethernet multicast addresses written according to the Ethernet specification for address display.

❷ Displays an Ethernet physical address.

❸ Displays the first part of an imperfect filter setup frame buffer, in little endian byte ordering, with set bits for the multicast addresses as in ❶.

❹ Displays the second part of the buffer with the physical address as in ❷, in little endian byte ordering.

❺ Displays the first part of an imperfect filter setup frame buffer, in big endian byte ordering, with set bits for the multicast addresses as in ❶.

❻ Displays the second part of the buffer with the physical address as in ❷, in big endian byte ordering.

4.3 Functional Description

This section describes the reset commands, interrupt handling, and startup. It also describes the transmit and receive processes.

The functional operation of the 21143 is controlled by the driver interface located in the host communication area. The driver interface activity is controlled by control and status registers (CSRs), descriptor lists, and data buffers.

Descriptor lists and data buffers, collectively referred to as the host communication area, reside in host memory. These data structures process the actions and status related to buffer management. The 21143 transfers frame data to and from the receive and transmit buffers in host memory. Descriptors resident in the host memory point to these buffers.

4.3.1 Reset Commands

The following two commands are available to reset the 21143 hardware and software:

- Assert **rst_l**, to initiate a hardware reset.
- Assert CSR0<0>, to initiate a software reset.

For a proper hardware reset, both **pci_clk** and **xtal1** clocks should be active. Note that after a hardware reset, the mode is set to 10BASE-T/AUI. For a proper software reset, both **pci_clk** and the correct serial clock (for example, **mii_tclk** when in MII mode or **xtal1** when in either 10BASE-T or AUI mode) should be active. For both the hardware and software reset commands, the 21143 *aborts* all processing and starts the reset sequence. The 21143 initializes all internal states and registers.

Note: No internal states are retained, no descriptors are owned, and all the host-visible registers are set to the reset values. However, a software reset command has no effect on the configuration registers or on CSR6<18> port select.

The 21143 does not explicitly disown any owned descriptor; descriptor-owned bits can be left in a state indicating 21143 ownership. Section 4.2.1.1 and Section 4.2.2.1 provide a detailed description of own bits.

After either a hardware or software reset command, the first bus transaction to the 21143 should not be initiated for at least 50 PCI clock cycles. When the reset sequence completes, the 21143 can accept host commands. The receive and transmit processes are placed in the stopped state (Table 4–13 and Table 4–14). It is permissible to issue successive reset commands (hardware or software).

4.3.2 Power-Saving Modes

The 21143 incorporates two different power-saving modes: sleep mode and snooze mode. The following subsections describe these power-saving modes.

4.3.2.1 Sleep Power-Saving Mode

Sleep mode can be activated when the 21143 is not being used (for example, not connected to the network) and it is important to reduce its power dissipation. While in sleep mode, most of the internal circuits are disabled. This includes the DMA machine, FIFOs, RxM, TxM, SIA, twisted-pair interface, AUI interface, and the general-purpose timer. The PCI section is not affected and access to the 21143 configuration registers remains possible. Access to the 21143 CSRs is not allowed.

To enter sleep mode, the driver must take the following actions:

1. Stop the receive and transmit processes by writing 0 to the CSR6<1> and CSR6<13> fields, respectively. The driver must wait for any previously scheduled frame activity to cease. This is done by polling the transmit process state (CSR5<22:20>) and the receive process state (CSR5<19:17>).
2. In 10BASE-T/AUI mode, reset the SIA by writing 0 to CSR13<0>.
3. Set the CFDD<31> bit.

To exit sleep mode, the driver must take the following actions:

1. Clear CFDD<31>.
2. Wait 10 ms.
3. In 10BASE-T/AUI mode, start the SIA by writing 1 to CSR13<0>.
4. Wait at least 5 μs.
5. Start the receive and transmit processes by writing 1 to the CSR6<1> and CSR6<13> fields, respectively.

The 21143 powers up in sleep mode. Sleep mode must be exited before initialization of the 21143.

4.3.2.2 Snooze Power-Saving Mode

Snooze mode is a dynamic power-saving mode. When the snooze mode bit (CFDD<30>) is set, the 21143 reduces its power dissipation unless one or more of the following conditions is true:

- PCI slave or master access is conducted.
- Transmit process is in the running state.
- Receive process is in the running state but not waiting for a packet.
- Receive FIFO is not empty.
- MAC receive engine is not idle.
- Carrier is sensed.
- Link pass or link fail interrupt occurred.

When none of these conditions is true, the 21143 disables all its internal circuitries except for the PCI interface (not including the Manchester decoder that uses the 100-MHz phases). The 21143 automatically and immediately reenables all its circuitries when at least one of the following occurs:

- PCI slave access is conducted.
- Carrier is sensed.
- Link pass or link fail interrupt occurred.

This results in the 21143 dynamically getting into and out of low-power mode, and overall power dissipation is reduced.

Note: The general-purpose timer and the automatic poll demand functions cannot be used in snooze mode.

4.3.3 Arbitration Scheme

The arbitration scheme is used by the 21143 to grant precedence to the receive process instead of the transmit process (CSR0<1>). The technical expressions used in this table are described in the following list:

- *Txreq*—Specifies a DMA request for the transmit process to:
  - Fetch descriptor.
  - Close descriptor.
  - Process setup packet.
  - Transfer data from the host buffer to the transmit FIFO when there is sufficient space in the transmit FIFO for a full data burst.
- *Rxreq*—Specifies a DMA request for the receive process to:
  - Fetch descriptor.
  - Close descriptor.
  - Transfer data from the receive FIFO to the host buffer when the receive FIFO contains sufficient data for a full data burst or contains the end of the packet.
- *TxEN*—Specifies that the 21143 is currently transmitting.
- *RxF<thrx*—Specifies that the amount of free bytes left in the receive FIFO is less than an internal threshold.
- *TxF<thtx*—Specifies that the amount of bytes in the transmit FIFO is less than an internal threshold.

Table 4–12 lists a description of the arbitration scheme.

Table 4–12 Arbitration Scheme

Txreq	Rxreq	TxEN	RxF<thrx	TxF<thtx	Chosen Process
0	0	0	—	—	—
0	0	1	—	—	—
0	1	0	—	—	Receive process
0	1	1	—	—	Receive process
1	0	0	—	—	Transmit process
1	0	1	—	—	Transmit process
1	1	0	—	—	Receive process
1	1	1	0	0	Transmit process
1	1	1	0	1	Transmit process
1	1	1	1	0	Receive process
1	1	1	1	1	Transmit process[1]

[1]The transmit process choice is true only when working in half-duplex mode. When working in full-duplex mode, a round-robin arbitration scheme will be applied.

In addition to the arbitration scheme listed in Table 4–12, two other factors must be considered:

- The transmit process obtains a window for one burst between two consecutive receive packets.
- The receive process obtains a window for one burst between two consecutive transmit packets.

4.3.4 Interrupts

Interrupts can be generated as a result of various events. CSR5 contains all the status bits that might cause an interrupt. The following list contains the events that cause interrupts:

CSR5<0>—Transmit interrupt
CSR5<1>—Arbitration Scheme Transmit process stopped
CSR5<2>—Transmit buffer unavailable
CSR5<3>—Transmit jabber timeout
CSR5<4>—Link pass or autonegotiation completed interrupt
CSR5<5>—Transmit underflow
CSR5<6>—Receive interrupt
CSR5<7>—Receive buffer unavailable
CSR5<8>—Receive process stopped
CSR5<9>—Receive watchdog timeout
CSR5<10>—Early transmit interrupt
CSR5<11>—General-purpose timer expired
CSR5<12>—Link fail interrupt
CSR5<13>—Fatal bus error
CSR5<14>—Early receive interrupt
CSR5<26>—General-purpose port interrupt
CSR5<27>—Link-changed interrupt

Interrupt bits are cleared by writing a 1 to the bit position. This enables additional interrupts from the same source.

Interrupts are not queued, and if the interrupting event recurs *before* the driver has responded to it, no additional interrupts are generated. For example, receive interrupt (CSR5<6>) indicates that one or more received frames were delivered to host memory. The driver must scan *all* descriptors, from the last recorded position to the first one owned by the 21143.

An interrupt is generated only *once* for simultaneous, multiple interrupting events. The driver must scan CSR5 for the interrupt cause or causes. The interrupt is not generated *again*, unless a new interrupting event occurs after the driver has cleared the appropriate CSR5 bits.

For example, transmit interrupt (CSR5<0>) and receive interrupt (CSR5<6>) are set simultaneously. The host acknowledges the interrupt, and the driver begins executing by reading CSR5. Next, receive buffer unavailable (CSR5<7>) is set. The driver writes back its copy of CSR5, clearing transmit interrupt and receive interrupt. The interrupt line is deasserted for one cycle and then asserted again with receive buffer unavailable.

4.3.5 Startup Procedure

The following sequence of checks and commands must be performed by the driver to prepare the 21143 for operation:

1. Wait 50 PCI clock cycles for the 21143 to complete its reset sequence.
2. Update configuration registers (Section 3.1):
   a. Read the configuration ID and revision registers to identify the 21143 and its revision.
   b. Write the configuration interrupt register (if interrupt mapping is necessary).
   c. Write the configuration base address registers to map the 21143 I/O or memory address space into the appropriate processor address space.
   d. Write the configuration command register.
   e. Write the configuration latency counter to match the system latency guidelines.
3. Write CSR0 to set global host bus operating parameters (Section 3.2.2.1).
4. Write CSR7 to mask unnecessary (depending on the particular application) interrupt causes.
5. The driver must create the transmit and receive descriptor lists. Then, it writes to both CSR3 and CSR4, providing the 21143 with the starting address of each list (Section 3.2.2.4). The first descriptor on the transmit list may contain a setup frame (Section 4.2.3).

Caution: If address filtering (either perfect or imperfect) is desired, the receive process should only be started after the setup frame has been processed (Section 4.2.3).

6. When in either 10BASE-T or AUI mode, change the default settings of the jabber timers and also the initial SIA settings by writing to CSR13 (Section 3.2.2.13), CSR14 (Section 3.2.2.14), and CSR15 (Section 3.2.2.15).
7. Write CSR6 (Section 3.2.2.6) to set global serial parameters and to start both the receive and transmit processes. The receive and transmit processes enter the running state and attempt to acquire descriptors from the respective descriptor lists. Then the receive and transmit processes begin processing incoming and outgoing frames. The receive and transmit processes are independent of each other and can be started and stopped separately.

4.3.6 Receive Process

While in the running state, the receive process polls the receive descriptor list, attempting to acquire free descriptors. Incoming frames are processed and placed in acquired descriptors' data buffers. Status information is written to receive descriptor 0.

4.3.6.1 Descriptor Acquisition

The 21143 always attempts to acquire an extra descriptor in anticipation of incoming frames. Descriptor acquisition is attempted if any of the following conditions are satisfied:

- When start/stop receive (CSR6<1>) sets immediately after being placed in the running state.
- When the 21143 begins writing frame data to a data buffer pointed to by the current descriptor, and the buffer ends before the frame ends.
- When the 21143 completes the reception of a frame, and the current receive descriptor has been closed.
- When the receive process is suspended because of a host-owned buffer (RDES0<31>=0), and a new frame is received.
- When receive poll demand is issued (Section 3.2.2.3).

4.3.6.2 Frame Processing

As incoming frames arrive, the 21143 recovers the incoming data and clock pulses, and then sends them to the receive engine. The receive engine strips the preamble bits and stores the frame data in the receive FIFO. Concurrently, the receive section performs address filtering depending on the results of inverse filtering (CSR6<6>), hash/perfect receive filtering mode (CSR6<0>), and hash-only receive filtering mode (CSR6<2>), and also its internal filtering table. If the frame fails the address filtering, it is ignored and purged from the FIFO. Frames that are shorter than 64 bytes, because of collision or premature termination, are also ignored and purged from the FIFO (unless pass bad frames bit CSR6<3> is set).

After 64 bytes have been received, the 21143 requests the PCI bus to begin transferring the frame data to the buffer pointed to by the current descriptor. While waiting for the PCI bus, the 21143 continues to receive and store the data in the FIFO. After receiving the PCI bus, the 21143 sets first descriptor (RDES0<9>), to delimit the frame. Then, the descriptors are released when the OWN (RDES0<31>) bit is reset to 0, either as the data buffers fill up or as the last segment of a frame is transferred to a buffer. If a frame is contained in a single descriptor, both last descriptor (RDES0<8>) and first descriptor (RDES0<9>) are set.

The 21143 fetches the next descriptor, sets last descriptor (RDES0<8>), and releases the RDES0 status bits in the last frame descriptor. Then the 21143 sets receive interrupt (CSR5<6>). The same process repeats unless the 21143 encounters a descriptor flagged as being owned by the host. If this occurs, the receive process sets receive buffer unavailable (CSR5<7>) and then enters the suspended state. The position in the receive list is retained.

4.3.6.3 Receive Process Suspended

If a receive frame arrives while the receive process is suspended, the 21143 refetches the current descriptor in host memory. If the descriptor is now owned by the 21143, the receive process reenters the running state and starts the frame reception. If the descriptor is still owned by the host, the 21143 discards the current frame in the receive FIFO and increments the missed frames counter (CSR8<15:0>). If more than one frame is stored in the receive FIFO, the process repeats.

4.3.6.4 Receive Process State Transitions

Table 4–13 lists the receive process state transitions and the resulting actions.

Table 4–13 Receive Process State Transitions

From State	Event	To State	Action
Stopped	Start receive command.	Running	Receive polling begins from last list position or from the list head, if this is the first start receive command issued, or if the receive descriptor list address (CSR3) was modified by the driver.
Running	The 21143 attempts to acquire a descriptor owned by the host.	Suspended	Receive buffer unavailable (CSR5<7>) sets when the last acquired descriptor buffer is consumed. The position in the list is retained.
Running	Stop receive command.	Stopped	Receive process is stopped after the current frame, if any, is completely transferred to data buffers. Receive process stopped (CSR5<8>) sets. The position in the list is retained.
Running	Memory or host bus parity error encountered.	Running	The 21143 operation is stopped and fatal bus error (CSR5<13>) sets. The 21143 remains in the running state. A software reset must be issued to release the 21143.
Running	Reset command.	Stopped	Receive capability is cut off.
Suspended	Receive poll demand or incoming frame and available descriptor.	Running	Receive polling resumes from last list position.
Suspended	Stop receive command.	Stopped	Receive process stopped (CSR5<8>) sets.
Suspended	Reset command.	Stopped	None.

4.3.7 Transmit Process

While in the running state, the transmit process polls the transmit descriptor list for frames requiring transmission. After polling starts, it continues in either sequential descriptor ring order or chained order. When it completes frame transmission, status information is written into transmit descriptor 0 (TDES0). If the 21143 detects a descriptor flagged as owned by the host, or if an error condition occurs, the transmit process is suspended and both transmit buffer unavailable (CSR5<2>) and normal interrupt summary (CSR5<16>) are set.

Transmit interrupt (CSR5<0>) is set after completing transmission of a frame that has interrupt on completion (TDES1<31>) set in its last descriptor. When this occurs, the transmission process continues to run.

While in the running state, the transmit process can simultaneously acquire two frames. As the transmit process completes copying the first frame, it immediately polls the transmit descriptor list for the second frame. If the second frame is valid, the transmit process copies the frame before writing the status information of the first frame.

4.3.7.1 Frame Processing

Frames can be data-chained and span several buffers. Frames must be delimited by the first descriptor (TDES1<29>) and the last descriptor (TDES1<30>), respectively.

As the transmit process starts execution, the first descriptor must have TDES1<29> set. When this occurs, frame data transfers from the host buffer to the internal FIFO. Concurrently, if the current frame has the last descriptor TDES1<30> clear, the transmit process attempts to acquire the next descriptor. The transmit process expects this descriptor to have TDES1<29> clear. If TDES1<30> is clear, it indicates an intermediary buffer. If TDES1<30> is set, it indicates the last buffer of the frame.

After the last buffer of the frame has been transmitted, the 21143 writes back the final status information to the transmit descriptor 0 (TDES0) word of the descriptor that has the last segment set in transmit descriptor 1 TDES1<30>). At this time, if interrupt on completion (TDES1<31>) was set, the transmit interrupt (CSR5<0>) is set, the next descriptor is fetched, and the process repeats.

Actual frame transmission begins after the internal FIFO has reached either a programmable threshold CSR6<15:14> (Table 3–43), or a full frame is contained in the FIFO. There is also an option for store and forward mode CSR6<21>, (Table 3–42). Descriptors are released (OWN bit TDES0<31> clears) when the 21143 completes the packet transmission.

4.3.7.2 Transmit Polling Suspended

Transmit polling can be suspended by either of the following conditions:

- The 21143 detects a descriptor owned by the host (TDES0<31>=0). To resume, the driver must give descriptor ownership to the 21143 and then issue a poll demand command.
- A frame transmission is aborted when a locally induced error is detected. The appropriate transmit descriptor 0 (TDES0) bit is set.

If either of the previous two conditions occur, both abnormal interrupt summary (CSR5<15>) and transmit interrupt (CSR5<0>) are set, and the information is written to transmit descriptor 0, causing the suspension.

In both of the cases previously described, the position in the transmit list is retained. The retained position is that of the *descriptor following the last descriptor closed* (set to host ownership) by the 21143.

Note: The 21143 *does not* automatically poll the transmit descriptor list. The driver *must* explicitly issue a transmit poll demand command after rectifying the suspension cause, unless the transmit automatic polling (CSR0<19:17>) field is nonzero. In case of suspension as a result of underflow, the 21143 does not automatically poll the descriptors list even if CSR0<19:17> is nonzero.

4.3.7.3 Transmit Process State Transitions

Table 4–14 lists the transmit process state transitions and the resulting actions.

Table 4–14 Transmit Process State Transitions *(Sheet 1 of 2)*

From State	Event	To State	Action
Stopped	Start transmit command.	Running	Transmit polling begins from one of the following positions: • The last list position. • The head of the list, if this is the first start command issued after CSR4 was initialized or modified.
Running	The 21143 attempts acquisition of a descriptor owned by the host.	Suspended	Transmit buffer unavailable. (CSR5<2>) is set.
Running	Frame transmission aborts because a locally induced underflow error (TDES0<1>) is detected (Section 4.2.2.1).	Suspended	The following bits are set: TDES0<1>—Underflow error CSR5<5>—Transmit underflow CSR5<15>—Abnormal interrupt summary
Running	Stop transmit command.	Stopped	Transmit process is topped after the current frame, if any, is transmitted.
Running	Frame transmission aborts because a transmit jabber timeout (TDES0<14>) was detected (Section 4.2.2.1).	Stopped	The following bits are set: TDES0<14>— Transmit jabber time out CSR5<1>—Transmit process stopped CSR5<3>—Transmit jabber time out CSR5<15>—Abnormal interrupt summary
Running	Parity error detected by memory or host bus.	Running	Transmission is cut off and fatal bus error (CSR5<13>) is set. The 21143 remains in the running state. If a software reset occurs, normal operation continues.

Table 4–14 Transmit Process State Transitions *(Sheet 2 of 2)*

From State	Event	To State	Action
Running	Reset command.	Stopped	Transmission is cut off. If CSR4 was not changed, the position in the list is retained. If CSR4 was changed, the next descriptor address is fetched from the header list (CSR4) when the poll demand command is issued. Transmit process stopped (CSR5<1>) is set.
Suspended	Transmit poll demand command issued.	Running	Transmit polling resumes from the last list position.
Suspended	Stop transmit command.	Stopped	Transmit process stopped (CSR5<1>) is set.
Suspended	Reset command.	Stopped	None.

5
Host Bus Operation

This chapter describes the commands and operations of read and write cycles for a bus slave and a bus master. It also explains the initiation of termination cycles by the bus master or bus slave.

5.1 Overview

The peripheral component interconnect (PCI) is the physical interconnection used between highly integrated peripheral controller components and the host system. The 21143 uses the PCI bus to communicate with the host CPU and memory.

The 21143 is directly compatible with revision 2.0 and revision 2.1 of the *PCI Local Bus Specification*. The 21143 supports a subset of the PCI-bus cycles (transactions). When communicating with the host, the 21143 operates as a bus slave; when communicating with the memory, as a bus master.

All signals are sampled on the rising edge of the clock. Each signal has a setup and hold aperture with respect to the rising clock edge. Refer to the *Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Data Sheet* for detailed timing information. Table 5–1 lists the codes for bus commands.

Note: The term **clock cycle**, as used in this chapter, refers to the PCI bus clock period specification.

5.2 Bus Commands

Table 5–1 lists the bus commands.

Table 5–1 Bus Commands

c_be_l<3:0>	Command	Type of Support
0000	Interrupt acknowledge	Not supported
0001	Special cycle	Not supported
0010	I/O read	Supported as target
0011	I/O write	Supported as target
0100	Reserved	—
0101	Reserved	—
0110	Memory read	Supported as master and target
0111	Memory write	Supported as master and target
1000	Reserved	—
1001	Reserved	—
1010	Configuration read	Supported as target
1011	Configuration write	Supported as target
1100	Memory read multiple	Supported as master and target[1]
1101	Dual-address cycle	Not supported
1110	Memory read line	Supported as master and target
1111	Memory write and invalidate	Supported as master and target

[1]Master support for this command is controlled by (CSR0<21>.

5.3 Bus Slave Operation

All host accesses to CSRs and configuration registers in the 21143 are executed with the 21143 acting as the slave. The bus slave can perform the following operations:

- I/O read
- I/O write
- Configuration read

- Configuration write
- Memory read
- Memory write

Other bus slave operations include memory write and invalidate, memory read line, and memory read multiple.

Note: The 21143 does not support the following bus transactions:

Interrupt acknowledge
Special cycle
Dual-address cycle

If the 21143 is targeted for a burst I/O or memory operation, it responds with a retry on the second data transaction.

5.3.1 Slave Read Cycle (I/O or Memory Target)

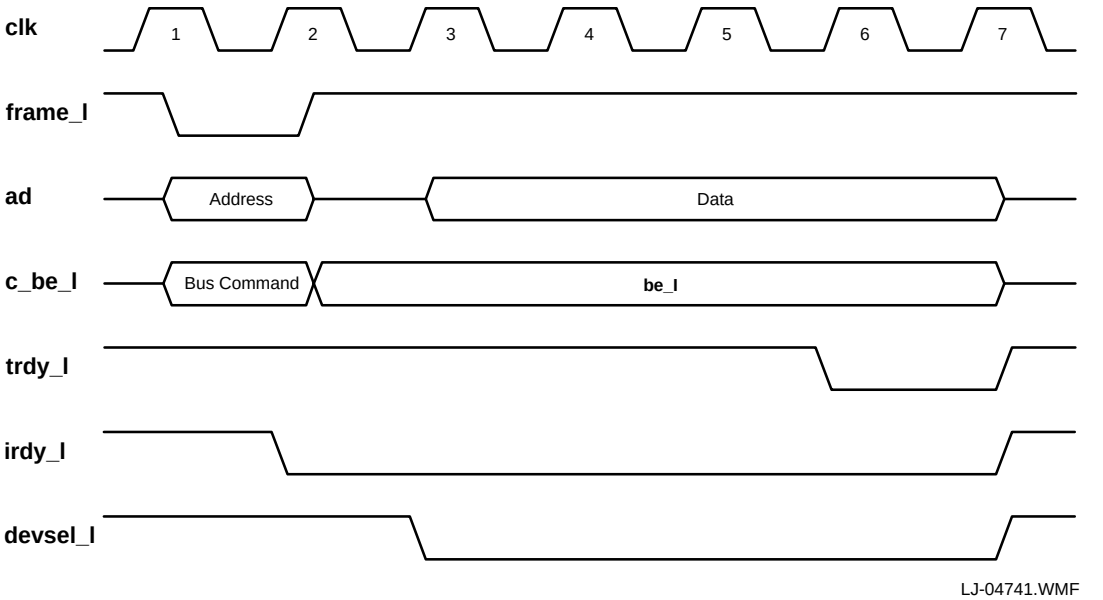
Figure 5–1 shows a typical slave read cycle. The 21143 I/O read cycle is executed as follows:

1. The host initiates the slave read cycle by asserting the **frame_l** signal, driving the address on the **ad** lines and driving the bus command (slave read operation) on the **c_be_l** lines.
2. The 21143 samples the address and the bus command on the next clock edge.
3. The host deasserts **frame_l** signal and asserts **irdy_l** signal.
4. The 21143 asserts **devsel_l**, and, at the next cycle, drives the data on the **ad** lines.
5. The read transaction completes when both **irdy_l** and **trdy_l** are asserted by the host and the 21143, respectively, on the same clock edge.

   The 21143 assumes that **c_be_l** lines are 0000 (longword access).

   If the **c_be_l** lines are 1111, the **ad** bus read is 00000000H with correct parity.
6. The host and the 21143 terminates the cycle by deasserting **irdy_l** and **trdy_l**, respectively.

Figure 5–1 Slave Read Cycle



5.3.2 Slave Write Cycle (I/O or Memory Target)

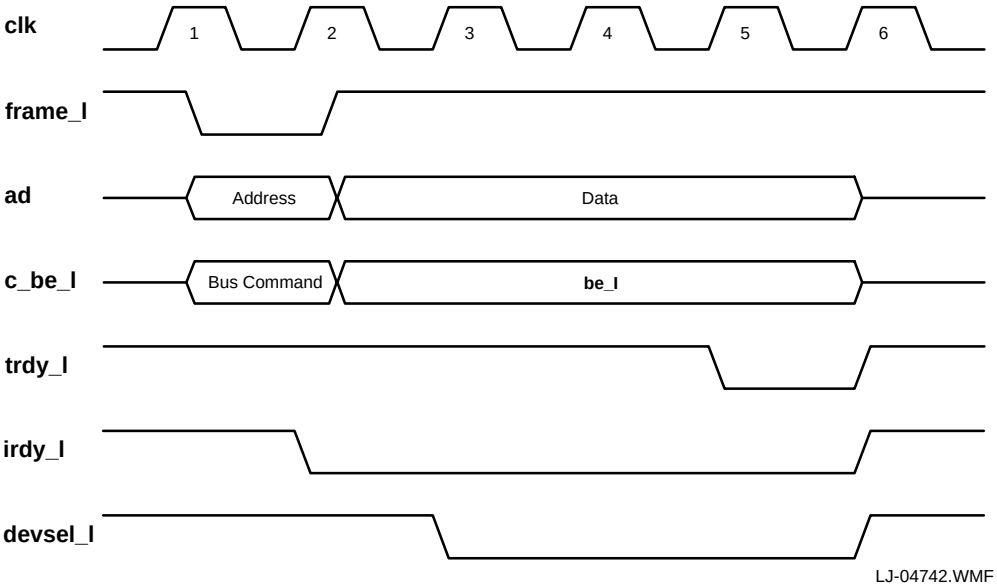
Figure 5–2 shows a typical slave write cycle. The 21143 slave write cycle is executed as follows:

1. The host initiates the slave write cycle by asserting the **frame_l** signal, driving both the address on the **ad** lines and the bus command (slave write operation) on the **c_be_l** lines.
2. The 21143 samples the address and the bus command on the next clock edge.
3. The host deasserts **frame_l** and drives the data on the **ad** lines along with **irdy_l**.
4. The 21143 samples the data, and also asserts both **devsel_l** and **trdy_l**.
5. The host and the 21143 complete the write transaction by asserting both **irdy_l** and **trdy_l**, respectively, on the same clock edge.

   The 21143 assumes that **c_be_l** lines are 0000 (longword access).

   If the **c_be_l** lines are 1111, the write transaction completes normally on the bus, but the write transaction to the CSR is not executed.
6. The host and the 21143 terminate the cycle by deasserting **irdy_l** and **trdy_l**, respectively.

Figure 5–2 Slave Write Cycle



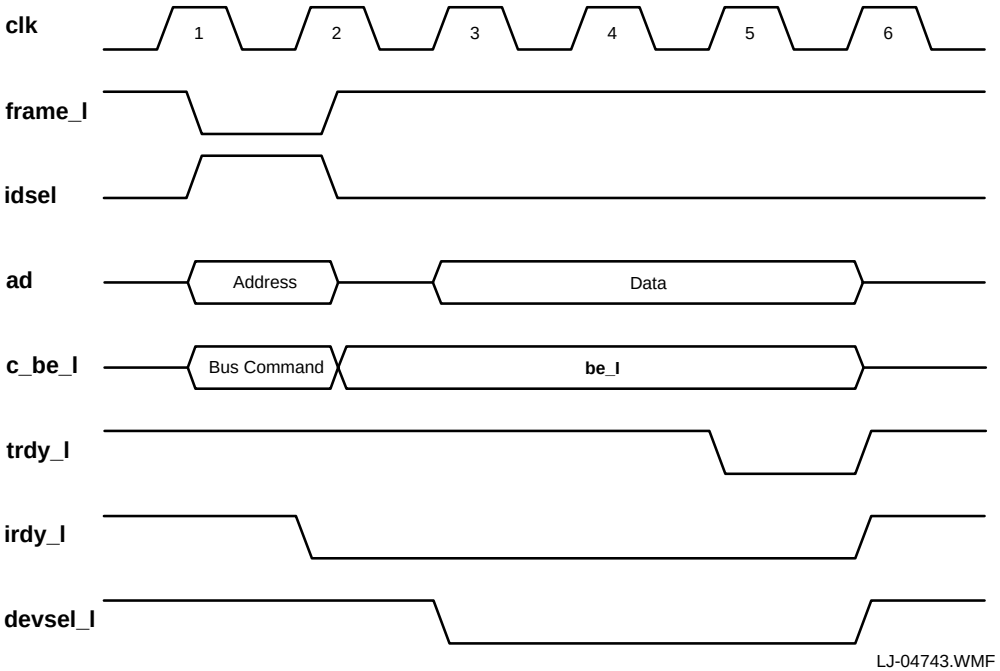
5.3.3 Configuration Read and Write Cycles

The 21143 provides a way for software to analyze and configure the system before defining any address assignments or mapping. The 21143 provides 256 bytes of configuration registers. Section 3.1 describes these registers.

Note: Configuration space accesses provide support for **c_be_l** lines.

Figure 5–3 shows a configuration read cycle. The host selects the 21143 by asserting **idsel**. The 21143 responds by asserting **devsel_l**. The remainder of the read cycle is similar to the slave read cycle (Section 5.3.1).

Figure 5–3 Configuration Read Cycle



5.4 Bus Master Operation

All memory accesses are completed with the 21143 as the master on the PCI bus. The bus master can perform the following operations:

- Bus arbitration
- Memory read cycle
- Memory write cycle
- Termination cycles

5.4.1 Bus Arbitration

The 21143 uses the PCI central arbitration mechanism with its unique request (**req_l**) and grant (**gnt_l**) signals. Figure 5–4 shows the bus arbitration mechanism. The 21143 bus arbitration is executed as follows:

1. The 21143 requests the bus by asserting **req_l**.
2. The arbiter, in response, asserts **gnt_l** (**gnt_l** can be deasserted on any clock).
3. The 21143 ensures that its **gnt_l** is asserted on the clock edge that it wants to drive **frame_l**. (If **gnt_l** is deasserted, the 21143 does not proceed.)
4. The 21143 deasserts **req_l** on the cycle that it asserts **frame_l**.

Figure 5–4 Bus Arbitration

The 21143 uses **gnt_l** according to the following rules:

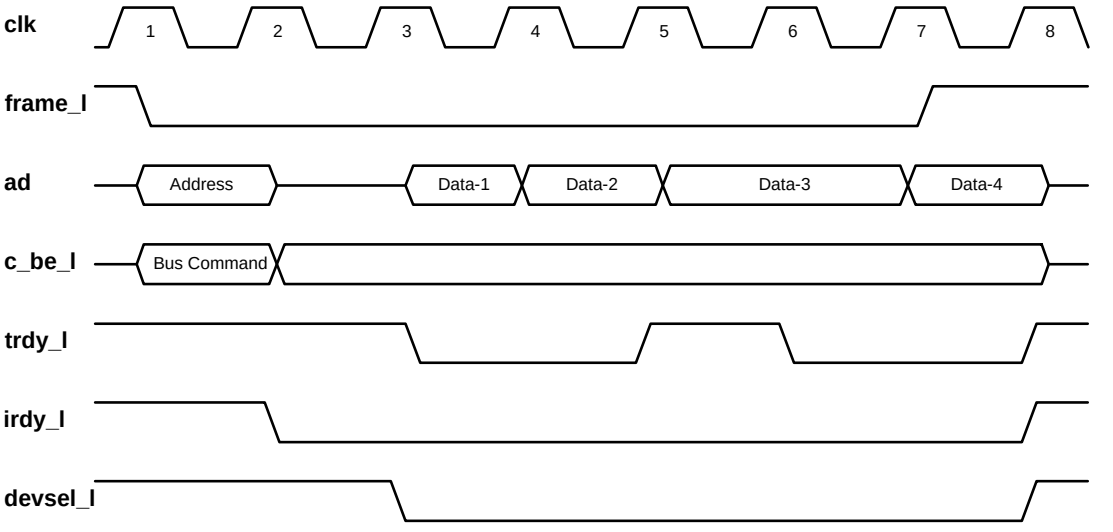
- If **gnt_l** is deasserted together with the assertion of **frame_l**, the 21143 continues its bus transaction.
- If **gnt_l** is asserted while **frame_l** remains deasserted, the arbiter can deassert **gnt_l** at any time. The 21143 does not assert **frame_l** until it is granted again.

5.4.2 Memory Read Cycle

Figure 5–5 shows the memory read cycle. The memory read cycle is executed as follows:

1. The 21143 initiates the memory read cycle by asserting **frame_l** signal. It also drives the address on the **ad** lines and the appropriate bus command (read operation) on the **c_be_l** lines.
2. The memory controller samples the address and the bus command on the next clock edge.
3. The 21143 asserts **irdy_l** until the end of the read transaction.
4. During the data transfer cycles, **c_be_l** indicates which byte lines are involved in each cycle. The 21143 drives 0000 on the **c_be_l** lines (longword access).
5. The memory controller drives the data on the **ad** lines and asserts **trdy_l**.
6. The 21143 samples the data on each rising clock edge when both **irdy_l** and **trdy_l** are asserted.
7. The previous two steps can be repeated a number of times.
8. The cycle is terminated when **frame_l** is deasserted by the 21143.
9. Signal **irdy_l** is deasserted by the 21143 and **trdy_l** is deasserted by the memory controller.

Figure 5–5 Memory Read Cycle



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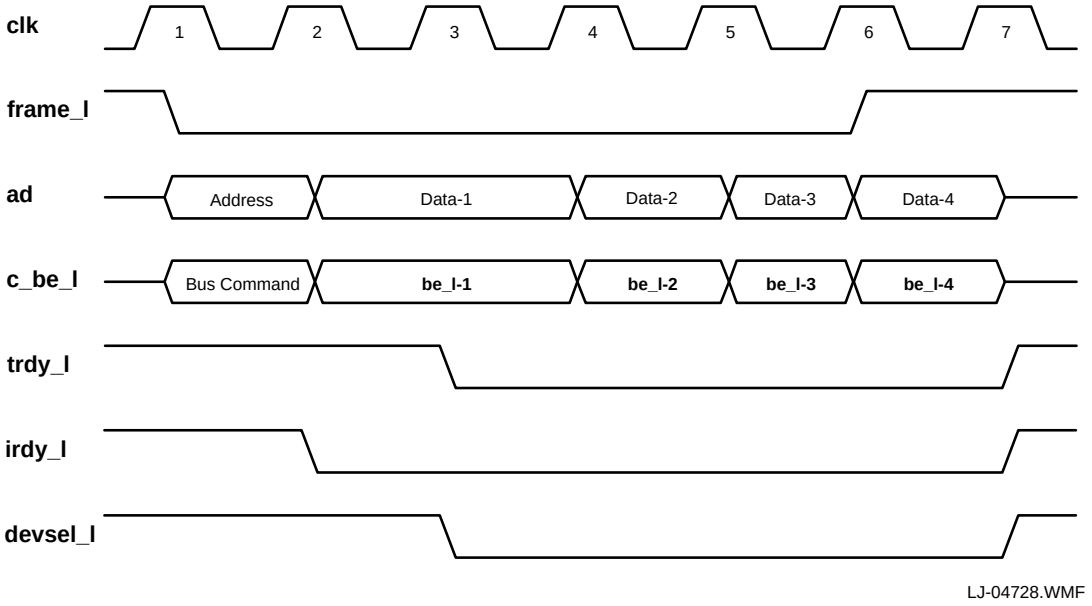
5.4.3 Memory Write Cycle

Figure 5–6 shows the memory write cycle. The memory write cycle is executed as follows:

1. The 21143 initiates the memory write cycle by asserting **frame_l**. It also drives both the address on the **ad** lines and the write operation bus command on the **c_be_l** lines.
2. The 21143 asserts **irdy_l** until the end of the transaction and drives the data on the **ad** lines.
3. The memory controller samples the address and the bus command on the next clock edge and asserts **devsel_l**.
4. During the data transfer cycles, the **c_be_l** lines indicate which byte lines are involved in each cycle. The 21143 drives 0000 on the **c_be_l** lines (longword access).
5. The memory controller samples the data and asserts **trdy_l**. Each data cycle is completed on the rising clock edge when both **irdy_l** and **trdy_l** are asserted.
6. The previous two steps can be repeated a number of times.

7. The 21143 terminates the cycle by deasserting **frame_l**.
8. The 21143 deasserts **irdy_l** and the memory controller deasserts **trdy_l**.

Figure 5–6 Memory Write Cycle



5.5 Termination Cycles

Termination cycles can be initiated during either slave or master cycles.

5.5.1 Slave-Initiated Termination

A slave-initiated termination can occur when the 21143 operates as a slave device on the PCI bus. A slave can initiated the following types of terminations:

Disconnect

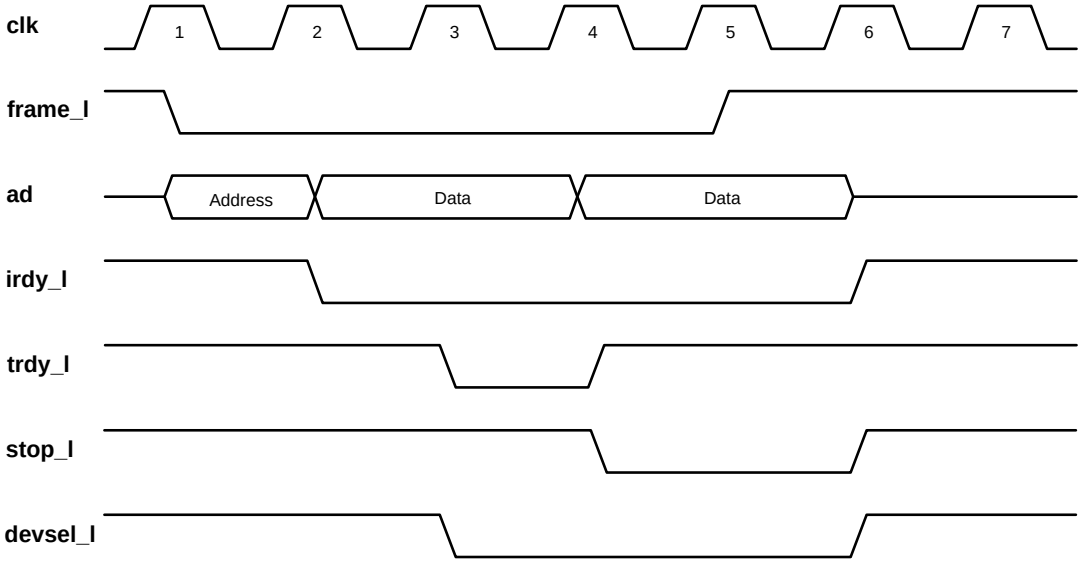
Retry

5.5.1.1 Disconnect Termination

The 21143 initiates disconnect termination in slave mode when it is accessed by the host with I/O or memory burst cycles. The 21143 asserts **stop_l** to request the host to terminate the transaction. After **stop_l** is asserted, it remains asserted until **frame_l** is deasserted.

Figure 5–7 shows the disconnected device (the host) releasing the bus. The host retries the last data transaction after acquiring the bus in a different arbitration.

Figure 5–7 21143-Initiated Disconnect Cycle



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5.5.1.2 Retry Termination

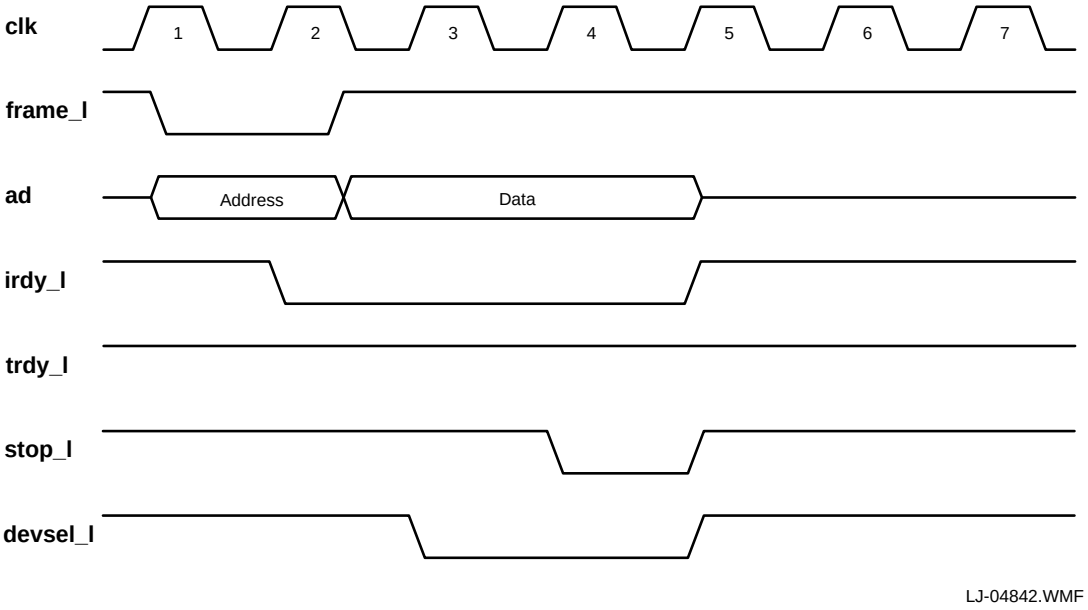
The 21143 initiates retry termination in slave mode when one of the following transactions occur:

- The 21143 registers CSR9 and CSR10 are accessed by the host, while the 21143 is still handling either a previous boot ROM or serial ROM access.
- The 21143 configuration registers CSID and CCIS are accessed by the host, before their contents are loaded from the serial ROM.

The 21143 does not assert **trdy_l** in response to these host accesses. It asserts **stop_l** requesting that the host terminate the transaction. Signal **stop_l** remains asserted until **irdy_l** is deasserted.

Figure 5–8 shows the retried device (the host) releasing the bus. The host retries the last data transaction after acquiring the bus in a different arbitration.

Figure 5–8 21143-Initiated Retry Cycle



5.5.2 Master-Initiated Termination

A master-initiated termination can occur when the 21143 operates as a master device on the PCI bus. Terminations can be issued by either the 21143 or the memory controller.

The 21143 can perform the following terminations:

Normal completion

Timeout

Master abort

The memory-controller can perform the following terminations (target):

Target abort

Target disconnect

Target retry

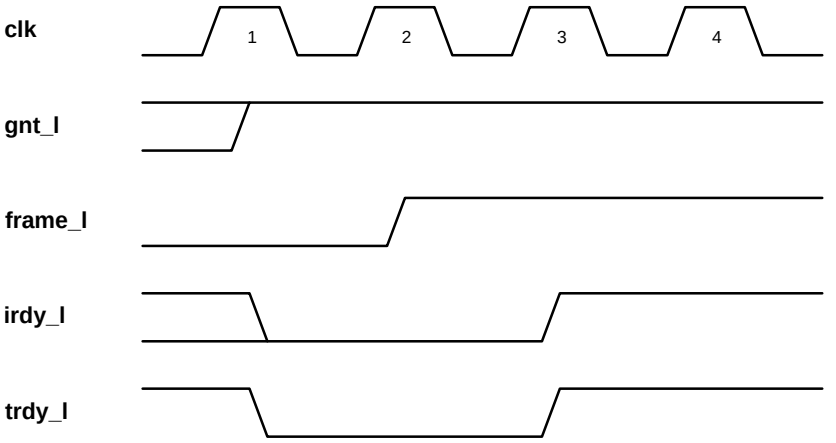
5.5.2.1 21143-Initiated Termination

A 21143-initiated termination occurs when **frame_l** is deasserted and **irdy_l** is asserted. This indicates to the memory controller that the final data phase is in progress. The final data transfer occurs when both **irdy_l** and **trdy_l** assert. The transaction completes when both **frame_l** and **irdy_l** deassert. This is an idle bus condition.

Normal Completion

Figure 5–9 shows a normal completion cycle termination. This indicates that the 21143 successfully completed its intended transaction.

Figure 5–9 Normal Completion



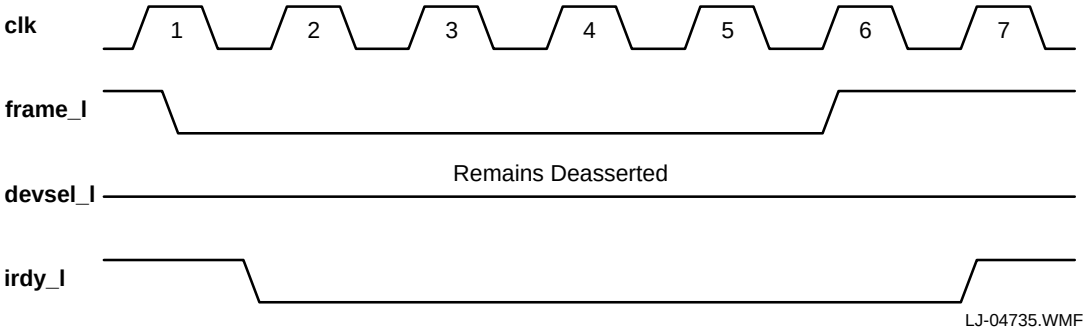
Timeout

A timeout cycle termination occurs when the **gnt_l** line has been deasserted by the arbiter and the 21143 internal latency timer has expired. However, the intended transaction has not completed. A maximum of two additional data phases are permitted and then the 21143 performs a normal transaction completion.

Master Abort

If the target does not assert **devsel_l** within five cycles from the assertion of **frame_l**, the 21143 performs a normal completion. It then releases the bus and asserts both master abort (CFCS<29>) and fatal bus error (CSR5<13>). Figure 5–10 shows the 21143 master abort termination.

Figure 5–10 Master Abort



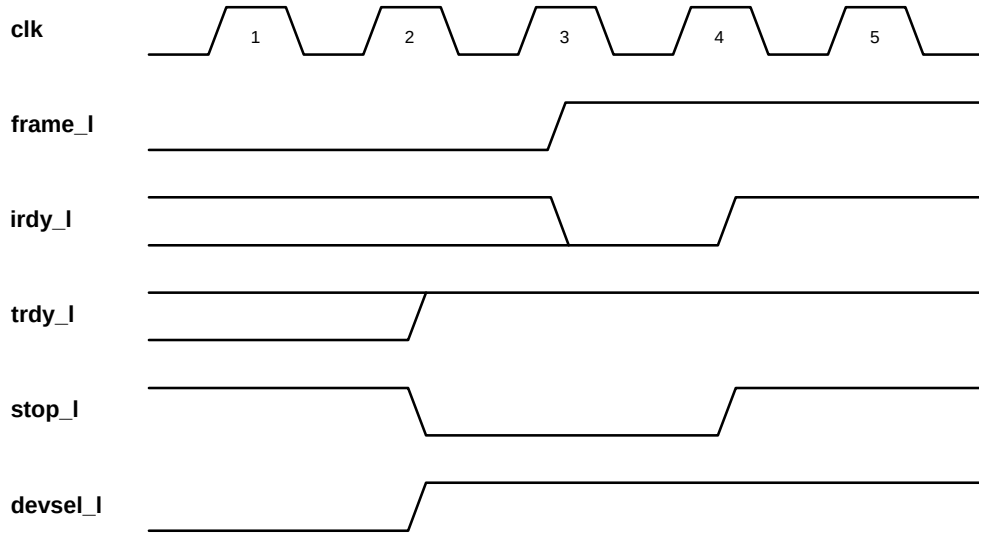
5.5.2.2 Memory-Controller-Initiated Termination

The memory controller or target can initiate certain terminations when the 21143 is the bus master.

Target Abort

The 21143 aborts the bus transaction when the target asserts **stop_l** and deasserts **devsel_l**. This indicates that the target wants the transaction to be aborted. The 21143 releases the bus and asserts both received target abort (CFCS<28>) and fatal bus error (CSR5<15>). Figure 5–11 shows the 21143 target abort.

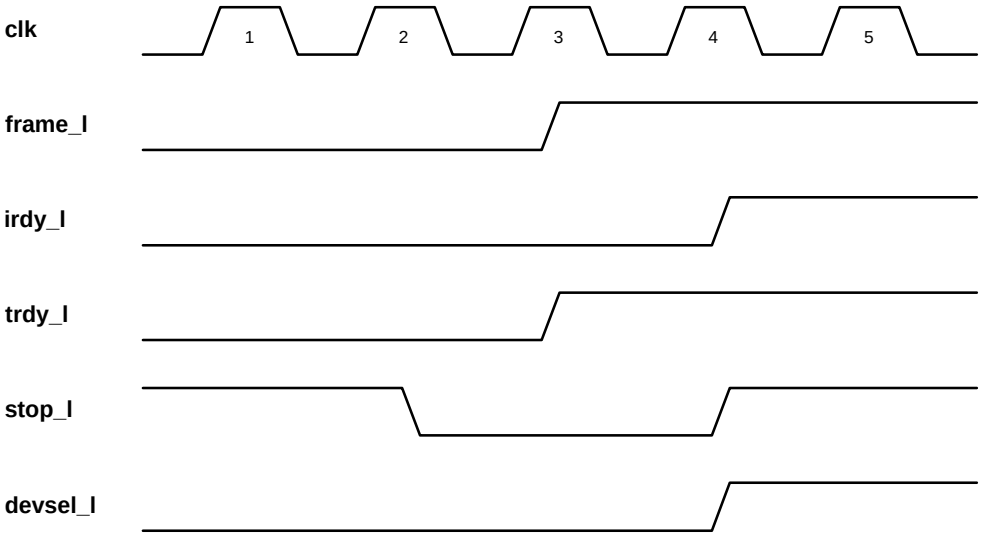
Figure 5–11 Target Abort



Target Disconnect Termination

The 21143 terminates the bus transaction when the target asserts **stop_l**, which remains asserted until **frame_l** is deasserted. The 21143 releases the bus. Then, it retries at least the last data transaction after regaining the bus in another arbitration. Figure 5–12 shows the 21143 target disconnect.

Figure 5–12 Target Disconnect



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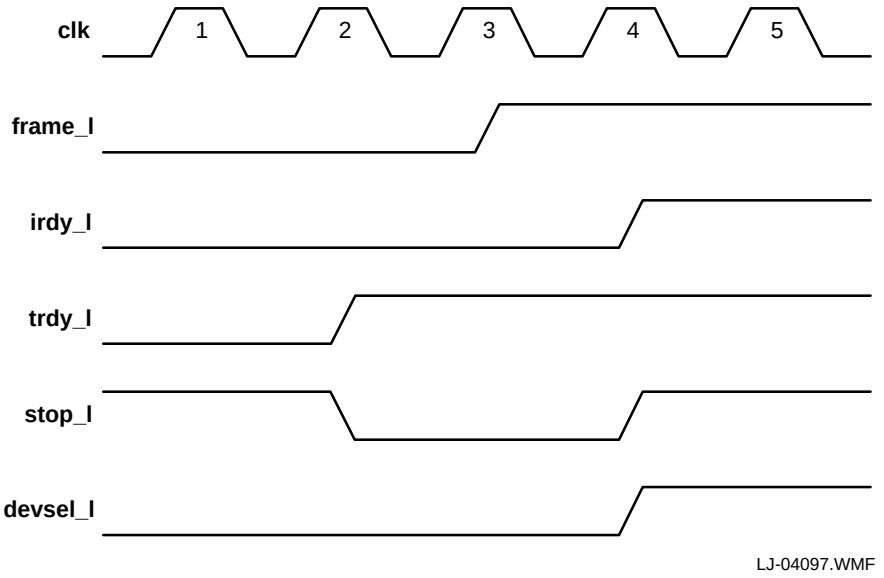
Target Retry

The 21143 retries the bus transaction when the target asserts **stop_l** and deasserts **trdy_l**; **stop_l** remains asserted until **frame_l** is deasserted. The 21143 releases the bus. Then, it retries at least the last two data transactions after regaining the bus in another arbitration. Figure 5–13 shows the 21143 target retry.

Figure 5–13 Target Retry

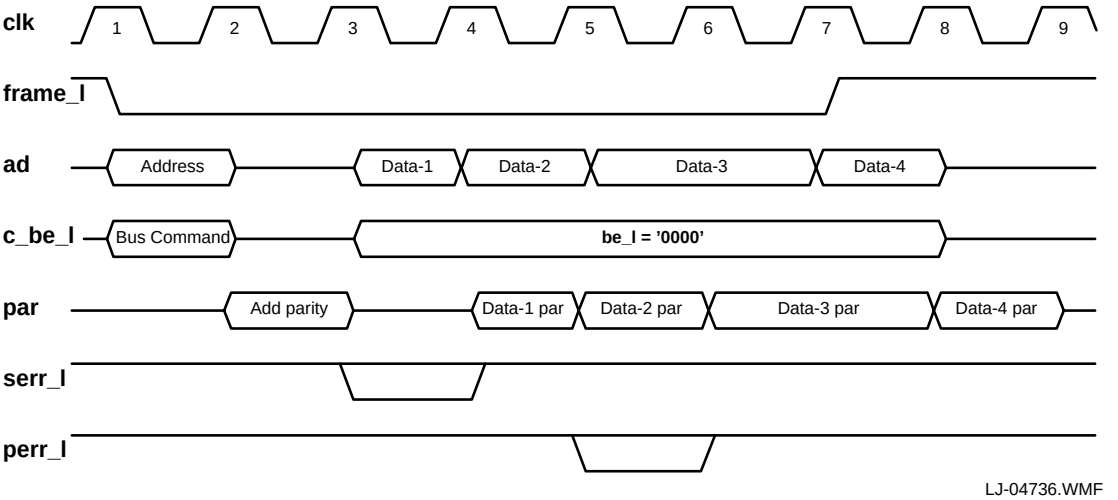


5.6 Parity

The 21143 supports parity generation on all address, data, and command bits. Parity is always checked and generated on the 32-bit address and data bus (**ad**) as well as on the four command (**c_be_l**) lines. The 21143 always transfers stable values (1 or 0) on all the **ad** and **c_be_l** lines. If a data parity error is detected or **perr_l** is asserted when the 21143 is a bus master, the 21143 asserts data parity report (CFCS<24>) and fatal bus error (CSR5<13>).

Figure 5–14 shows an example of parity generation on a memory write burst transaction. Note that valid parity is generated one cycle after the address and data segments were generated on the bus. One cycle after the assertion of the address parity, **serr_l** is asserted for one cycle because of an address parity error during slave operation. One cycle after the assertion of the data parity, **perr_l** is asserted because of a parity data error in either slave write or master read operations.

Figure 5–14 Parity Operation



5.7 Parking

Parking in the PCI bus allows the central arbiter to pause any selected agent. The 21143 enters the parking state when the arbiter asserts its **gnt_l** line while the bus is idle.

6
Network Interface Operation

This chapter describes the operation of the MII/SYM port, the 10BASE-T port, and the AUI port. It also describes media access control (MAC), loopback, and full-duplex operations. Appendix D describes the port selection procedure.

6.1 MII/SYM Port

This section provides a description of the 100BASE-T terminology, the interface, the signals used, and the operating modes.

6.1.1 100BASE-T Terminology

This subsection provides a description of the 100BASE-T terminology used for the MII/SYM port. A list of these terms follows:

- Media-independent interface (MII) is defined between the media access control (MAC) sublayer and the physical layer protocol (PHY) layer.
- Physical coding sublayer (PCS) is a sublayer within the PHY defined by 100BASE-T. The PCS implements the higher level functions of the PHY.
- 100BASE-T is a generic term that refers to all members in the IEEE 802.3 family of 100-Mb/s carrier-sense multiple access with collision detection (CSMA/CD) standards.
- 100BASE-T4 is the standard IEEE 802.3 for 100 Mb/s, using unshielded twisted-pair (UTP) category 3 (CAT3) cables. The PHY requires four pairs.
- 100BASE-X refers to all members of the IEEE 802.3 family contained in the 100-Mb/s CSMA/CD standard. It implements a specific physical medium attachment (PMA) and PCS. Members of this family include 100BASE-TX and 100BASE-FX.

- 100BASE-TX refers to the IEEE 802.3 PHY layer, which includes the 100BASE-X PCS and PMA together with the physical layer medium dependent (PMD). It uses UTP category 5 (CAT5) cables and STP cables.
- 100BASE-FX refers to the IEEE 802.3 PHY layer, which includes the 100BASE-X PCS and PMA together with the PMD. It uses multimode fiber.

6.1.2 Interface Description

The MII port is an IEEE 802.3 compliant interface that provides a simple, inexpensive, and easily implemented interconnection between the MAC sublayer and the PHY layer. It also interconnects the PHY layer devices and station management (STA) entities. This interface has the following characteristics:

- Supports both 100-Mb/s and 10-Mb/s data rates
- Contains data and delimiters that are synchronous to clock references
- Provides independent, 4-bit-wide transmit and receive data paths
- Uses TTL signal levels, compatible with common CMOS application-specific integrated circuit (ASIC) processes
- Provides a simple management interface

6.1.2.1 Signal Standards

Table 6–1 provides the standards that reference the MII/SYM port signal names with the appropriate IEEE 802.3 signal names.

Table 6–1 IEEE 802.3 and MII/SYM Signals *(Sheet 1 of 2)*

MII/SYM Signals	IEEE 802.3 Signals	Purpose
mii_clsn	COL	Collision detect is asserted by the PHY layer when it detects a collision on the medium. It remains asserted while this condition persists. For the 10-Mb/s implementation, collision is derived from the signal quality error of the PMA. For the 100-Mb/s implementation, collision is defined for each PHY layer separately.
mii_crs	CRS	Carrier sense is asserted by the PHY layer when either the transmit or receive medium is active (not idle).

Table 6–1 IEEE 802.3 and MII/SYM Signals *(Sheet 2 of 2)*

MII/SYM Signals	IEEE 802.3 Signals	Purpose
mii_dv	RX_DV	Receive data valid is asserted by the PHY layer when the first received preamble nibble is driven over the MII/SYM and remains asserted for the remainder of the frame.
mii_rx_err	RX_ERR	Receive error is asserted by the PHY layer to indicate either a coding error or any other type of error that the MAC cannot detect was received. This error was detected on the frame currently being received and transferred over the MII/SYM.
mii_mdc	MDC	Management data clock is the clock reference for the **mii_mdio** signal.
mii_mdio	MDIO	Management data input/output is used to transfer control signals between the 21143 and the PHY chip. The 21143 is capable of initiating the transfer of control signals to and from the PHY device by using this line.
mii/sym_rclk	RX_CLK	Receive clock synchronizes all receive signals.
mii/sym_rxd<3:0>	RXD<3:0>	These lines provide receive data.
mii/sym_tclk	TX_CLK	Transmit clock synchronizes all transmit signals.
mii/sym_txd<3:0>	TXD<3:0>	These lines provide transmit data.
mii_txen	TX_EN	Transmit enable is asserted by the MAC sublayer when the first transmit preamble nibble is driven over the MII/SYM and remains asserted for the remainder of the frame.
Note:	The remaining three signals are activated when the MII/SYM port uses either the 100BASE-TX or 100BASE-FX applications.	
mii_sd	—	Signal detect indication is supplied by an external PMD device.
sym_rxd<4>	—	This line is used for receive data.
sym_txd<4>	—	This line is used for transmit data.

6.1.2.2 Operating Modes

The 21143 implements the MII/SYM port signals (Table 6–1) to support the following operating modes:

- **MII 100-Mb/s mode**—The 21143 implements the MII with a data rate of 100 Mb/s and both the receive clock (**mii/sym_rclk)** and the transmit clock **(mii/sym_tclk**) operate at 25 MHz. In this mode, the 21143 can be used with any device that implements the 100BASE-T PHY layer (for example, 100BASE-TX, 100BASE-FX, or 100BASE-T4) and an MII.
- **MII 10-Mb/s mode**—The 21143 implements the MII with a data rate of 10 Mb/s and both the receive clock **mii/sym_rclk** and the transmit clock **mii/sym_tclk** operate at 2.5 MHz. In this mode, the 21143 can be used with any device that implements the 10-Mb/s PHY layer and an MII.
- **100BASE-TX mode**—The 21143 implements certain functions of the PCS for STP PMD and UTP CAT5 PMD. The receive symbols are 5 bits wide and are transferred over the **mii/sym_rxd<3:0>** and **sym_rxd<4>** lines. The transmit symbols are also 5 bits wide and are transferred over the **mii/sym_txd<3:0>** and **sym_txd<4>** lines. The 21143 implements the following functions:
  - 4-bit and 5-bit decoding and encoding
  - Start-of-stream delimiter (SSD) and end-of-stream delimiter (ESD) detection and generation
  - Bit alignment
  - Carrier detect
  - Collision detect
  - Symbol error detection
  - Scrambling and descrambling
  - Link timer

  This mode enables a direct interface with existing fiber distributed data interface (FDDI) TP-PMD devices that implement the physical functions.
- **100BASE-FX mode**—The 21143 implements certain functions of the PCS sublayer for multimode fiber. The receive symbols are 5 bits wide and are transferred over the **mii/sym_rxd<3:0>** and **sym_rxd<4>** lines. The transmit symbols are also 5 bits wide and are transferred over the **mii/sym_txd<3:0>** and **sym_txd<4>** lines. The 21143 implements the following functions:

- 4-bit and 5-bit decoding and encoding
- SSD and ESD detection and generation
- Bit alignment
- Carrier detect
- Collision detect
- Symbol error detection
- Link timer

This mode enables a direct interface with existing FDDI TP-PMD devices that implement the physical functions.

Note: The SSD detection logic compares the incoming data to JK and not to IJK (this complies with IEEE 802.3, draft number 2).

6.2 10BASE-T and AUI Functions

The 10BASE-T and AUI protocols include the following functions:

- Supports data driver and is receiver compatible with 10BASE-T specifications
- Supports data driver and is receiver compatible with AUI specifications
- Provides AUI collision receiver compatible with AUI specifications
- Selects either AUI or 10BASE-T interfaces
- Implements Manchester decoder for incoming data
- Implements Manchester encoder for outgoing data
- Contains onchip, 20-MHz crystal oscillator circuitry
- Enables watchdog timers on incoming and outgoing data
- Contains 10BASE-T enhanced features that include:
  - Smart squelch, rejecting noise detected by the 10BASE-T receiver interface
  - Combined autopolarity and link test detection, presenting a robust algorithm for detection of both wire failure and switching of wires. Polarity correction is automatically done, while wire failure is reported to higher layers.

6.2.1 Receivers and Drivers

The host selects one set of data receivers and drivers at a time: either AUI or Twisted-Pair (TP). The other receiver and driver sets are enabled too, unless CSR14<15> (10BASE-T/AUI autosensing enable) is reset.

6.2.2 Manchester Decoder

The Manchester decoder is a phase-locked loop decoder that provides received clocks and data to the media access control (MAC) interface (Section 6.3).

6.2.3 Manchester Encoder

The Manchester encoder receives clocked data from the transmit engine and uses the 20-MHz clock to provide Manchester encoded data. The encoder provides the transition to idle for the AUI and TP drivers.

6.2.4 Oscillator Circuitry

The 21143 supports two options for generating the internal 10-MHz clock required by the internal circuitry.

1. An external parallel resonant crystal connected between **xtal1** and **xtal2** to drive the 21143-integrated oscillator circuitry.
2. An external clock generator module connected to **xtal1**; **xtal2** remains unconnected.

In both cases, the 21143 must be provided with a 20-MHz signal that is internally divided by 2 to generate the 10-MHz clock.

When driving the oscillator from an external clock source, an external clock having the following characteristics must be used to ensure proper operation of the 21143:

- Clock frequency: 20-MHz ±0.01% (100 ppm, TTL, or CMOS)
- Rise/fall time: < 4 ns
- Duty cycle: 40%–60%

Table 6-2 lists the specifications for the crystal oscillator.

Table 6–2 Crystal Oscillator Specification

Category	Value
Frequency	20 MHz
Tolerance	±0.01% at 25°C (100 ppm)
Stability	±0.005% at 0°C to 70°C (100 ppm)

6.2.5 Smart Squelch

The 21143 implements an intelligent squelch on its TP receiver to ensure that impulse noise detected on the receive inputs is not mistaken for valid signals. The squelch circuitry employs a combination of both amplitude and timing measurements to determine the validity of data received on the TP inputs.

The squelch circuit allows only valid differential receive data to pass through to the Manchester decoder provided that the following two conditions are satisfied:

1. The input amplitude is greater than the minimum signal threshold level.
2. A specific pulse sequence is received.

Satisfying these two conditions ensures that a good signal-to-noise ratio is maintained while the signal pair is active, and it prevents system noise from causing false squelch deactivation.

The line squelch quickly activates and deactivates within the specified time intervals, when the input squelch threshold is exceeded and a specific pulse sequence of proper polarity is detected.

The squelch circuitry rejects system noise by ignoring received pulses that are less than the required fixed time width. It also rejects pulses that are greater than the expected signal duration.

6.2.6 Autopolarity Detector

The autopolarity detector (CSR14<13>) provides a method of detecting receive wire polarity by switching the polarity of the data going into the MAC layer accordingly. To detect polarity, the 21143 uses the link test pulse and the end-of-frame delimiter in an algorithm integrated into the link integrity test, as specified in the IEEE 802.3 10BASE-T supplement.

6.2.7 Network Port Autosensing

The 21143 can sense the AUI and 10BASE-T ports at the same time. In addition, while the AUI port is used for transmission, it can also send the 10BASE-T link pulses onto the TP wires. These features, along with reported status bits and interrupts, together with indications taken from the 100BASE-T PHY chip located on the board, allow the driver to choose between the three ports for network connection without any network configuration information.

To implement the autosensing algorithm, the driver can use the following hardware support provided by the 21143 (a detailed description of these bits is provided in Chapter 3):

- Interrupts
  - Link pass CSR5<4>
  - Link fail CSR5<12>
  - Timer expired CSR5<11>
- CSRs
  - Autosensing enable bit CSR14<15>
  - Activity sensed on the AUI port CSR12<8>
  - Activity sensed on the 10BASE-T port CSR12<9>
  - Activity sensed on the MII port CSR12<10>
  - General-purpose timer (CSR11)

Additional information about the MII port activity can be taken from the 100BASE-T PHY chip located on the board through the MII management port (**mii_mdc** and **mii_mdio)**.

Selecting one of the serial ports requires programming of CSR6, CSR13, CSR14, and CSR15. Table 3–68 provides the programming values for autosensing enabling. To change the selection, start by resetting the SIA using CSR13.

6.2.8 10BASE-T Link Integrity Test

Before transmitting on an Ethernet CSMA/CD network, each device has to check the reliability of its receive lines. For the AUI connection, this is indicated by the carrier signal present during transmission. In the twisted-pair (TP) case, link pulses are sent every 8 ms to 24 ms at the interval between two transmissions.

The 21143 monitors the received link pulses and end-of-frame delimiters to be spaced and electrically shaped as specified in the IEEE 802.3 10BASE-T supplement. Accordingly, the 21143 implements the Link Integrity Test.

After a software or hardware reset, the 21143 wakes up in the link fail state. In this state, only link pulses are sent onto the transmit lines. Upon detection of the required line activity, and autonegotiation completion (if enabled), the 21143 enters the link pass state enabling the receive and transmit paths.

A broken or noisy wire can bring the 21143 back to the link fail state. It will then report the wire failure by generating a link fail interrupt to the host and will immediately stop the receive and transmit paths. These paths will not be enabled again until the Link Integrity Test ends successfully.

6.3 Media Access Control Operation

The 21143 supports a full implementation of the MAC sublayer of IEEE 802.3. It can operate in half-duplex mode, full-duplex mode, and loopback mode.

6.3.1 MAC Frame Format

The 21143 handles both IEEE 802.3 and Ethernet MAC frames. While operating in either the 100BASE-FX mode or 100BASE-TX mode, the 21143 encapsulates the frames it transmits according to the IEEE 802.3, clause 24. Receive frames are encapsulated according to the IEEE 802.3, clause 24.

The changes between a MAC frame (Section 6.3.1.1) and the encapsulation used when operating either in 100BASE-TX or 100BASE-FX mode are listed as follows:

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.
2. After the frame check sequence (FCS) byte of the MAC frame, the TR symbol pair is inserted.

6.3.1.1 Ethernet and IEEE 802.3 Frames

Ethernet is the generic name for the network type. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes, exclusive of the preamble and the start frame delimiter.

An Ethernet frame format consists of the following parts:

Preamble
Start frame delimiter (SFD)
Two address fields
Type or length field
Data field
Frame check sequence (CRC value)

6.3.1.2 Ethernet Frame Format Description

Figure 6–1 shows the Ethernet frame format.

Figure 6–1 Ethernet Frame Format

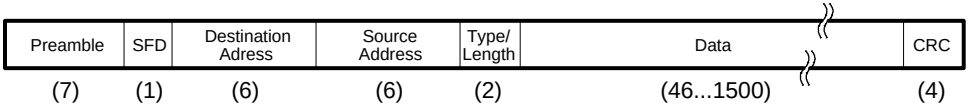


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Table 6–3 describes the Ethernet frame format.

Table 6–3 Ethernet Frame Format *(Sheet 1 of 2)*

Field	Description
Preamble	A 7-byte field of 56 alternating 1s and 0s, beginning with a 0.
SFD—Start frame delimiter	A 1-byte field that contains the value 10101011; the most significant bit is transmitted and received first.
Destination address	A 6-byte field that contains either a specific station address, the broadcast address, or a multicast (logical) address where this frame is directed.
Source address	A 6-byte field that contains the specific station address where this frame originated.

Table 6–3 Ethernet Frame Format *(Sheet 2 of 2)*

Field	Description
Type/length	A 2-byte field that indicates whether the frame is in IEEE 802.3 format or Ethernet format (Table 6–4). A field greater than 1500 is interpreted as a type field, which defines the type of protocol of the frame. A field smaller than or equal to 1500 (05-DC) is interpreted as a length field, which indicates the number of data bytes in the frame.
Data	A data field consists of 46 bytes to 1500 bytes of information that is fully transparent because any arbitrary sequence of bits can occur. A data field shorter than 46 bytes, which is specified by the length field, is allowed. Unless padding is disabled (TDES1<23>), it is added by the 21143 when transmitting to fill the data field up to 46 bytes.
CRC	A frame check sequence is a 32-bit cyclic redundancy check (CRC) value that is computed as a function of the destination address field, source address field, type field, and data field. The FCS is appended to each transmitted frame, and is used at reception to determine if the received frame is valid.

Table 6–4 lists the possible values for the frame format. The values are expressed in hexadecimal notation and the 2-byte field is displayed with a hyphen separating the 2 bytes. The byte on the left of the hyphen is the most significant byte and is transmitted first.

Table 6–4 Frame Format Table

Frame Format	Length or Type	Hexadecimal Value
IEEE 802.3	Length field	00-00 to 05-DC
Ethernet	Type field	05-DD to FF-FF

The CRC polynomial, as specified in the Ethernet specification, is as follows:

$$FCS(X) = X^{31} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} +$$
$$X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

The 32 bits of the CRC value are placed in the FCS field so that the X^{31} term is the right-most bit of the first octet, and the X^{0} term is the left-most bit of the last octet. The bits of the CRC are thus transmitted in the order X^{31}, X^{30}, ... , X^{1}, X^{0}.

6.3.2 Ethernet Reception Addressing

The 21143 can be set up to recognize any one of the Ethernet receive address groups described in Table 6–5. Each group is separate and distinct from the other groups.

Table 6–5 Ethernet Receive Address Groups *(Sheet 1 of 2)*

Group	Description
1	16-address perfect filtering The 21143 provides support for the perfect filtering of up to 16 Ethernet physical or multicast addresses. Any mix of addresses can be used for this perfect filter function of the 21143. The 16 addresses are issued in setup frames to the 21143.
2	One physical address, unlimited multicast addresses imperfect filtering The 21143 provides support for one, single physical address to be perfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered. This case supports the needs of applications that require one, single physical address to be filtered as the station address, while enabling reception of more than 16 multicast addresses, without suffering the overhead of pass-all-multicast mode. The single physical address, for perfect filtering, and a 512-bit mask, for imperfect filtering using a hash algorithm, are issued in a setup frame to the 21143. When hash hits are detected, the 21143 delivers the received frame (Section 4.2.3)
3	Unlimited physical addresses, unlimited multicast addresses imperfect filtering The 21143 provides support for unlimited physical addresses to be imperfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered as well. This case supports applications that require more than one physical address to be filtered as the station address, while enabling the reception of more than 16 multicast addresses, without suffering the overhead of pass-all-multicast mode. A 512-bit mask, for imperfect filtering using a hash algorithm, is issued in a setup frame to the 21143. When hash hits are detected, the 21143 delivers the received frame (Section 4.2.3).
4	Promiscuous Ethernet reception The 21143 provides support for reception of all frames on the network regardless of their destination. This function is controlled by a CSR bit. This group is typically used for network monitoring.

Table 6–5 Ethernet Receive Address Groups *(Sheet 2 of 2)*

Group	Description
5	16-address perfect filtering and reception of all multicast Ethernet addresses This group augments the receive address Group 1 and also receives all frames on the Ethernet with a multicast address.
6	16-address inverse filtering In this mode, the 21143 applies the reverse filter of Group 1. The 21143 provides support for the rejection of up to 16 Ethernet physical or multicast addresses. Any mix of addresses may be used for this filter function of the 21143. The 16 addresses are issued in setup frames to the 21143.

6.3.3 Detailed Transmit Operation

This section describes the transmit operation in detail, as supported by the 21143. This description includes the specific control register definitions, setup frame definitions, and a mechanism used by the host processor software to manipulate the transmit list (that is, the descriptors and buffers that can be found in Section 4.2).

6.3.3.1 Transmit Initiation

The host CPU initiates a transmit by storing the entire information content of the frame to be transmitted in one or more buffers in memory. The host processor software prepares a companion transmit descriptor, also in host memory, for the transmit buffer and signals the 21143 to take it. After the 21143 has been notified of this transmit list, the 21143 starts to move the data bytes from the host memory to the internal transmit FIFO.

When the transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the 21143 begins to encapsulate the frame.

The threshold level can be programmed with various quantities (Table 3–43). The lower threshold is for low bus latency systems and the high threshold is for high bus latency systems.

The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission of the data onto the network until the network has been idle for a minimum interpacket gap (IPG) time.

6.3.3.2 Frame Encapsulation

The transmit data frame encapsulation stream consists of appending the 56 preamble bits together with the SFD to the basic frame beginning and the FCS (for example, CRC), to the basic frame end.

The basic frame read from the host memory includes the destination address field, the source address field, the type/length field, and the data field. If the data field length is less than 46 bytes, and padding (TDES1<23>) is enabled, the 21143 pads the basic frame with the pattern 00 for up to 46 bytes before appending the FCS field to the end.

While operating either in 100BASE-FX mode or 100BASE-TX mode, the 21143 encapsulates the frames it transmits according to IEEE 802.3, clause 24 and the receive frame is encapsulated as defined in IEEE 802.3, clause 24.

The changes between a MAC frame (Section 6.3.1) and the encapsulation used when operating either in 100BASE-TX or 100BASE-FX modes are listed as follows:

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.
2. After the FCS byte of the MAC frame, the TR symbol pair is inserted.

6.3.3.3 Initial Deferral

The 21143 constantly monitors the line and can initiate a transmission any time the host CPU requests it. Actual transmission of the data onto the network occurs only if the network has been idle for a 96-bit time period, and any backoff time requirements have been satisfied.

The IPG time is divided into two parts: IPS1 and IPS2.

1. IPS1 time (60-bit time): the 21143 monitors the network for an idle state. If a carrier is sensed on the serial line during this time, the 21143 defers and waits until the line is idle again before restarting the IPS1 time count.
2. IPS2 time (36-bit time): the 21143 continues to count time even though a carrier has been sensed on the network, and thus forces collisions on the network. This enables all network stations to have access to the serial line.

6.3.3.4 Collision

A collision occurs when concurrent transmissions from two or more Ethernet nodes take place. When the 21143 detects a collision while transmitting, it halts the transmission of the data, and instead, transmits a jam pattern consisting of hexadecimal AAAAAAAA. At the end of the jam transmission, the 21143 begins the backoff wait period.

If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (if the 21143 is in 100BASE-FX or 100BASE-TX operating modes, this includes the JK symbol pair as described in Section 6.3.4.2.2). This action results in a minimum 96-bit fragment.

The 21143 scheduling of retransmission is determined by a controlled randomization process called truncated binary exponential backoff. The delay is an integer multiple of slot times. The number of slot times of delay before the *n*th retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$$0 \le r < 2^k$$

$$k = \min (n, N) \text{ and } N = 10$$

When 16 attempts have been made at transmission and all have been terminated by a collision, the 21143 sets an error status bit in the descriptor (TDES0<8>) and, if enabled, issues a normal transmit termination (CSR5<0>) interrupt to the host.

Note: The jam pattern is a fixed pattern that is not compared with the actual frame CRC. This has the very low probability (0.5^{32}) of having a jam pattern equal to the CRC.

6.3.3.5 Terminating Transmission

A specific frame transmission is terminated by any of the following conditions:

- Normal—The frame has been transmitted successfully. When the last byte is serialized, the pad and CRC are optionally appended and transmitted, thus concluding frame transmission.
- Underflow—Transmit data is not ready when needed for transmission. The underflow status bits (TDES0<1> and CSR5<5>) are set, and the packet is terminated on the network with a bad CRC.
- Excessive collisions—If a collision occurs for the 15th consecutive retransmission attempt of the same frame, TDES0<8> is set.

- Jabber timer expired—If the timer expires (TDES0<14> sets) while transmission continues, the programmed interval transmission is cut off.
- Memory error—This generic error indicates either a host bus timeout or a host memory error.
- Late collision—If a collision occurs after the collision window (transmitting at least 64 bytes), transmission is cut off and TDES0<9> sets.

At the completion of every frame transmission, status information about the frame is written into the transmit descriptor. Status information is written into CSR5 if an error occurs during the operation of the transmit machine itself. If a normal interrupt summary (CSR7<16>) is enabled, the 21143 issues a normal transmit termination interrupt (CSR5<0>) to the host.

6.3.3.6 Transmit Parameter Values

Table 6–6 lists the transmit parameter values for both the 10-Mb/s and 100-Mb/s serial bit rates.

Table 6–6 Transmit Parameter Values

Parameter	Condition	Value
Defer time	IPS1+IPS2=96-bit time period	—
IPS1	—	60-bit time period
IPS2	—	36-bit time period
Slot time interval	—	512-bit time period
Network acquisition time	—	512-bit time period
Transmission attempts	—	16
Backoff limit	—	10
Jabber timer	Default	16,000-bit to 20,000-bit time period
Jabber timer	Programmable range	26,000-bit to 32,000-bit time period

6.3.4 Detailed Receive Operation

This section describes the detailed receive operation as supported by the 21143. This description includes the specific control register definitions, setup frame definitions, and a mechanism used by the host processor software to manipulate the receive list (that is, the descriptors and buffers that can be found in Section 4.2).

6.3.4.1 Receive Initiation

The 21143 continuously monitors the network when reception is enabled. When activity is recognized, it starts to process the incoming data. After detecting receive activity on the line, the 21143 starts to process the preamble bytes based on the mode of operation.

6.3.4.2 Preamble Processing

Preamble processing varies depending on the 21143 operating mode. The next two subsections describe how this processing is handled.

6.3.4.2.1 MII/SYM, 10BASE-T, or AUI Mode Preambles

In MII/SYM, 10BASE-T, or AUI mode, the preamble, as defined by Ethernet, can be up to 64 bits (8 bytes) long.

The 21143 allows any arbitrary preamble length. However, depending on the mode, there is a minimum preamble length.

- In MII/SYM mode, at least 8 bits are required to recognize a preamble.
- In 10BASE-T or AUI mode, at least 16 bits are required to recognize a preamble.
- While in snooze mode, at least 20 bits are required to recognize a preamble. This is true for MII/SYM, 10BASE-T, and AUI modes.

Recognition occurs as follows:

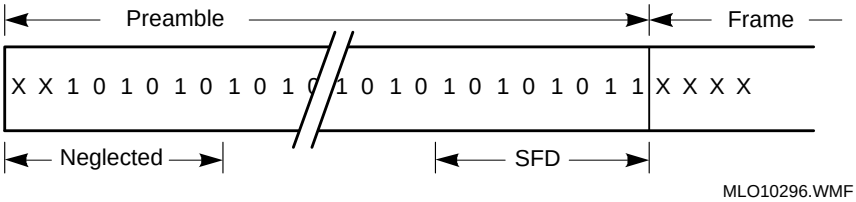
- In MII/SYM mode, the 21143 checks for the start frame delimiter (SFD) byte content of 10101011.
- In 10BASE-T or AUI mode:

  1. The first 8 preamble bits are ignored.
  2. The 21143 checks for the start frame delimiter (SFD) byte content of 10101011.

While checking for SFD, if the 21143 receives an 11_2 (before receiving 14 bits in 10BASE-T or AUI mode or 6 bits in MII/SYM mode) or a 00_2 (everywhere), the reception of the current frame is aborted. The frame is not received, and the 21143 waits until the network activity stops (Section 6.3.4.1) before monitoring the network activity for a new preamble.

Figure 6–2 shows the preamble recognition sequence bit fields.

Figure 6–2 Preamble Recognition Sequence in 10BASE-T or AUI Mode



6.3.4.2.2 100BASE-TX or 100BASE-FX Mode Preambles

When operating in either 100BASE-TX or 100BASE-FX mode, the 21143 expects the frame to start with the symbol pair JK followed by the preamble, as specified in Section 6.3.4.2.1. If a JK symbol pair is not detected, the reception of the current frame is aborted (not received), and the 21143 waits until the network activity stops before monitoring the network activity for a new preamble.

6.3.4.3 Address Matching

Ethernet addresses consist of two 6-byte fields: one field for the destination address and one for the source address. The first bit of the destination address signifies whether it is a physical address or a multicast address as listed in Table 6–7.

Table 6–7 Destination Address Bit 1

Bit 1	Address
0	Station address (physical)
1	Multicast address

The 21143 filters the frame based on the Ethernet receive address group filtering mode that has been enabled (Section 6.3.2).

If the frame address passes the filter, the 21143 removes the preamble and delivers the frame to the host processor memory. If, however, the address does not pass the filter when the mismatch is recognized, the 21143 terminates its reception. In this case, no data is sent to the host memory nor is any receive buffer consumed.

If receive all (CSR6<30>) is set, the 21143 receives all incoming packets, regardless of the destination address. The address recognition status is posted in RDES0<30>.

6.3.4.4 Frame Decapsulation

The 21143 checks the CRC bytes of all received frames before releasing them to the host processor. When operating in either 100BASE-TX or 100BASE-FX mode, the 21143 also checks that the frame ends with the TR symbol pair; if not, the 21143 reports a CRC error in the packet reception status.

6.3.4.5 Terminating Reception

Reception of a specific frame is terminated when any of the following conditions occur:

- Normal termination—The network activity (Section 6.3.4.1) stops for the various operating modes.
- Overflow—The receive DMA cannot empty the receive FIFO into host processor memory as rapidly as it is filled, and an error occurs as frame data is lost. The overflow status bit (RDES0<0>) is set.
- Watchdog timer expired —If the timer expires (CSR5<9> and RDES0<4> both set) while reception is still in process.
- Collision—If a late collision occurs after the reception of 64 bytes of the packet, the collision seen status bit RDES0<6> is set.

6.3.4.6 Frame Reception Status

When reception terminates, the 21143 determines the status of the received frame and loads it into the receive status word in the buffer descriptor. An interrupt is issued if enabled. The 21143 may report the following conditions at the end of frame reception:

- Overflow—The 21143 receive FIFO overflowed.
- CRC error—The 32-bit CRC transmitted with the frame did not match the CRC calculated upon reception. The CRC check is always executed and is independent of any other errors. In addition, the 21143 reports a CRC error in any of the following cases:
  - The **mii_err** signal asserts during frame reception over the MII when operating in one of the MII operating modes.
  - The 21143 is operating in either the 100BASE-TX or 100BASE-FX mode and one of the following events occur:
    * An invalid symbol is received in the middle of the frame.
    * The frame does not end with the symbol T followed by the symbol R.
- Dribbling bits error—This indicates the frame did not end on a byte boundary. The 21143 signals a dribbling bits error only if the number of dribbling bits in the last byte is 4 in MII operating mode, or at least 3 in 10BASE-T/AUI serial operating mode. Only *whole bytes* are run through the CRC check. This means that although up to 7 dribbling bits may have occurred and a framing error was signaled, the frame might nevertheless have been received correctly.
- Alignment error—A CRC error and a dribbling bit error occur together. This means that the frame did not contain an integral number of bytes and the CRC check failed.
- Frame too short (runt frame)—A frame containing less than 64 bytes was received (including CRC). Reception of runt frames is optionally selectable. The 21143 defaults to inhibit reception of runts.
- Frame too long—A frame containing more than 1500 bytes was received. Reception of frames too long completes with an error indication.

- Collision seen—A frame collision occurred after the 64 bytes following the start frame delimiter (SFD) were received. Reception of such frames is completed and an error bit is set in the descriptor.
- Descriptor error—An error was found in one of the receive descriptors, which disabled the correct reception of an incoming frame.

6.4 Loopback Operations

The 21143 supports two loopback modes: internal loopback and external loopback. Both internal and external loopback require external clock activity (**mii_tclk** in MII mode and **xtal1** in 10BASE-T or AUI mode).

6.4.1 Internal Loopback Mode

Internal loopback mode is normally used to verify that the internal logic operations function correctly. Internal loopback mode is enabled according to CSR6<11:10>. Internal loopback mode includes all the internal functions. In loopback mode, the 21143 disengages from the Ethernet wire.

Internal loopback mode also supports the following modes of operation:

1. Media access control (MAC) internal loopback mode in which transmit packets are looped back at the MAC level and the 21143 disengages the SIA. The loopback data rate is 10 Mb/s, or 10/100 Mb/s in MII/SYM mode.
2. 10BASE-T internal loopback mode in which transmit packets from the encoder output are selected and looped back to the decoder input. The loopback data rate is 10 Mb/s.

6.4.2 External Loopback Mode

External loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In external loopback mode, the 21143 takes frames from the transmit list and transmits them on the Ethernet wire. Concurrently, the 21143 listens to the line that carries its own transmissions and places incoming frames in the receive list.

Caution: In external loopback mode, when transmitted frames are placed on the Ethernet wire, the 21143 does not check the origin of any incoming frames. It is possible for frames not originating from the 21143 to enter the receive buffers.

External loopback mode also supports the following modes of operation:

- 10BASE-T external loopback mode transmits packets using twisted-pair wires. Concurrently, the 21143 disables the internal collision detector and thus listens to the line that carries its own transmission.
  The board designer must use an external shunt to connect the transmit line with the receive line.
- AUI external loopback mode transmits packets using the AUI cable up-to-MAU (medium attachment unit) to check the MAU integrity.
- MII/SYM external loopback mode transmits packets using the MII/SYM interface to check the MII/SYM integrity.

6.4.3 Driver Entering Loopback Mode

To enter a specific loopback mode, the driver must take the following actions:

Note: All address filtering and validity checking rules apply in all loopback modes.

1. Stop the receive and transmit processes by writing 0 to both the start/stop receive (CSR6<1>) and the start/stop transmit (CSR6<13>) fields. The driver must wait for any previously scheduled frame activity to cease by polling the transmit process state (<22:20>) and the receive process state (<19:17>) fields in CSR5.

2. Prepare the appropriate transmit and receive descriptor lists in host memory. These lists can follow the existing lists at the point of suspension or be new lists identified to the 21143 by the receive list base address in CSR3 and by the transmit list address in CSR4.
3. Stop the SIA by setting CSR13 to a value of 00000000H.
4. In 10BASE-T/AUI mode, program CSR13, CSR14, and CSR15 to the desired SIA operation mode according to Table 3–68.
5. Wait at least 5 μs.
6. Select the desired loopback mode according to Table 3–68.
7. Use start commands to place both the transmit and receive processes into the running state.
8. As in normal processing, execute any 21143 interrupts.

6.4.4 Driver Restoring Normal Operation

To restore normal operation, the driver must execute the following procedure:

1. Stop both the receive and transmit processes. The driver must wait for any previously scheduled frame activity to cease by polling both the transmit (CSR5<22:20>) and receive process state (CSR5<19:17>) fields in CSR5.
2. Prepare appropriate transmit and receive descriptor lists in host memory. These lists can either follow the existing lists at the point of suspension or be new lists that have to be identified to the 21143 by the receive list base address in CSR3 and the transmit list base address in CSR4.
3. Stop the SIA by setting CSR13 to a value of 00000000H.
4. In 10BASE-T/AUI mode, program CSR13, CSR14, and CSR15 to the desired SIA operation mode according to Table 3–68.
5. Wait at least 5 μs.
6. Select normal mode operation according to Table 3–68.
7. Use start commands to place both the transmit and receive processes into the running state.
8. Resume normal processing. Execute any 21143 interrupts.

6.5 Full-Duplex Operation

The 21143 activates the transmit and receive processes simultaneously. It also supports receive back-to-back packets with an interpacket gap (IPG) of 96-bit times in parallel with transmit back-to-back packets with an IPG of 96-bit times.

The 21143 implements a programmable full-duplex operating mode (CSR6<9>) bit that commands the MAC to ignore both the carrier and the collision detect signal. In 10BASE-T mode, when the autonegotiation algorithm is used (CSR14<7>), the 21143 operates in full-duplex mode only if the negotiation results allow it. For additional information about programming full-duplex operation with autonegotiation, refer to Section 6.6.

The driver must take the following actions to enter full-duplex operation.

1. Stop the receive and transmit processes by writing 0 to CSR6<1> and CSR6<13> fields, respectively. The driver must wait for any previously scheduled frame activity to cease by polling the transmit process state (<22:20>) and receive process state (<19:17>) fields in CSR5.
2. Reset the SIA by writing 0 to CSR13.
3. Prepare appropriate transmit and receive descriptor lists in host memory. These lists can use the existing lists at the point of suspension, or can create new lists that must be identified to the 21143 by referencing the receive list base address in CSR3 and the transmit list base address in CSR4.
4. Set full-duplex mode (CSR6<9>).
5. In 10BASE-T/AUI mode, using Table 3–68 as a guide, set CSR13 through CSR15.
6. In 10BASE-T/AUI mode, wait for the link pass interrupt.
7. Place the transmit and receive processes in the running state by using the start commands.
8. Resume normal processing. Execute any 21143 interrupts.

6.6 Autonegotiation

The IEEE 802.3 10BASE-T autonegotiation algorithm allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment. Similarly, a device can detect corresponding enhanced operation modes that the other device may be advertising. The algorithm builds upon the existing 10BASE-T link pulse scheme and is based on data exchange in the physical layer between two nodes.

The 21143 implements this algorithm for 10BASE-T and 100BASE-TX half-duplex and full-duplex mode autonegotiation and 100BASE-T4 mode autonegotiation. The whole negotiation is done by the 21143 without software involvement. At the end of the negotiation, the 21143 chooses the operating mode according to Table 6–8.

Table 6–8 Autonegotiation Modes Selection

CSR12<25:21>[1]	CSR14<18:16>[2]	CSR14<6>[2]	CSR6<9>[2]	Selected Mode
X1XXX[3]	X1X	X	X	100BASE-TX FD[4]
XX1XX	001	X	X	100BASE-TX HD[5]
001XX	XX1	X	X	100BASE-TX HD
XXX1X	000	X	1	10BASE-T FD
0001X	XXX	X	1	10BASE-T FD
XXXX1	000	1	0	10BASE-T HD
00001	XXX	1	X	10BASE-T HD
1XXXX	10X	X	X	T4
10XXX	1XX	X	X	T4
All other cases				No common mode

[1]Link partner's link code word

[2]21143 advertisement

[3]Binary representation

[4]Full-duplex

[5]Half-duplex

If the selected mode at the end of negotiation is 10BASE-TX, the receive and transmit paths are only enabled if the link integrity test passed successfully within 1 second. Otherwise, the autonegotiation process automatically starts again.

If the selected mode at the end of negotiation is 100BASE-TX, the driver should select the MII/SYM port. The receive and transmit paths are only enabled if the 100BASE-TX link integrity test passed successfully within 1 second. Otherwise, the autonegotiation process starts again.

In addition, when there is no common mode of operation between the two link partners, the autonegotiation process automatically starts once again within 1 second after negotiation has completed.

To enable the autonegotiation mechanism, CSR14<7> (autonegotiation enable) must be set. Table 3–68 shows the programming of the SIA with autonegotiation enabled.

Before enabling its receive or transmit paths, or after the link integrity test has failed, the 21143 starts an autonegotiation sequence with its link partner. The 21143 stops sending its link pulses for at least 1 second and moves its link partner into the link fail state, forcing it to renegotiate.

An autonegotiation completed interrupt, together with CSR12<14:12> read as 101#2, indicates the end of the negotiation. The driver then reads CSR12 to get the link test status, and the driver also has the ability to restart the negotiation by setting the CSR12<14:12> field to a value of 001.

6.7 Capture Effect–A Value-Added Feature

As a value-added feature, the 21143 provides a complete solution to an unsolved Ethernet and IEEE 802.3 problem referred to as capture effect. This solution is not part of the IEEE 802.3 standard. A device implementing this feature deviates from the IEEE 802.3 standard backoff algorithm. Therefore, this feature is optional and can be enabled or disabled using the CSR6<17> control bit.

6.7.1 What Is Capture Effect?

Consider two stations on the line, station A and station B. Each station has a significant amount of data ready to transmit. Each station is able to satisfy the minimum IPG rules (both from transmit-to-transmit and from receive-to-transmit operations). The following steps show how station A captures the line (Table 6–9):

1. Station A (with data A1) and station B (with data B1) both attempt to transmit simultaneously within a slot time of 51.2 μs. Each station has an initial collision count set to 0.

2. The stations experience a collision. Both stations increment their collision count to 1.
3. Each station picks a backoff time value that is uniformly distributed from 0 to (2*n*)–1 slots. In this example, station B selects a backoff of 1 (a 50% probability), and station A selects a backoff of 0.
4. Station A successfully transmits its A1 data packet. Station B waits for data A1 to be transmitted before attempting to retransmit data B1.
5. Collision count at station B remains at 1, while collision count at station A is reset to 0.
6. If station A has another packet (data A2) ready to transmit while station B still wants to transmit its packet (data B1), the stations both contend for the line again.
7. If these stations collide, the backoff value available for station A is 0 or 1 slots. The backoff value available for station B is 0, 1, 2, or 3 slots because the collision count is now at 2 (station A's collision count is at 1). Station A is more likely to succeed and transmit data A2, while data B1 from station B begins the deferral of completing its backoff interval.
8. It is possible, with this type of behavior between stations, that in the 2-node Ethernet, a station can capture the channel for an unfair amount of time. One station can transmit a significant number of packets back to back, while the other station continues to backoff further and further.
9. This process could continue until station B reaches the maximum number of collisions, 16, while attempting to transmit data B1. At this time, station B would access the line and transmit data B1.

Note: If station A completes the transmitting of a stream of packets during this type of capture, and station B is still in backoff, potentially for a long time, the line is idle for this period of time.

Table 6–9 shows the capture-effect sequence.

Table 6–9 Capture-Effect Sequence

Station A	Line	Station B	Collision A	Count B
Transmit packet A1	Collision	Transmit packet B1	0	0
Backoff 0, 1	—	Backoff 0, 1	1	1
Transmit packet A1	Packet A1	Backoff	0	1
Transmit packet A2	Collision	Transmit packet B1	0	1
Backoff 0, 1	—	Backoff 0, 1, 2, 3	1	2
Transmit packet A2	Packet A2	Backoff	0	2
Transmit packet A3	Collision	Transmit packet B1	0	2
Backoff 0, 1	—	Backoff 0, 1, 2, ... 7	1	3

6.7.2 Resolving Capture Effect

The 21143 generally resolves the capture effect by having the station use, after a successful transmission of a frame by a station, a 2–0 backoff algorithm on the next transmit frame. If the station senses a frame on the network before it attempts to transmit the next frame, regardless of whether the sensed frame destination address matches the station's source address, the station returns to use the standard truncated binary exponential backoff algorithm (Section 6.3.3.4).

When the station executes the 2–0 backoff algorithm, it always waits for a 2-slot period on the first collision, and for a 0-slot period on the second collision. For retransmission attempts greater than 2, it uses the standard truncated, binary exponential backoff algorithm.

Table 6–10 summarizes the 2–0 backoff algorithm.

Table 6–10 2–0 Backoff Algorithm

Retransmission Attempts	Backoff Period (Number of Slot Times)
$n = 1$	Backoff = 2 slots
$n = 2$	Backoff = 0 slots
$n = 3$ to 15	Backoff = $0 \leq r < 2^k$ k = min (n, N) and N = 10 r = uniformly distributed random integer

6.7.3 Enhanced Resolution for Capture Effect

The 21143 offers an enhanced resolution for capture effect. The enhancement is made by incorporating a stopped backoff algorithm (with the 2–0 backoff algorithm) to reduce collision while maintaining the key properties of the 2–0 backoff algorithm.

When the enhanced resolution for the capture effect bit is set (CSR6<31>), the 21143 activates the stopped backoff algorithm as follows: in a back-to-back transmit, while in backoff after the first collision (*n*=1, where *n* is the retransmission attempts), the 21143 stops its backoff timer for the duration when the channel is busy. It continues its backoff timer when the channel is idle. For any other collision cases, the backoff timer is not stopped.

6.8 Jabber and Watchdog Timers

The jabber timer monitors the time of each packet transmission. The watchdog timer monitors the time of each packet reception. If a single packet transmission or reception exceeds a programmable value (Section 3.2.2.15), the jabber and watchdog circuitry automatically disables both the transmit and receive path. The transmit jabber timer provides the jabber function by cutting off transmission and asserting the collision signal to the MAC.

The packet descriptor closes with both transmit jabber timeout (TDES0<14>) and late collision (TDES0<9>) setting if the jabber timer expires on a transmit packet.

The receive watchdog provides the watchdog function by cutting off reception. The packet descriptor closes with the receive watchdog bit (RDES0<4>) set.

7
External Ports

This chapter describes the interface and operation of the boot ROM, the MicroWire serial ROM, the general-purpose port, and the network activity LEDs. This chapter also describes how to connect an external register to the boot ROM port.

7.1 Overview

The 21143 provides a boot ROM interface that may be optionally used on the adapter. The boot ROM (expansion ROM) may contain code that can be executed for device-specific initialization and, possibly, a system boot function. During machine boot, the BIOS looks for bootable devices by searching a specific signature (55AA). Once found, the BIOS copies the code from the boot ROM to a shadow RAM in the host memory and executes the code from the RAM. Refer to *PCI BIOS Specification Revision 2.1*.

The boot ROM interface supports:

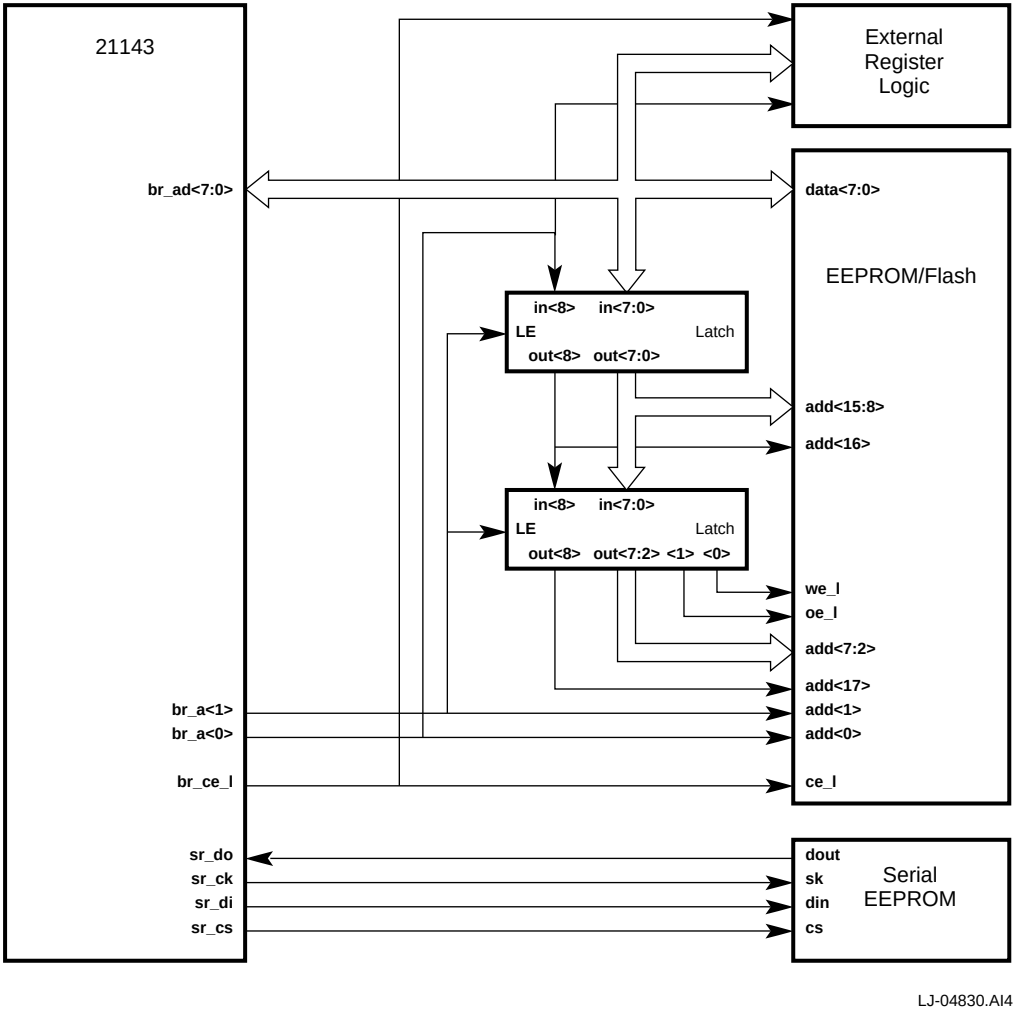
- 5-V or 12-V flash memory for code upgrade
- 240-ns EEPROM or faster
- Up to 256KB address space

The 21143 provides a software-controlled, serial port interface suitable for MicroWire and other common serial ROM devices. The serial ROM contains the IEEE address and, optionally, other system parameters.

7.2 Boot ROM and Serial ROM Connection

Figure 7–1 shows the connection of a 256KB boot ROM and the serial ROM. The two 9-bit edge trigger latches are used to latch the boot ROM addresses <17:2> and the **oe_l** and **we_l** control signals.

Figure 7–1 Boot ROM, Serial ROM, and External Register Connection



7.3 Boot ROM Operations

Access to the boot ROM is done in two ways:

- Byte access (read/write) by using CSR9 and CSR10.
- Dword (32-bit) read access from the PCI expansion ROM address space.

The following sections describe these accesses. For each, the boot ROM must be set to the desired mode (read or write) prior to the actual access for the read or write transaction. For additional information about how this is done, refer to the specific ROM device documentation.

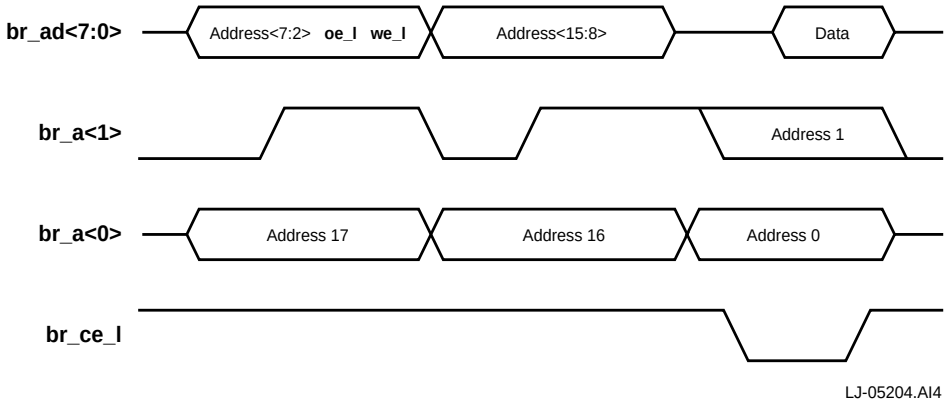
Any mixture between byte access and Dword access is allowed, providing that byte access followed by Dword access will be separated by at least 20 PCI clock cycles.

7.3.1 Byte Read

Figure 7–2 shows the 21143 byte read cycle. It is executed as follows:

1. The host initiates a byte read cycle to the boot ROM by writing the boot ROM offset to CSR10 and by setting a read command in CSR9 (CSR9<14>) and CSR9<12> = 1.
2. The 21143 drives the boot ROM address bits <7:2> and the signals **oe_l** and **we_l** on the **br_ad** lines, drives address bit 17 on the **br_a<0>** line, and sets **br_a<1>**. Signal **br_a<1>** is used as a latch_enable to latch the address, **oe_l**, and **we_l** in the upper edge trigger latch.
3. The 21143 clears **br_a<1>**.
4. The 21143 drives the boot ROM address bits <15:8> on the **br_ad** lines, drives address bit 16 on the **br_a<0>** line, and sets **br_a<1>**. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (17, <7:2>) and the control signals (**oe_l** and **we_l)** are latched in the lower edge trigger latch.
5. The 21143 drives address bits <1:0> on **br_a<1>** and **br_a<0>**, respectively, and asserts the **br_ce_l** pin.
6. In response, the boot ROM drives the data on the **br_ad** lines.
7. The 21143 terminates the byte read cycle by sampling the data, by placing it in CSR9<7:0>, and by deasserting the **br_ce_l** signal.
8. The driver can read the data from CSR9 after at least 20 PCI clock cycles passed since this CSR was previously written. Note that the results of trying to read the data earlier are **UNPREDICTABLE**.

Figure 7–2 Boot ROM Byte Read Cycle



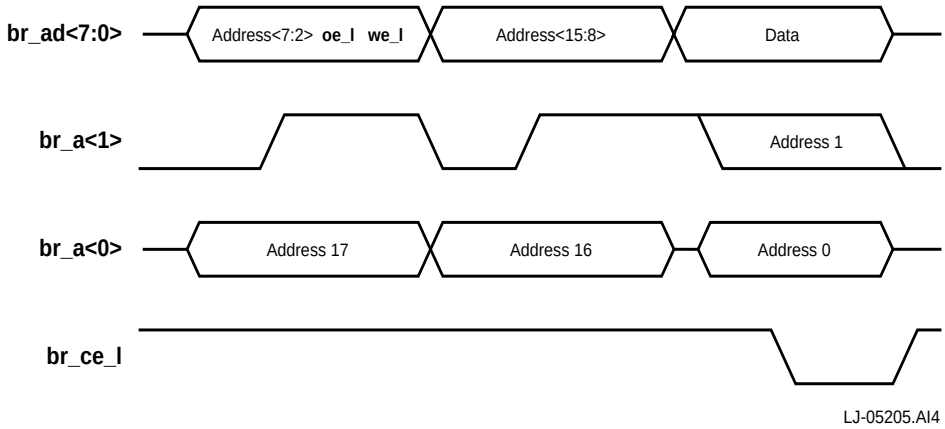
7.3.2 Byte Write

Before performing a write operation, all the boot ROM entries must be 1. This is achieved by using the erase command.

Figure 7–3 shows the 21143 byte write cycle. It is executed as follows:

1. The host initiates a byte write cycle to the boot ROM by writing the boot ROM offset to CSR10, setting a write command in CSR9 (CSR9<13> and CSR9<12> = 1), and by writing the data to CSR9<7:0>.
2. The 21143 drives the boot ROM address bits <7:2> and the signals **oe_l** and **we_l** on the **br_ad** lines, drives address bit 17 on the **br_a<0>** line, and sets **br_a<1>**. Signal **br_a<1>** is used as a latch_enable to latch the address, **oe_l**, and **we_l** in the upper edge trigger latch.
3. The 21143 clears **br_a<1>**.
4. The 21143 drives the boot ROM address bits <15:8> on the **br_ad** lines, drives address bit 16 on the **br_a<0>** line, and sets **br_a<1>**. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (<17>, <7:2>) and the control signals (**oe_l** and **we_l)** are latched in the lower edge trigger latch.
5. The 21143 drives address bits <1:0> on **br_a<1>** and **br_a<0>**, respectively; drives the data on the **br_ad** lines; and asserts the **br_ce_l** pin.
6. The boot ROM samples the data.
7. The 21143 terminates the byte write cycle by deasserting the **br_ce_l** signal.

Figure 7–3 Boot ROM Byte Write Cycle



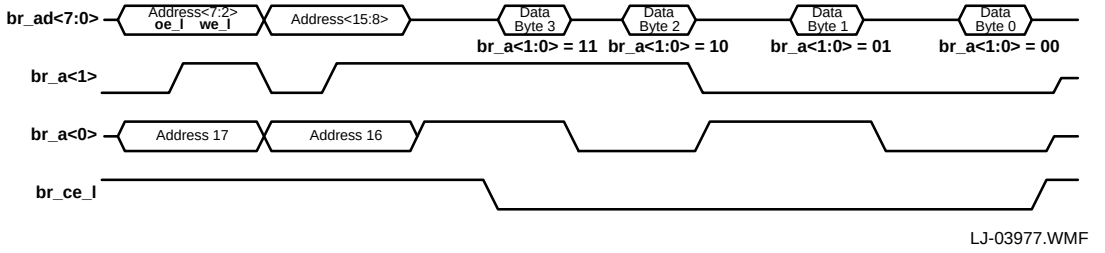
7.3.3 Dword Read

Figure 7–4 shows the Dword read cycle. The host initiates a Dword read cycle by executing a typical read cycle to the expansion ROM address space. The **ad** lines contain the expansion ROM address (base address and offset). Prior to the assertion of the **trdy_l** signal, the 21143 takes the following steps:

1. The 21143 drives the boot ROM address bits <7:2> and the control signals **oe_l** and **we_l** on the **br_ad** lines, drives address bit 17 on the **br_a<0>** line, and sets **br_a<1>**. Signal **br_a<1>** is used as a **latch_enable** to latch the address, **oe_l**, and **we_l** in the upper edge trigger latch.
2. The 21143 clears **br_a<1>**.
3. The 21143 drives the boot ROM address bits <15:8> on the **br_ad** lines, drives address bit 16 on the **br_ad<0>** line, and sets **br_a<1>**. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (17, <7:2>) and the control signals **oe_l** and **we_l** are latched in the lower edge trigger latch.
4. The 21143 remains **br_a<1>** high, drives **br_a<0>** to high, and asserts the **br_ce_l** pin.
5. In response, the boot ROM drives the data on the **br_ad** lines (byte 3).
6. The 21143 samples the data (byte 3).
7. The 21143 remains **br_a<1>** high, drives **br_a<0>** to low, and asserts the **br_ce_l** pin.

8. In response, the boot ROM drives the data on the **br_ad** lines (byte 2).
9. The 21143 samples the data (byte 2).
10. The 21143 drives **br_a<1>** to low, drives **br_a<0>** high, and asserts the **br_ce_l** pin.
11. In response, the boot ROM drives the data on the **br_ad** lines (byte 1).
12. The 21143 samples the data (byte 1).
13. The 21143 remains **br_a<1>** low, drives **br_a<0>** to low, and asserts the **br_ce_l** pin.
14. In response, the boot ROM drives the data on the **br_ad** lines (byte 0).
15. The 21143 samples the data and deasserts the **br_ce_l** signal.
16. The 21143 assembles the 4 bytes, drives the data on the **ad** lines, and asserts **trdy_l**.

Figure 7–4 Boot ROM Dword Read Cycle



7.4 Serial ROM Operations

There are four serial ROM interface pins (Table 3–52):

Serial ROM data out (CSR9<3>)
Serial ROM data in (CSR9<2>)
Serial ROM serial clock (CSR9<1>)
Serial ROM chip select (CSR9<0>)

All EEPROM access sequences and timing are handled by software. An exception to this is the loading of the CSID and CCIS configuration register values from the SROM. This read is automatically completed by the 21143 after a hardware reset without software involvement.

Serial ROM operations include the following: read and write. In addition, the erase EEPROM operation is also supported and is handled similarly to the read and write operations.

7.4.1 Read Operation

Read operations consist of three phases:

1. Command phase—3 bits (binary code of 110)
2. Address phase—6 bits for 256-bit to 1Kb ROMs, 8 bits for 2Kb to 4Kb ROMs.
3. Data phase—16 bits

Figure 7–5 and Figure 7–6 show a typical read cycle that describes the action steps that need to be taken by the driver to execute a read cycle. The timing (listed on the right side of the figures) specifies the minimum time that the driver must wait before advancing to the next action.

During both the address phase in Figure 7–5 and the data phase in Figure 7–6, 1 bit is handled during each phase cycle. Therefore, the address phase should be repeated 6 or 8 times depending on the address length and the data phase should be repeated 16 times. Note that the value DX is the current data bit.

Figure 7–5 Read Cycle (Page 1 of 2)

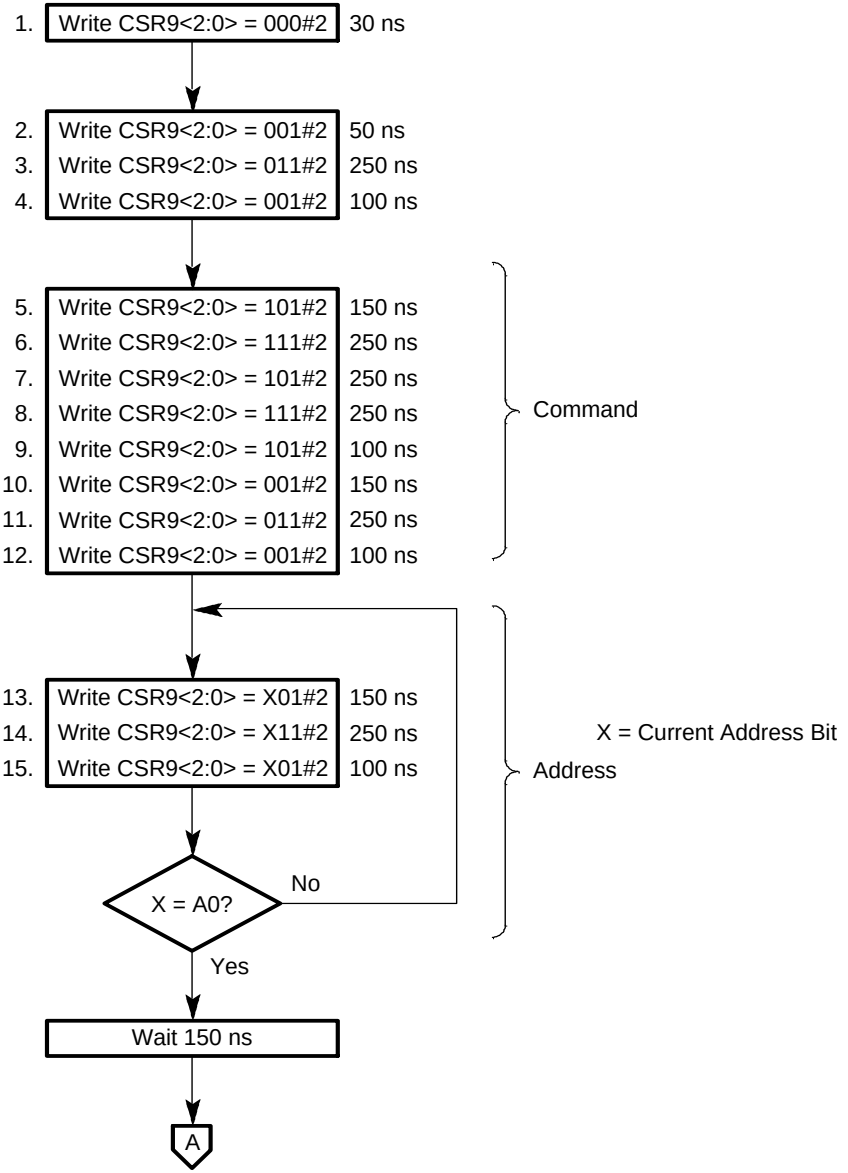


Figure 7–6 Read Cycle (Page 2 of 2)

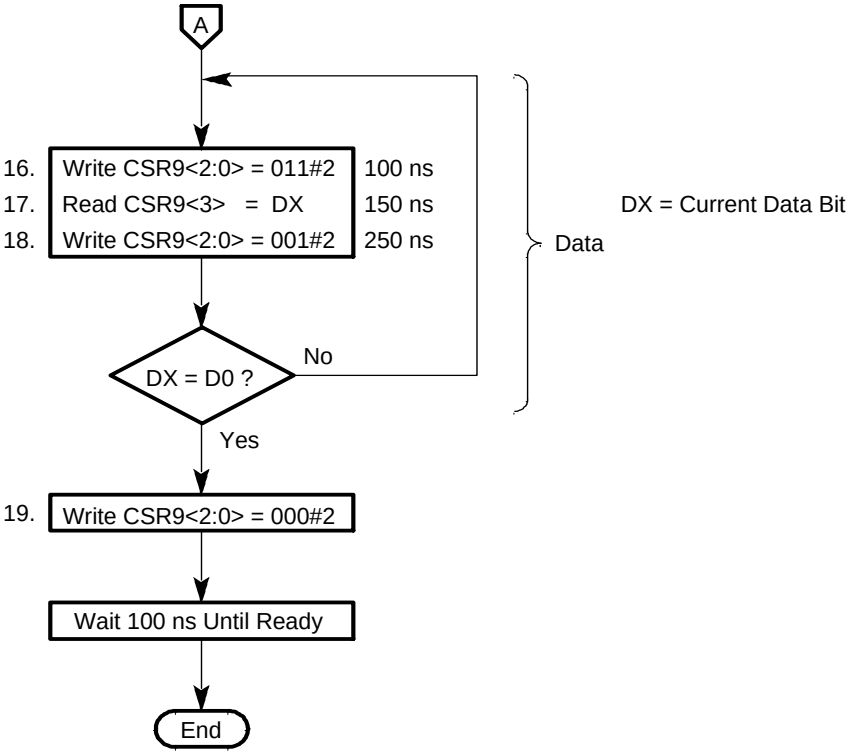
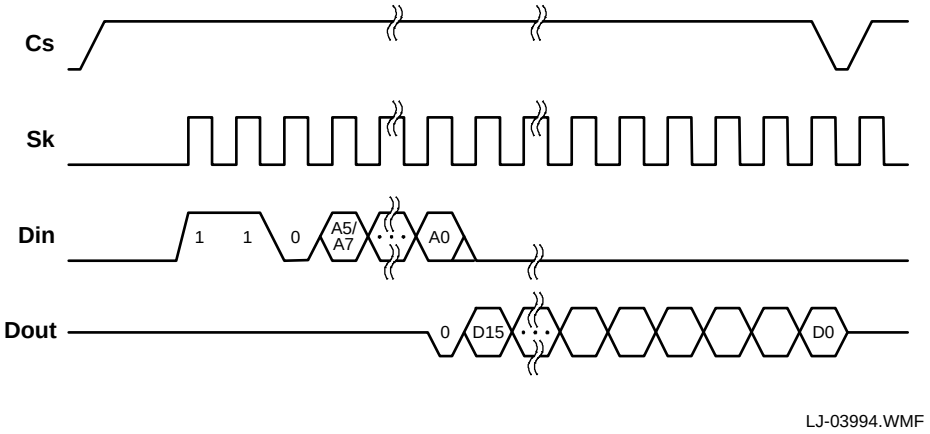


Figure 7–7 shows the read operation timing of the address and data.

Figure 7–7 Read Operation



7.4.2 Write Operation

Write operations consist of three phases:

1. Command phase—3 bits (binary code of 101
2. Address phase—6 bits for 256-bit to 1Kb ROMs, 8 bits for 2Kb to 4Kb ROMs.
3. Data phase—16 bits

Figure 7–8 and Figure 7–9 show a typical write cycle that describes the action steps that need to be taken by the driver to execute a write cycle. The timing (listed on the right side of the figures) specifies the minimum time that the driver must wait before advancing to the next action.

During both the address phase in Figure 7–8 and the data phase in Figure 7–9, 1 bit is handled during each phase cycle. Therefore, the address phase should be repeated 6 or 8 times depending on the address length and the data phase should be repeated 16 times.

Figure 7–8 Write Cycle (Page 1 of 2)

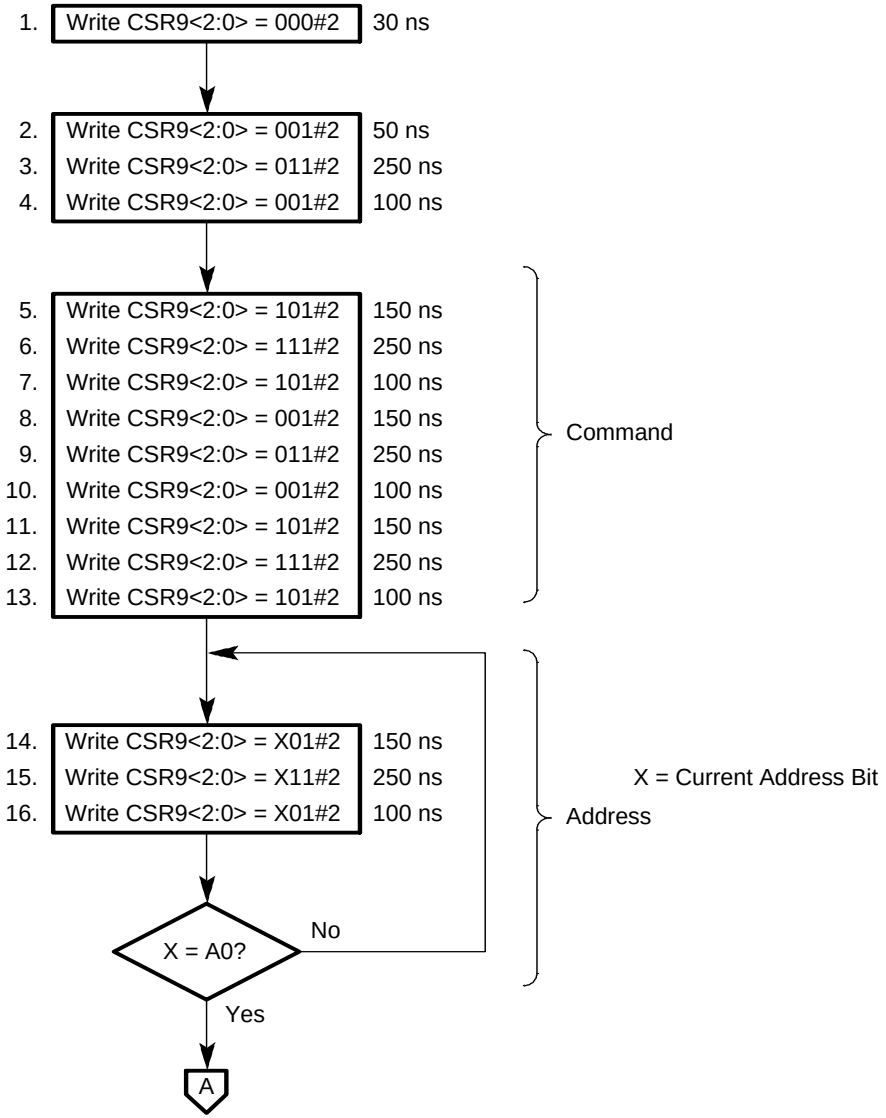


Figure 7–9 Write Cycle (Page 2 of 2)

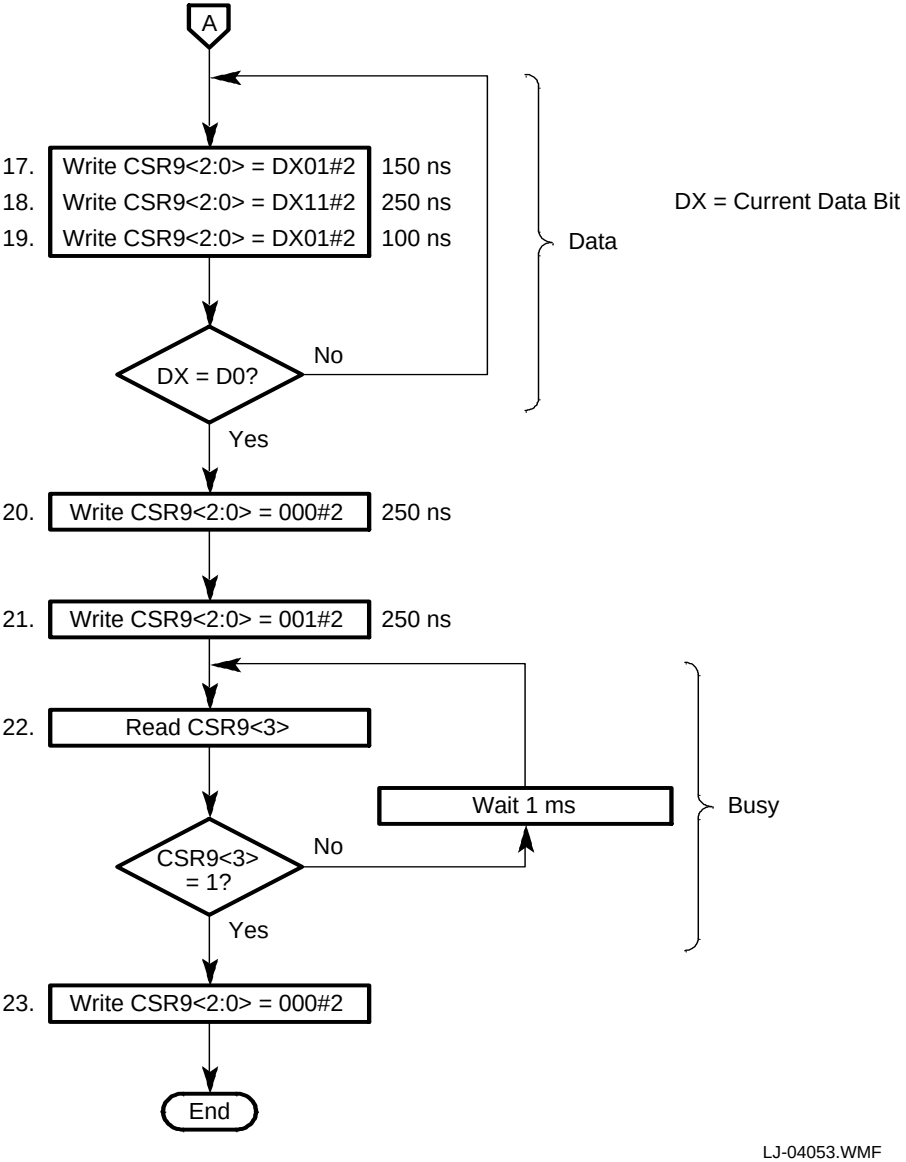
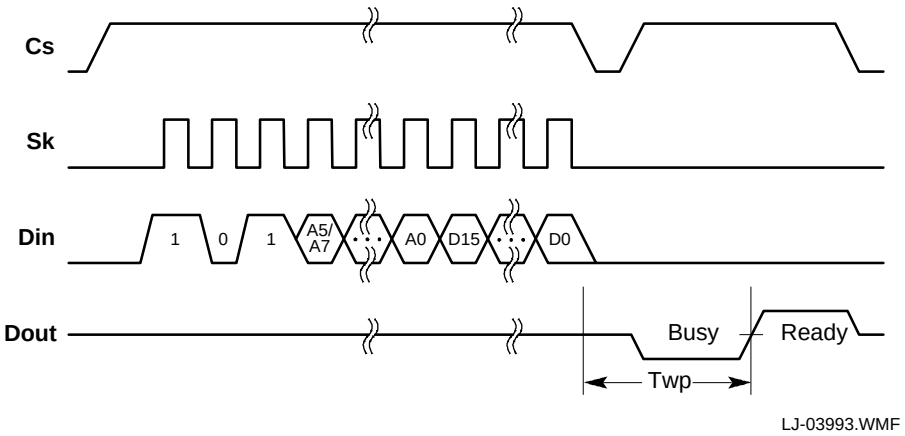


Figure 7–10 shows the write operation timing of the address and data. The time period indicated by **twp** is the actual write cycle time.

Figure 7–10 Write Operation



7.5 External Register Operation

The 21143 provides the ability to connect an external 8-bit register to the boot ROM port. Figure 7–1 illustrates the signals for this connection. For a detailed description of external register connection, refer to *Using the Digital Semiconductor 21143 Boot ROM, Serial ROM, and External Register: An Application Note*.

Note: CSR10 must be 0 before any external register access is done.

To read from the external register, the driver should set the read command (CSR9<14>) and select the external register (CSR9<10> =1). The 21143 performs the same steps as described in Section 7.3.1. The only differences are that now the 21143 drives 1 on both the **we_l** and **oe_l** boot ROM inputs and drives 0 on **br_a<0>**. This, together with the assertion of **br_ce_l**, performs the actual read operation. The data is sampled by the 21143 and is placed in CSR9<7:0>.

To write to the external register, the driver should set the write command (CSR9<13>), select the external register (CSR9<10>=1), and write the data to CSR9<7:0>. The 21143 performs the same steps as described in Section 7.3.2. The only differences are that now the 21143 drives 1 on both the **we_l** and **oe_l** boot ROM inputs and drives 1 on **br_a<0>**. This, together with the assertion of **br_ce_l**, performs the actual write operation.

7.6 General-Purpose Port and LEDs

The 21143 contains a 4-bit port (**gep<3:0>**) that can be used as either as a general-purpose port or for network event LEDs. Each of the four pins can be programmed to be either a general-purpose port pin or for an LED/control pin. Each general-purpose port pin can be programmed to be either an input pin or an output pin. When programmed as an input pin, **gep<1:0>** can generate an interrupt when the pin changes its state either from 1 to 0 or 0 to 1. Refer to Section 3.2.2.15 (CSR15<30:16>) for a detailed programming description.

Section 7–1 provides a description of each LED and related pin connection.

Table 7–1 LED Description

Signal	Pin Number	Description
aui_bnc	100	AUI (10BASE5) or BNC (10BASE2) select line.
activ	101	Receive or transmit activity.
rcv_match	102	A receive packet passed address recognition.
10bt_link	103	The 10BASE-T link integrity test passed successfully.

8
Remotely Waking Up the LAN

This chapter describes the operation for remotely waking up a sleeping workstation using the remote wake-up-LAN and SecureON features of the 21143.[1]

8.1 Overview

The remote wake-up-LAN mode of operation is a mechanism that uses Advanced Micro Device's Magic Packet technology to power up a sleeping workstation on the network. This mechanism is accomplished when the 21143 receives a specific packet of information, called a Magic Packet, addressed to the node on the network.

For additional protection, SecureON is an optional security feature that can be added to the Magic Packet that requires a password to power up the sleeping workstation.

When the 21143 is in remote wake-up-LAN mode, main system power can be shut down leaving power only for the 21143 and the PHY chip (hereafter called the auxiliary power condition).

The 21143 performs no network activities while in the remote wake-up-LAN mode of operation—it only monitors the network for receipt of a Magic Packet. If a Magic Packet is addressed to the 21143 on the network, the 21143 asserts (low) an interrupt pin (**int_l**)[2] and sets (high) a special output pin (**gep<2>**)[2] to wake up the system. If the SecureON feature has been enabled, the password added to the Magic Packet is also verified prior to waking up the system.

8.2 Remote Wake-Up Controller Block Diagram

Figure 8–1 shows a block diagram of the 21143 that includes the Remote Wake-Up Controller. The Remote Wake-Up Controller supports the following features:

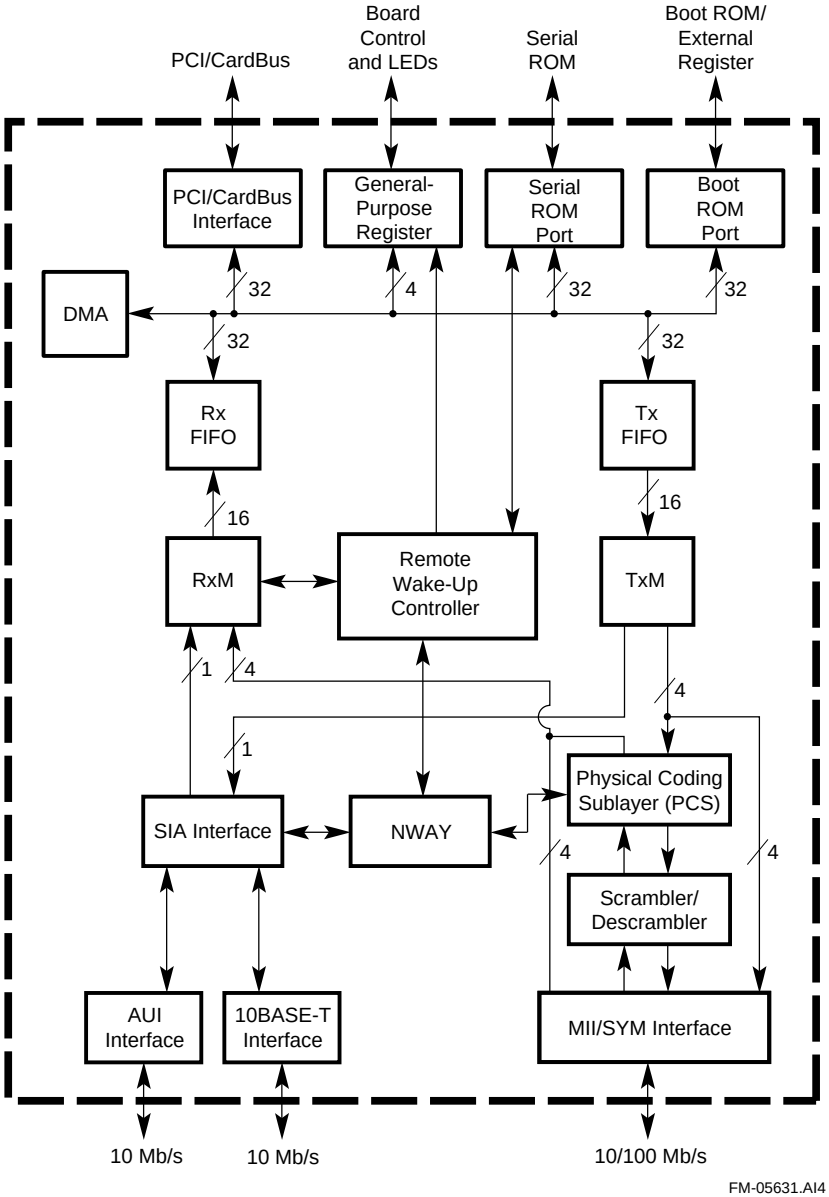
- Remote wake-up-LAN—Mechanism that powers up a sleeping workstation upon receiving a Magic Packet.

[1]These features are not supported on the 21143–PA and the 21143–TA.

[2]This function is in addition to those listed in Table 2–1.

- SecureON—Enables a password-security feature that can be added to the Magic Packet and an attack-limiter circuit for limiting the number of invalid passwords.

Figure 8–1 21143 Remote Wake-Up Controller Block Diagram



8.3 Remote Wake-Up-LAN Operation

There are two methods for using the remote wake-up-LAN mode of operation:

- With the main system power *off* (auxiliary power condition)
- With the main system power *on*

8.3.1 Remote Wake-Up-LAN Mode with Main System Power Off

The 21143 and all other components needed for operation of the network interface obtain power from an auxiliary power source.

The 21143 continually senses the main system power status on a single dedicated pin. When the 21143 notices that the main system power has been turned off, it automatically enters remote wake-up-LAN mode. Also, if the auxiliary power supply goes off and then returns (with the main power still off), the 21143 will automatically enter remote wake-up-LAN mode.

While in remote wake-up-LAN mode, the 21143 is in sleep mode except for the remote wake-up-LAN circuits. The 21143 places all PCI output pins in tristate mode and disables all its PCI input drivers. This drastically reduces the 21143 power consumption.

The IEEE address for the Magic Packet and a control word are stored in a dedicated data block within the SROM.[1] The control word indicates if the SecureON password feature is enabled and the type of cable autosensing.

When the 21143 enters the remote wake-up-LAN mode of operation, it reads the remote wake-up-LAN data block from the SROM. If it detects bad CRC for the block, the 21143 ignores its remote wake-up-LAN functions. If the 21143 detects good CRC, it uses the remote wake-up-LAN IEEE address as a receive address filter. Only Magic Packets with that address or a broadcast address will be checked to meet the wake-up packet requirements. Magic Packets that pass the address filtering (physical or broadcast) will be checked to meet the remote wake-up-LAN data format with the same remote wake-up-LAN IEEE address appearing 16 times. If the SecureON password feature is enabled, the password is verified and the system benefits from an attack-limiter circuit. For more information about the attack-limiter circuit, see Section 8.4.

[1]The remote wake-up-LAN IEEE address might be different from the run-time IEEE address of the workstation.

While the 21143 is in remote wake-up-LAN mode, it is totally independent of the software driver. The 21143 implements network port autosensing and autonegotiation (NWAY). It automatically selects the correct serial port for network connection after link failure or auxiliary power loss and return. The 21143, after successfully detecting a Magic Packet, asserts the interrupt signal **int_l** low along with signal **gep<2>** high. The system recognizes assertion of these pins as a wake-up call. The system will then turn on main system power and issue a hardware reset signal (PCI reset), forcing the 21143 out of remote wake-up-LAN mode.

8.3.2 Remote Wake-Up-LAN Mode with Main System Power On

In this mode, the main system power remains on. System software sets the FORCE_WAKE_UP_LAN (FWUL) bit in the 21143's configuration wake-up command register (see Section 8.7.3).

When this bit is set, the 21143 is forced to enter remote wake-up-LAN mode and read the remote wake-up-LAN data block from the SROM. If it detects bad CRC for the block, the 21143 ignores its remote wake-up-LAN functions. If the 21143 detects good CRC, it uses the remote wake-up-LAN IEEE address as a receive address filter. Only Magic Packets with that address or a broadcast address will be checked to meet the wake-up packet requirements. Magic Packets that pass the address filtering (physical or broadcast) will be checked to meet the remote wake-up-LAN data format with the same remote wake-up-LAN IEEE address appearing 16 times. If the SecureON password feature is enabled, the password is verified and the system benefits from an attack-limiter circuit. For more information about the attack-limiter circuit, see Section 8.4.

The remote wake-up-LAN parameters stored in the SROM are also implemented as registers in the PCI configuration space. These parameters can be written by the system software while the 21143 is in the remote wake-up-LAN mode if the LOCK bit is not set. This allows the system software to override any remote wake-up-LAN parameter read from the SROM through the PCI configuration space remote wake-up-LAN registers. These parameters include the remote wake-up-LAN IEEE address, SecureON password, and remote wake-up-LAN command parameters. If the LOCK bit is set in the SROM's remote wake-up-LAN command word or in the remote wake-up-LAN command register, the remote wake-up-LAN parameters cannot be written by the system software.

The remote wake-up-LAN command register cannot be read after the 21143 completes a remote wake-up-LAN operation. The remote wake-up-LAN IEEE address and SecureON password can never be read from their registers.

If those registers are accessed while the 21143 is reading the remote wake-up-LAN parameters from the SROM, it will send a PCI retry response. This mechanism ensures that remote wake-up-LAN IEEE address and remote wake-up-LAN command override by system software will occur after the 21143 has finished reading the remote wake-up-LAN parameters from the SROM.

The 21143, after successfully detecting a Magic Packet, asserts the interrupt signal **int_l** low along with signal **gep<2>** high. The system recognizes the assertion of these pins as a wake-up call. The 21143 also provides a register status bit that indicates receipt of a Magic Packet. This register bit will not be cleared by any reset (write 1 to clear the bit).

There are two ways to return the 21143 from remote wake-up-LAN mode operation to normal mode operation:

- The system issues a hardware reset signal (PCI reset) forcing the 21143 out of remote wake-up-LAN mode.
- The system software issues a reset command by writing a 1 to CSR0 bit 0 in the 21143. This action is equivalent to a hardware reset.

Note: The 21143 does not process any setup frame that is queued while the 21143 is in remote wake-up-LAN mode.

8.4 Invalid Password Limiter

To limit the number of invalid passwords from unauthorized users, the 21143 benefits from a special attack-limiter circuit. This circuit is activated by enabling the SecureON feature. Any Magic Packet with a valid remote wake-up-LAN format, including a good CRC but with an invalid password, is identified as an attack attempt. The 21143 counts every attack and sets CSR15<15> (HCKR) after receiving 16 attack attempts.

The 21143 also counts all attack attempts within a time interval of 20 seconds. If there are no attack attempts within a 20-second interval, this count is reset to zero. If there are four attack attempts within a 20-second interval, the attack-limiter circuitry locks the reception of further Magic Packets for a duration of 20 seconds.

8.5 Configuration Revision Register (CFRV–Offset 08H)

The CFRV register contains the 21143 revision number. Figure 8–2 shows the CFRV register bit fields and Table 8–1 describes the bit fields.

Figure 8–2 CFRV Register Bit Fields

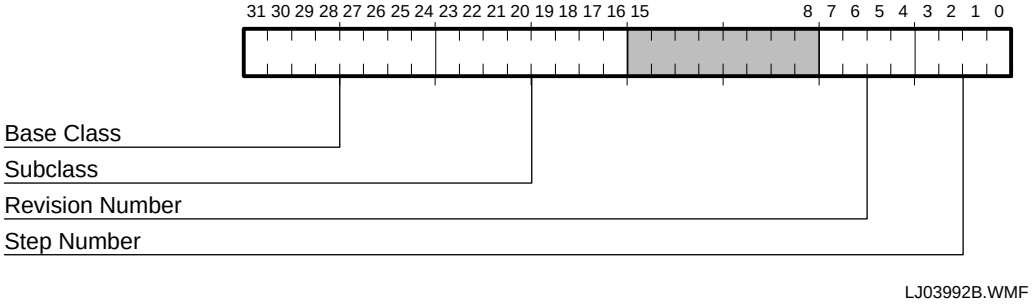


Table 8–1 CFRV Register Bit Fields Description

Field	Description
31:24	**Base Class**
	Indicates the network controller and is equal to 2H.
23:16	**Subclass**
	Indicates the fast Ethernet controller and is equal to 0H.
7:4	**Revision Number**
	Indicates the 21143 revision number and is equal to 3H. This number is incremented for subsequent 21143 revisions.
3:0	**Step Number**
	Indicates the 21143 step number and is equal to 0H. This number is incremented for subsequent 21143 steps within the current revision.

Table 8–2 lists the access rules for the CFRV register.

Table 8–2 CFRV Register Access Rules

Category	Description
Value after hardware reset	02000030H
Read access rules	—
Write access rules	Writing has no effect.

8.6 SIA and General-Purpose Port Register (CSR15–Offset 78H)

This section shows and describes the enhanced format of CSR15, which includes the addition of bit 15 (HCKR) and bit 14 (RMP).

Figure 8–3 shows the CSR15 register bit fields. CSR15 is divided into two sections: the SIA general register (CSR15<15:0>) and the general-purpose port register (CSR15<31:16>). Appendix E describes the general-purpose port programming procedures.

Figure 8–3 CSR15 Register Bit Fields

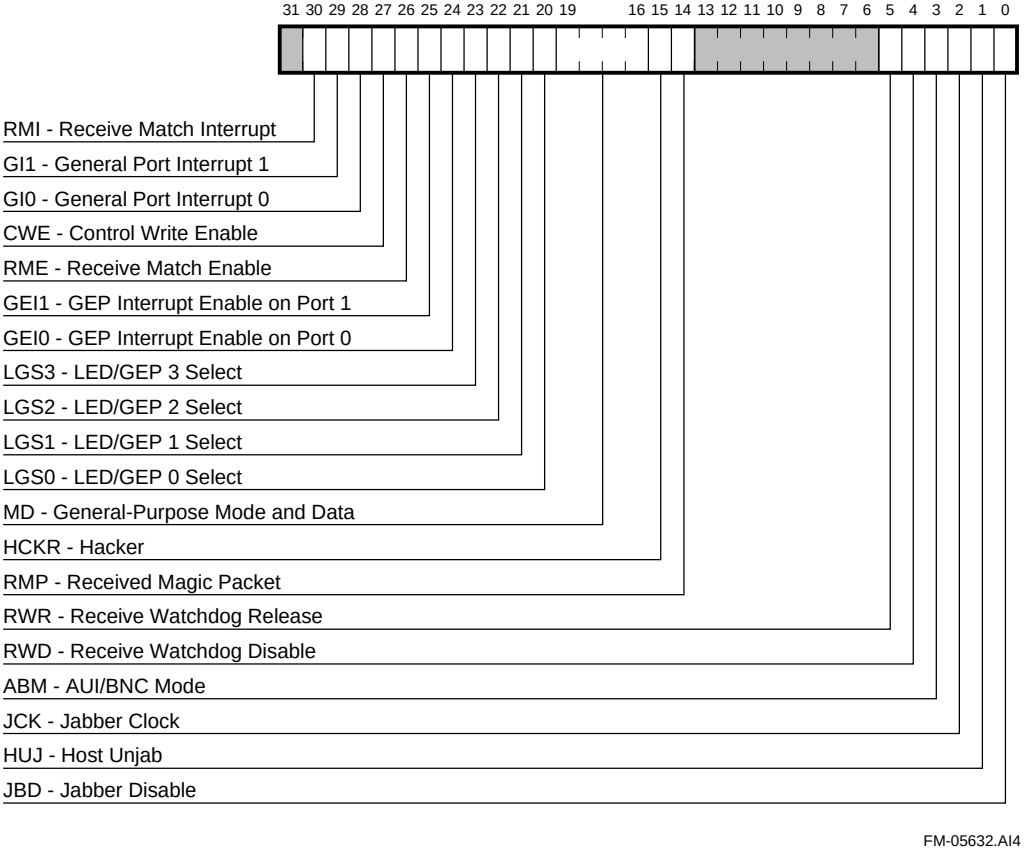


Table 8–3 describes the bit fields.

Table 8–3 CSR15 Register Bit Fields Description *(Sheet 1 of 4)*

Field	Description
30	**RMI—Receive Match Interrupt** Indicates that a packet has passed address filtering. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
29	**GI1—General Port Interrupt 1** Indicates that **gep<1>** has changed state. This bit is set only when **gep<1>** is programmed to be a general-purpose input port. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
28	**GI0—General Port Interrupt 0** Indicates that **gep<0>** has changed state. This bit is set only when **gep<0>** is programmed to be a general-purpose input port. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
27	**CWE—Control Write Enable** When CSR15 is written and CSR15<27> value is 1, the general-purpose control bits will be written. The general-purpose control bits include interrupt enables (CSR15<26:24>), LED/GEP selects (CSR15<23:20>), and general-purpose pin directions (CSR15<19:16>). When CSR15 is written and CSR15<27> value is 0, only general-purpose data (CSR15<19:16>) will be written.
26	**RME—Receive Match Enable** When this bit is set, receive match interrupt (CSR15<30>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
25	**GEI1—GEP Interrupt Enable on Port 1** When this bit is set, the interrupt from pin **gep<1>** (CSR15<29>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.

Table 8–3 CSR15 Register Bit Fields Description *(Sheet 2 of 4)*

Field	Description
24	**GEI0—GEP Interrupt Enable on Port 0** When this bit is set, the interrupt from **gep<0>** (CSR15<28>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
23	**LGS3—LED/GEP 3 Select** This bit selects either the **10bt_link** or **gep<3>** function for 21143 pin number 103. When this bit is set, the **10bt_link** function is selected, which provides a LED indicating the status of the 10BASE-T port link integrity test (sets when the test completes successfully). When this bit is reset, the **gep<3>** function is selected. The **gep<3>** pin is a general-purpose port. After a hardware or software reset, the **gep<3>** function is selected.
22	**LGS2—LED/GEP 2 Select** This bit selects either the **rcv_match** or **gep<2>** function for 21143 pin number 102. When this bit is set, the **rcv_match** function is selected, which provides a LED indicating the status of the address recognition (sets when a packet passes address recognition). When this bit is reset, the **gep<2>** function is selected. The **gep<2>** pin is a general-purpose port. After a hardware or software reset, the **gep<2>** function is selected.
21	**LGS1—LED/GEP 1 Select** This bit selects either the **activ** or **gep<1>** function for 21143 pin number 101. When this bit is set, the **activ** function is selected, which provides a LED indicating receive or transmit activity on the selected port (sets when there is receive or transmit activity on the selected port). When this bit is reset, the **gep<1>** function is selected. The **gep<1>** pin is a general-purpose port. After a hardware or software reset, the **gep<1>** function is selected.
20	**LGS0—LED/GEP 0 Select** This bit selects either the **aui_bnc** or **gep<0>** function for 21143 pin number 100. When this bit is set, the **aui_bnc** function is selected, which provides a control line to select either 10BASE5 (AUI) or 10BASE2 (BNC) as programmed by CSR15<3>. When this bit is reset, the **gep<0>** function is selected. The **gep<0>** pin is a general-purpose port. After a hardware or software reset, the **gep<0>** function is selected.

Table 8–3 CSR15 Register Bit Fields Description *(Sheet 3 of 4)*

Field	Description
19:16	**MD—General-Purpose Mode and Data** When CSR15<27> is set, the value that is written by the host to CSR15<19:16> directs pins **gep<3:0>** to act as input or output pins (CSR15<19> controls pin **gep<3>** and so on). A 1 directs the pin to be an output while a 0 directs the pin to be an input. When CSR15<27> is reset, the values written to CSR15<19:16> are the values that will be driven on pins **gep<3:0>**, respectively. This is only true for the pins that are configured as output pins. After the 21143 is reset, all **gep** pins become input pins. If **gep<1:0>** pins are selected as input pins, an interrupt occurs when either of these bits change state from 1 to 0 or 0 to 1 (provided that the interrupt CSR15<25:24> is enabled). The application of the general-purpose pins in board design should be correlated with the way the port driver software is using it. Reading CSR15<19:16> returns the values of pins **gep<3:0>**.
15	**HCKR—Hacker** When set, indicates that 16 packets have been received with a matching remote wake-up-LAN format, including a good CRC but with a nonmatching password.
14	**RMP—Received Magic Packet** When set, indicates that a Magic Packet has been received. Writing a 1 to this bit will clear it. It is unaffected by any reset.
5	**RWR—Receive Watchdog Release** Defines the time interval from receive watchdog expiration until reenabling the receive channel (*no carrier)*. When set, the receive watchdog is released 40- to 48-bit-times from the last carrier deassertion. When reset, the receive watchdog is released 16- to 24-bit-times from the last carrier deassertion.
4	**RWD—Receive Watchdog Disable** When set, the receive watchdog counter is disabled. When clear, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog counter to timeout. Packets shorter than 2048 bytes are guaranteed to pass.
3	**ABM—AUI/BNC Mode** This bit is used by the driver to select either AUI or BNC mode. When set, AUI (10BASE5) is selected. When clear, BNC (10BASE2) is selected. The value programmed to this bit is the value that is driven in the **gep<0>/aui_bnc** pin when it is set to **aui_bnc**. This pin is used mainly to enable the external BNC transceiver in 10BASE2 mode.

Table 8–3 CSR15 Register Bit Fields Description *(Sheet 4 of 4)*

Field	Description
2	**JCK—Jabber Clock** When set, transmission is cut after 2048 bytes to 2560 bytes are transmitted (1.6 ms to 2.0 ms). When reset, transmission is cut after 26 ms to 33 ms in 10BASE-T/AUI mode or after 2.6 ms to 3.3 ms in 100-Mb/s MII/SYM mode.
1	**HUJ—Host Unjab** Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the transmit jabber is released 365 ms to 420 ms after jabber expiration in 10BASE-T/AUI mode or 36.5 ms to 42 ms after jabber expiration in 100-Mb/s MII/SYM mode.
0	**JBD—Jabber Disable** When set, the transmit jabber function is disabled.

Table 8–4 lists the access rules for the CSR15 register.

Table 8–4 CSR15 Register Access Rules

Category	Description
Value after reset	8FFX0000H
Read access rules	CSR15<27:20> are write-only bits.
Write access rules	CSR13 should be reset to 00000000H before writing CSR15 bits 0 through 5, and should be released with or just after writing those bits.

8.7 PCI Configuration Registers

The 21143 contains five configuration registers in addition to those registers listed in Table 3–1. The Ethernet address and the SecureON password registers use a naming convention of A-B-C-D-E-F, with "A" representing the first byte of the remote wake-up-LAN IEEE address to be transmitted on the Ethernet wire (see Section 8.9).

These registers are described in Table 8–5 and shown in Table 8–6.

Table 8–5 Remote Wake-Up-LAN Configuration Registers

Configuration Register	Identifier	I/O Address Offset
Configuration Wake-Up-LAN IEEE address 0 (D, C, B, A)	CWUA0	44H
Configuration Wake-Up-LAN IEEE address 1 (F, E)	CWUA1	48H
SecureON Password (D, C, B, A)	SOP0	4CH
SecureON Password (F, E)	SOP1	50H
Configuration Wake-Up command	CWUC	54H

Table 8–6 Remote Wake-Up-LAN Registers in the PCI Configuration Space

PCI-Specific Fields		0
Remote Wake-Up-LAN IEEE Address (B)	Remote Wake-Up-LAN IEEE Address (A)	44
Remote Wake-Up-LAN IEEE Address (D)	Remote Wake-Up-LAN IEEE Address (C)	46
Remote Wake-Up-LAN IEEE Address (F)	Remote Wake-Up-LAN IEEE Address (E)	48
Not Implemented (Read As 0)		4A
SecureON Password (B)	SecureON Password (A)	4C
SecureON Password (D)	SecureON Password (C)	4E
SecureON Password (F)	SecureON Password (E)	50
Not Implemented (Read As 0)		52
Remote Wake-Up-LAN Command	Remote Wake-Up-LAN Command	54

8.7.1 Configuration Wake-Up-LAN IEEE Address 0 Register (CWUA0–Offset 44H)

The CWUA0 is a write-only register and contains the remote wake-up-LAN IEEE address <47:16>. This address is used as the 21143 address in remote wake-up-LAN mode. The CWUA0 is loaded from the serial ROM when remote wake-up-LAN mode is entered. Writing to this register will override the value that was loaded from the serial ROM. If the CWUA0 is accessed by the host before the remote wake-up-LAN IEEE parameters are loaded from the serial ROM, the 21143 responds with a retry termination on the PCI bus. Figure 8–4 shows the CWUA0 register.

Figure 8–4 CWUA0 Register Bit Fields

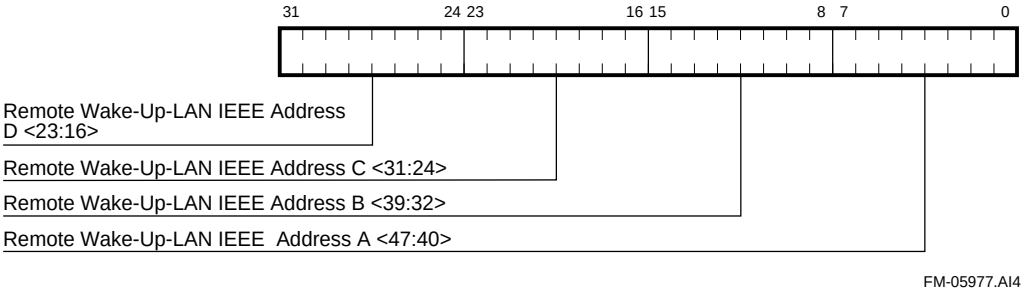


Table 8–7 describes the CWUA0 register bit fields.

Table 8–7 CWUA0 Register Bit Fields Description

Field	Description
31:24	**Remote Wake-Up-LAN IEEE Address D <23:16>**
	Defines one byte of the remote wake-up-LAN IEEE address.
23:16	**Remote Wake-Up-LAN IEEE Address C <31:24>**
	Defines one byte of the remote wake-up-LAN IEEE address.
15:8	**Remote Wake-Up-LAN IEEE Address B <39:32>**
	Defines one byte of the remote wake-up-LAN IEEE address.
7:0	**Remote Wake-Up-LAN IEEE Address A <47:40>**
	Defines the first byte of the remote wake-up-LAN IEEE address.

Table 8–8 contains the CWUA0 register access rules.

Table 8–8 CWUA0 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	Not allowed
Write access rules	—

8.7.2 Configuration Wake-Up-LAN IEEE Address 1 Register (CWUA1–Offset 48H)

The CWUA1 is a write-only register and contains the remote wake-up-LAN IEEE address <15:0>. This address is used as the 21143 address in remote wake-up-LAN mode. The CWUA1 is loaded from the serial ROM when remote wake-up-LAN mode is entered. Writing to this register will override the value that was loaded from the serial ROM. If the CWUA1 is accessed by the host before the remote wake-up-LAN IEEE parameters are loaded from the serial ROM, the 21143 responds with a retry termination on the PCI bus. Figure 8–5 shows the CWUA1 register.

Figure 8–5 CWUA1 Register Bit Fields

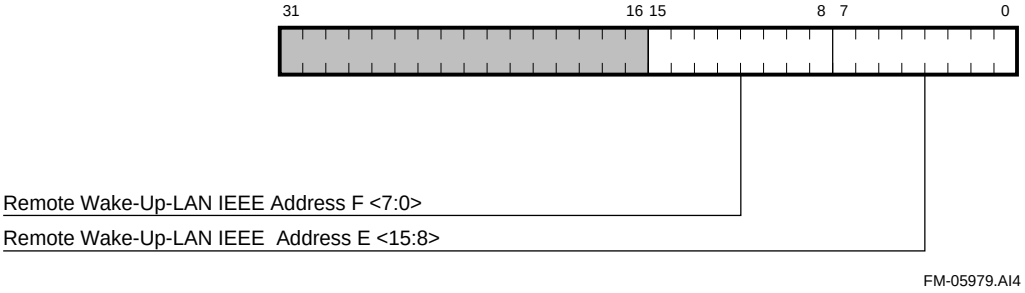


Table 8–9 describes the CWUA1 register bit fields.

Table 8–9 CWUA1 Register Bit Fields Description

Field	Description
15:8	**Remote Wake-Up-LAN IEEE Address F <7:0>**
	Defines one byte of the remote wake-up-LAN IEEE address.
7:0	**Remote Wake-Up-LAN IEEE Address E <15:8>**
	Defines the last byte of the remote wake-up-LAN IEEE address.

Table 8–10 contains the CWUA1 register access rules.

Table 8–10 CWUA1 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	Not allowed
Write access rules	—

8.7.3 Configuration Wake-Up Command Register (CWUC–Offset 54H)

The CWUC controls functions of the remote wake-up-LAN feature. The CWUC is loaded from the serial ROM when remote wake-up-LAN mode is entered. Writing to this register will override the value that was loaded from the serial ROM. If the CWUC is accessed by the host before the remote wake-up-LAN parameters are loaded from the serial ROM, the 21143 responds with a retry termination on the PCI bus. Figure 8–6 shows the CWUC register.

Figure 8–6 CWUC Register Bit Fields

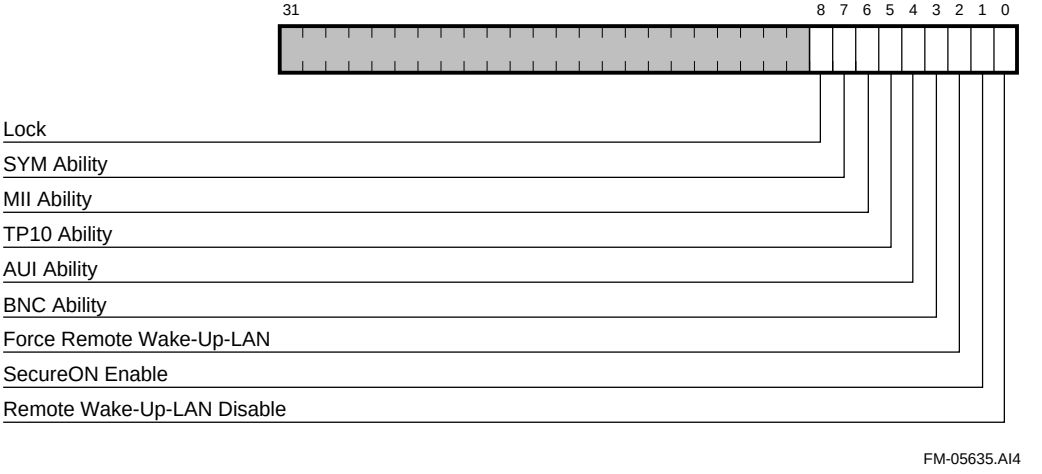


Table 8–11 describes the CWUC register bit fields.

Table 8–11 CWUC Register Bit Fields Description *(Sheet 1 of 2)*

Field	Description
8	**Lock** If set to 1: • Remote wake-up-LAN command register is disabled for writes and reads all 1s. • Remote wake-up-LAN IEEE address register and SecureON password register are disabled for writes. The 21143 exits from the Lock state only in a hardware reset.

Table 8–11 CWUC Register Bit Fields Description *(Sheet 2 of 2)*

Field	Description
7[1]	**SYM Ability** When set, indicates that the 21143 is connected to a symbol PHY device. The remote wake-up-LAN mode attempts autosensing on the SYM PHY port and enables autonegotiation
6	**MII Ability** When set, indicates that the 21143 is connected to an MII PHY device. The remote wake-up-LAN mode selects the MII PHY port.
5[1]	**TP10 Ability**[2] When set, indicates that the 21143 is connected to the twisted pairs. The remote wake-up-LAN mode attempts autosensing on TP 10 Mb/s and enables autonegotiation.
4[1]	**AUI Ability** When set, indicates that the 21143 is connected to an AUI. The remote wake-up-LAN mode attempts autosensing on the AUI.
3[1]	**BNC Ability**[3] When set, indicates that the 21143 is connected to the BNC. The remote wake-up-LAN mode attempts autosensing on the BNC.
2	**Force Remote Wake-Up-LAN** When set, forces the 21143 into remote wake-up-LAN mode. Usually, the 21143 enters remote wake-up-LAN mode by sensing power-supply conditions. This bit is used in specific implementations.
1	**SecureON Enable** When set, enables the password-security feature for Magic Packet and the attack-limiter circuit.
0	**Remote Wake-Up-LAN Disable** When set, disables the remote wake-up-LAN mode.

[1]The **mii_mdio** pin (pin 135) should be tied to **Vss** when not in MII mode.

[2]If no PHY device is connected to the MII/SYM port, the **sd** pin (pin 117) should be tied to **Vss** in order to make the link-integrity test operate properly.

[3]If BNC is selected when in remote wake-up-LAN mode, pin **gep<0>** will be set to enable the external BNC transceiver. It will be set regardless of the values in CSR15<20> (LED/GEP 0 Select) and CSR15<3> (AUI/BNC Mode).

Table 8–12 contains the CWUC register access rules.

Table 8–12 CWUC Register Access Rules

Category	Description
Value after reset	00000000H
Read access rules	—
Write access rules	CWUC<2> may be set only when receive and transmit processes are stopped.

8.7.4 SecureON™ Password Register (SOP0–Offset 4CH)

The SOP0 is a write-only register that contains the SecureON password <47:16>. This password is compared to the password in the Magic Packet for validation while the 21143 is in remote wake-up-LAN mode. The SOP0 is loaded from the serial ROM while the 21143 is in remote wake-up-LAN mode. The SOP0 register can also be written by a software application while the 21143 is in remote wake-up-LAN mode with the system power on. The SOP0 register is not readable; a value of 0 will be returned if a read is attempted.

If the SOP0 is accessed by the host before the remote wake-up-LAN parameters are loaded from the serial ROM, the 21143 responds with a retry termination on the PCI bus. Figure 8–7 shows the SOP0 register.

Figure 8–7 SOP0 Register Bit Fields

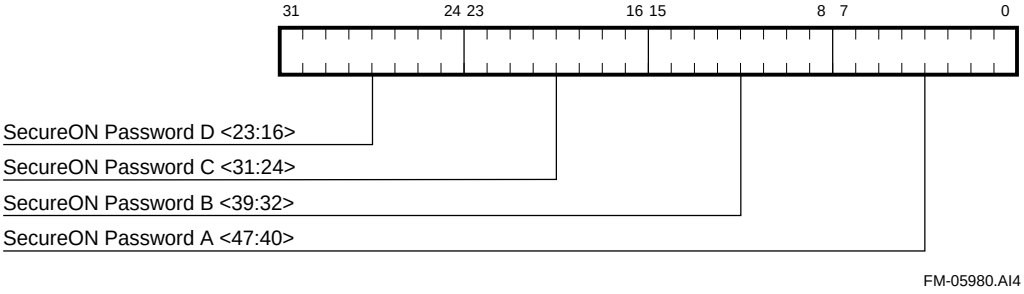


Table 8–13 describes the SOP0 register bit fields.

Table 8–13 SOP0 Register Bit Fields Description

Field	Description
31:24	**SecureON Password D <23:16>**
	Defines one byte of the SecureON password.
23:16	**SecureON Password C <31:24>**
	Defines one byte of the SecureON password.
15:8	**SecureON Password B <39:32>**
	Defines one byte of the SecureON password.
7:0	**SecureON Password A <47:40>**
	Defines the first byte of the SecureON password.

Table 8–14 contains the SOP0 register access rules.

Table 8–14 SOP0 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	Not allowed
Write access rules	—

8.7.5 SecureON Password Register (SOP1–Offset 50H)

The SOP1 is a write-only register that contains the SecureON password <15:0>. This password is compared to the password in the Magic Packet for validation while the 21143 is in remote wake-up-LAN mode. The SOP1 is loaded from the serial ROM while the 21143 is in remote wake-up-LAN mode. The SOP1 register can also be written by a software application while the 21143 is in remote wake-up-LAN mode with the system power on. The SOP1 register is not readable; a value of 0 will be returned if a read is attempted.

If the SOP1 is accessed by the host before the remote wake-up-LAN parameters are loaded from the serial ROM, the 21143 responds with a retry termination on the PCI bus. Figure 8–8 shows the SOP1 register.

Figure 8–8 SOP1 Register Bit Fields

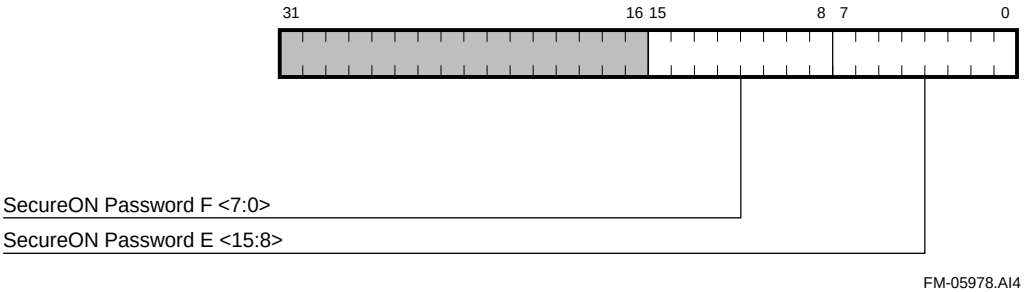


Table 8–15 describes the SOP1 register bit fields.

Table 8–15 SOP1 Register Bit Fields Description

Field	Description
15:8	**SecureON Password F <7:0>**
	Defines one byte of the SecureON password.
7:0	**SecureON Password E <15:8>**
	Defines the last byte of the SecureON password.

Table 8–16 contains the SOP1 register access rules.

Table 8–16 SOP1 Register Access Rules

Category	Description
Value after reset	**UNPREDICTABLE**
Read access rules	Not allowed
Write access rules	—

8.8 Remote Wake-Up-LAN Data Block in the SROM

Table 8–17 shows the remote wake-up-LAN data block in the SROM.

Table 8–17 Data Block in the SROM

15 8	7 0	Byte Offset[1] in SROM
Application-Specific SROM Data		0
SecureON Password (B)	SecureON Password (A)[2]	96
SecureON Password (D)	SecureON Password (C)	98
SecureON Password (F)	SecureON Password (E)	100
Remote Wake-Up-LAN IEEE Address (B)	Remote Wake-Up-LAN IEEE Address (A)	102
Remote Wake-Up-LAN IEEE Address (D)	Remote Wake-Up-LAN IEEE Address (C)	104
Remote Wake-Up-LAN IEEE Address (F)	Remote Wake-Up-LAN IEEE Address (E)	106
Remote Wake-Up-LAN Command	Remote Wake-Up-LAN Command	108
Reserved (16 Bytes) Must Be Zero		110
Reserved (1 Byte) Must Be Zero	WAKE_UP_LAN_BLOCK_CRC (Calculated on Bytes 96:127)	126

[1]Byte offset of 1Kb in SROM.

[2]Reserved if SecureON is enabled, otherwise must be zero.

8.8.1 Remote Wake-Up-LAN IEEE Address and Command (SROM)

Table 8–18 describes the fields for the SecureON password, the remote wake-up-LAN IEEE address, and the remote wake-up-LAN command in the SROM.

Table 8–18 Remote Wake-Up-LAN Data Block in the SROM *(Sheet 1 of 3)*

Field	Size (Bytes)	Description
SecureON Password	6	This field contains the SecureON password. If the SecureON feature is enabled, only remote wake-up-LAN packets that have valid passwords will invoke the system. This field is enabled by setting bit 1 in the remote wake-up-LAN command word in the SROM or the equivalent bit in the remote wake-up-LAN command register.
Remote Wake-Up-LAN IEEE Address	6	This field contains the IEEE address of the workstation to be awakened. The format is the same as the IEEE network address field format. Only remote wake-up-LAN packets or broadcast packets that passed the remote wake-up-LAN IEEE address filtering will invoke the system.

Table 8–18 Remote Wake-Up-LAN Data Block in the SROM *(Sheet 2 of 3)*

Field	Size (Bytes)	Description
Remote Wake-Up-LAN Command	2	This field controls the remote wake-up-LAN functions.

15 9	8	7	6	5	4	3	2	1	0
MBZ	Lock	SYM	MII	TP10	AUI	BNC	MBZ	Sec_ON_En	WUL_Dis

MBZ	These bits must be 0s.
Lock	If set to 1: • Remote wake-up-LAN command register is disabled for writes and reads all 1s. • Remote wake-up-LAN IEEE address register and SecureON password register are disabled for writes. The 21143 exits from the Lock state only in a hardware reset.
SYM	When set, indicates that the 21143 is connected to a symbol PHY device. The remote wake-up-LAN mode attempts autosensing on the SYM PHY port and enables autonegotiation.
MII	When set, indicates that the 21143 is connected to an MII PHY device. The remote wake-up-LAN mode selects the MII PHY port.
TP10	When set, indicates that the 21143 is connected to the twisted pairs. The remote wake-up-LAN mode attempts autosensing on TP 10 Mb/s and enables autonegotiation.
AUI	When set, indicates that the 21143 is connected to an AUI. The remote wake-up-LAN mode attempts autosensing on the AUI.
BNC	When set, indicates that the 21143 is connected to the BNC. The remote wake-up-LAN mode attempts autosensing on the BNC.
MBZ	This bit must be 0.
Sec_ON_En	Enables SecureON password matching mode and functionality.
WUL_Dis	When set, disables the remote wake-up-LAN mode.

Table 8–18 Remote Wake-Up-LAN Data Block in the SROM *(Sheet 3 of 3)*

Field	Size (Bytes)	Description
WAKE_UP_ LAN_BLOCK_ CRC	1	The CRC polynomial for the remote wake-up-LAN block is calculated on bytes 96:127 as follows: FCS(X) = $X^8 + X^2 + X^1 + 1$.

8.9 21143 Magic Packet Format

Table 8–19 shows the structure of a Magic Packet used in the 21143.

Table 8–19 Magic Packet Format for the 21143

Physical/Broadcast Destination Address (A)[1]	
Physical/Broadcast Destination Address (B)	
Physical/Broadcast Destination Address (C)	
Physical/Broadcast Destination Address (D)	
Physical/Broadcast Destination Address (E)	
Physical/Broadcast Destination Address (F)	
Source Node Physical Address (6 Bytes)	
Length/Type (2 Bytes)	
Miscellaneous Data (M Bytes)	
SYNCH1 (FFh)	
SYNCH2 (FFh)	
SYNCH3 (FFh)	
SYNCH4 (FFh)	
SYNCH5 (FFh)	
SYNCH6 (FFh)	
Remote Wake-Up-LAN IEEE Address (A)	
Remote Wake-Up-LAN IEEE Address (B)	Repeated
Remote Wake-Up-LAN IEEE Address (C)	16
Remote Wake-Up-LAN IEEE Address (D)	Times
Remote Wake-Up-LAN IEEE Address (E)	
Remote Wake-Up-LAN IEEE Address (F)	
SecureON Password (A)[2]	
SecureON Password (B)[2]	
SecureON Password (C)[2]	
SecureON Password (D)[2]	
SecureON Password (E)[2]	
SecureON Password (F)[2]	
Miscellaneous Data (N Bytes)	
CRC (4 Bytes)	

[1]Physical Address = Remote Wake-Up-LAN IEEE Address.

[2]Must be provided if the SecureON feature is enabled.

Example 8–1 shows the fields of a 21143 Magic Packet with a valid SecureON password.

Example 8–1 21143 Magic Packet Fields

```
Physical Destination Address (A-B-C-D-E-F) 08-00-2B-11-22-33

Source Node Physical Address 08-00-2B-44-55-66

Length/Type 00-00

SecureON Password (A-B-C-D-E-F) E1-E2-E3-E4-E5-E6

The Magic Packet for the 21143 would consist of the following
data plus four bytes of CRC, (transmitted in byte order from
left to right, and top to bottom):

08 00 2B 11 22 33    (Remote Wake-Up-LAN IEEE Address)
08 00 2B 44 55 66    (Source Node Physical Address)
00 00                (Length/Type Field)
FF FF FF FF FF FF    (Synchronization Pattern)
08 00 2B 11 22 33    (Remote Wake-Up-LAN IEEE Address)
08 00 2B 11 22 33    (Repeated 16 Times)
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
E1 E2 E3 E4 E5 E6    (SecureON Password)
```

Note: The match is performed byte by byte. If one address does not match, the 21143 scans the Magic Packet for another synchronization pattern and repeats the match process. The 21143 makes no assumption of the content of the source node physical address. For example, the source node physical address can start with consecutive FF or have FF at any place in the 6-byte address field.

A

Joint Test Action Group—Test Logic

This appendix describes the joint test action group (JTAG) test logic and the associated registers (instruction, bypass, and boundary scan).

A.1 General Description

JTAG test logic supports testing, observing, and modifying circuit activity during the components normal operation.

As a PCI device, the 21143 supports the IEEE standard 1149.1 *Test Access Port and Boundary Scan Architecture*. The IEEE 1149.1 standard specifies the rules and permissions that govern the design of the 21143 JTAG test logic support. Inclusion of JTAG test logic allows boundary scan to be used to test both the device and the board where it is installed. The JTAG test logic consists of the following four signals to serially interface within the 21143 (Table 2–1):

tck — JTAG clock

tdi — Test data and instructions in

tdo — Test data and instructions out

tms — Test mode select

Note: If JTAG test logic is not implemented, the **tck** pin should be connected to ground, and both the **tms** and **tdi** pins should be left unconnected or connected high. The **tdo** signal should remain unconnected.

These test pins operate in the same electrical environment as the 21143 PCI I/O buffers.

The system vendor is responsible for the design and operation of the 1149.1 serial chains (rings) required in the system. Typically, an 1149.1 ring is created by connecting one device's **tdo** pin to another device's **tdi** pin to create a serial chain of devices. In this application, the 21143 receives the same **tck** and **tms** signals as the other devices. The entire 1149.1 ring is connected to either a motherboard test connector for test purposes or to a resident 1149.1 controller.

Note: To understand the description of the 21143 JTAG test logic in this section, the system designer should be familiar with the IEEE 1149.1 standard.

A.2 Registers

In JTAG test logic design, three registers are implemented through the 21143 pads:

Instruction register

Bypass register

Boundary-scan register

A.2.1 Instruction Register

The 21143 JTAG test logic instruction register is a 3-bit (IR<2:0>) scan-type register that is used to direct the JTAG machine to the appropriate operating JTAG mode (Table A–1). Its contents are interpreted as test instructions. The test instructions select the boundary-scan registers for serial transfer of test data by using the **tdi** and **tdo** pins. These instructions also control the operation of the selected test features.

Table A–1 Instruction Register *(Sheet 1 of 2)*

IR<2>	IR<1>	IR<0>	Description
0	0	0	EXTEST mode (mandatory instruction) allows testing of the 21143 board-level interconnections. Test data is shifted into the boundary-scan register of the 21143 and then is transferred in parallel to the output pins.
0	0	1	Sample-preload mode (mandatory instruction) allows the 21143 JTAG boundary-scan register to be initialized prior to selecting other instructions such as EXTEST. It is also possible to capture data at system pins while the system is running, and to shift that data out for examination.
0	1	0	Reserved.

Table A–1 Instruction Register *(Sheet 2 of 2)*

IR<2>	IR<1>	IR<0>	Description
0	1	1	Reserved.
1	0	0	Reserved.
1	0	1	Tristate mode (optional instruction) allows the 21143 to enter power-saving mode. When this occurs, the PCI and serial ROM port pads are tristated. The MII and SRL ports continue to operate normally without any power reduction.
1	1	0	Continuity mode (optional instruction) allows the 21143 continuity test while in production.
1	1	1	Bypass mode (mandatory instruction) allows the test features on the 21143 JTAG test logic to be bypassed. This instruction selects the bypass register to be connected between **tdi** and **tdo**. When the bypass mode is selected, the operation of the test logic has no effect on the operation of the system logic. Bypass mode is selected automatically when power is applied.

A.2.2 Bypass Register

The bypass register is a 1-bit shift register that provides a single-bit serial connection between the **tdi** and **tdo** signals when either no other test data register in the 21143 JTAG test logic registers is selected, or the test logic in the 21143 JTAG is bypassed. When power is applied, JTAG test logic resets and then is set to bypass mode.

A.2.3 Boundary-Scan Register

The JTAG boundary-scan register consists of cells located at the PCI, serial ROM, boot ROM, GEP, and MII port pads. This register provides the ability to perform board-level interconnection tests. It also provides additional control and observation of the 21143 pins during the testing phases. For example, the 21143 boundary-scan register can observe the output enable control signals of the I/O pads: **ad_oe**, **cbe_oe**, and so on. When these signals are programmed to be 1 during EXTEST mode, data is applied to the output from the selected boundary-scan cells.

The following listing contains the order of the boundary-scan register pads:

tdi	-> int_l	-> rst_l	-> pci_clk	-> gnt_l
-> req_l	-> ad<31:24>	-> cbe_oe	-> c_be_l<3>	-> idsel
-> ad<23:16>	-> c_be_l<2>	-> frame_oe	-> frame_l	-> irdy_oe
-> irdy_l	-> trdy_oe	-> trdy_l	-> devsel_oe	-> devsel_l
-> stop_oe	-> stop_l	-> perr_oe	-> perr_l	-> serr_l
-> ad_oe	-> par_oe	-> par	-> c_be_l<1>	-> ad<15:8>
-> c_be_l<0>	-> ad<7:0>	-> inter0	-> br_a<0>	-> br_a<1>
-> br_ad<0>	-> br_ad<1>	-> br_ad<2>	-> br_ad<3>	-> br_ad<4>
-> br_ad<5>	-> br_ad_oe	-> br_ad<6>	-> br_ad<7>	-> gep<0>
-> gep0_oe	-> gep<1>	-> gep1_oe	-> gep<2>	-> gep2_oe
-> gep<3>	-> gep3_oe	-> sr_do	-> sr_di	-> sr_ck
-> inter1	-> mii_crs	-> mii_clsn	-> mii_clsn_oe	-> mii_txd<3>
-> mii_txd<2>	-> mii_txd<1>	-> mii_txd<0>	-> mii_txd0_oe	-> mii_txen
-> mii_txen_oe	-> mii_tclk	-> mii_tclk_oe	-> mii_rx_err	-> sel10_100_oe
-> mii_rclk	-> mii_rclk_oe	-> mii_dv	-> mii_dv_oe	-> mii_rxd<0>
-> mii_rxd0_oe	-> mii_rxd<1>	-> mii_rxd<2>	-> mii_rxd<3>	-> mii_mdc
-> mii_mdio	-> mii_mdio_oe	-> tdo		

Note: Internal registers inter0 and inter1 are part of the ring but unrelated to the boundary-scan register pads.

A.2.4 Test Access Port Controller

The test access port (TAP) controller interprets IEEE P1149.1 protocols received on the **tms** pin. The TAP controller generates clocks and control signals to control the operation of the test logic. The TAP controller consists of a state machine and control dispatch logic. The 21143 fully implements the TAP state machine as described in the IEEE P1149.1 standard.

B

DNA CSMA/CD Counters and Events Support

This appendix describes the 21143 features that support the driver when implementing and reporting the specified counters and events[1]. CSMA/CD[2] specified events can be reported by the driver based on these features.

B.1 CSMA/CD Counters

Table B–1 lists the counters and features.

Table B–1 CSMA/CD Counters *(Sheet 1 of 3)*

Counter	21143 Feature
Time since creation counter	Supported by the host driver.
Bytes received	Driver must add the frame length (RDES0<29:16>) fields of all successfully received frames.
Bytes sent	Driver must add the buffer 1 size (TDES1<10:0>) and buffer 2 size (TDES1<21:11>) fields of all successfully transmitted buffers.
Frames received	Driver must count the successfully received frames in the receive descriptor list.
Frames sent	Driver must count the successfully transmitted frames in the transmit descriptor list.
Multicast bytes received	Driver must add the frame length (RDES0<29:16>) fields of all successfully received frames with multicast frame (RDES0<10>) set.
Multicast frames received	Driver must count the successfully received frames with multicast frame (RDES<10>) set.

[1] As specified in the *DNA Maintenance Operations (MOP) Functional Specification*, Version T.4.0.0, 28 January 1988.

[2] Carrier-sense multiple access with collision detection.

Table B–1 CSMA/CD Counters *(Sheet 2 of 3)*

Counter	21143 Feature
Frames sent, initially deferred	Driver must count the successfully transmitted frames when deferred (TDES0<0>) is set.
Frames sent, single collision	Driver must count the successfully transmitted frames when the collision count (TDES0<6:3>) is equal to 1.
Frames sent, multiple collisions	Driver must count the successfully transmitted frames when the collision count (TDES0<6:3>) is greater than 1.
Send failure, excessive collisions	Driver must count the transmit descriptors when the excessive collisions (TDES0<8>) bit is set.
Send failure, carrier check failed	Driver must count the transmit descriptors when both late collision (TDES0<9>) and loss of carrier (TDES0<11>) are set.
Send failure, short circuit	There were two successive transmit descriptors when the no_carrier flag (TDES0<10>) is set. This indicates a short circuit.
Send failure, open circuit	There were two successive transmit descriptors when the excessive_collisions flag (TDES0<8>) is set. This indicates an open circuit.
Send failure, remote failure to defer	Flagged as a late collision (TDES0<9>) in the transmit descriptors.
Receive failure, block check error	Driver must count the receive descriptors when CRC error (RDES0<1>) is set and dribbling bit (RDES0<2>) is cleared.
Receive failure, framing error	Driver must count the receive descriptors when both CRC error (RDES0<1>) and dribbling bit (RDES0<2>) are set.
Receive failure, frame too long	Driver must count the receive descriptors when frame too long (RDES0<7>) is set.
Unrecognized frame destination	Not applicable.
Data overrun	Driver must count the receive descriptors when (RDES0<0>) is set.

Table B–1 CSMA/CD Counters *(Sheet 3 of 3)*

Counter	21143 Feature
System buffer unavailable	Reported in the missed frame counter CSR8<15:0> (Section 3.2.2.8).
User buffer unavailable	Maintained by the driver.
Collision detect check failed	Driver must count the transmit descriptors when heartbeat fail (TDES0<7>) is set.

C
Hash C Routine

This appendix provides examples of a C routine that generates the hash index for a given Ethernet address. The bit position in the hash table is taken from the CRC32 checksum derived from the first 6 bytes.

There are two C routines that follow: the first is for the little endian architecture and the second is for big endian architecture.

C.1 Little Endian Architecture Hash C Routine

```
#define CRC32_POLY   0xEDB88320UL   /* CRC-32 Poly -- Little Endian*/
#define HASH_BITS    9              /* Number of bits in hash */

unsigned
crc32_mchash(
     unsigned char *mca)
{
    u_int idx, bit, data, crc = 0xFFFFFFFFUL;

    for (idx = 0; idx < 6; idx++)
        for (data = *mca++, bit = 0; bit < 8; bit++, data >>=1)
            crc = (crc >> 1) ^ (((crc ^ data) & 1) ? CRC32_POLY : 0);

    return crc & ((1 << HASH_BITS) - 1)  /* return low bits for hash */
}
```

C.2 Big Endian Architecture Hash C Routine

```
#include <stdio>
unsigned HashIndex (char *Address);
```

Big Endian Architecture Hash C Routine

```
main (int argc, char *argv[]) {
   int Index;
   char m[6];
      if (argc < 2) {
      printf("usage: hash xx-xx-xx-xx-xx-xx\n");
      return;
   }
   sscanf(argv[1],"%2X-%2X-%2X-%2X-%2X-%2X",
     &m[0],&m[1],&m[2],
     &m[3],&m[4],&m[5]);

   Index = HashIndex(&m[0]);

   printf("hash_index = %d  byte: %d   bit: %d\n",
            Index,Index/8,Index%8);
}
unsigned HashIndex (char *Address) {

    unsigned Crc = 0xffffffff;
    unsigned const POLY  0x04c11db6
    unsigned Msb;
    int BytesLength = 6;

    unsigned char CurrentByte;
    unsigned Index;
    int Bit;
    int Shift;

    for (BytesLength=0; BytesLength<6; BytesLength++) {

      CurrentByte = Address[BytesLength];
      for (Bit=0; Bit<8 ; Bit++) {

         Msb = Crc >> 31;
         Crc  <<= 1;

         if ( Msb ^ (CurrentByte & 1)) {
             Crc ^= POLY;
             Crc |= 0x00000001;
         }
              CurrentByte >>= 1;
      }
     }
```

```
    /* the hash index is given by the upper 9 bits of the CRC
     * taken in decreasing order of significance
     * index<0> = crc<31>
     * index<1> = crc<30>
     * ...
     * index<9> = crc<23>
     */

    for (Index=0, Bit=23, Shift=8;
        Shift >= 0;
        Bit++, Shift--)  {
            Index |= ( ( (Crc>>Bit) & 1 ) << Shift );

    }

    return Index;

}
```

D

Port Selection Procedure

This appendix describes the port selection procedure for selecting one of the following 21143 ports:

MII
SYM
10BASE-T
AUI

These procedures provide the values to which the CSRs should be programmed, and also the order of programming. These procedures are for mode programming after reset, not for changing modes during operation. This appendix does not list all of the programming options. For additional options, refer to Table 3–67 and Table 3–68.

D.1 MII Port Selection

This section describes the MII port selection for both half-duplex and full-duplex modes.

- Half-duplex mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0000H
  CSR6<18> = 1

- Full-duplex mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0000H
  CSR6<9> = 1, CSR6<18> = 1

D.2 SYM Port Selection

This section describes SYM port selection for both half-duplex and full-duplex modes.

- Half-duplex mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0000H
  CSR6<18> = 1, CSR6<23> = 1, CSR6<24> = 1

- Full-duplex mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0000H
  CSR6<9> = 1, CSR6<18> = 1, CSR6<23> = 1, CSR6<24> = 1

D.3 10BASE-T Port Selection

This section describes the 10BASE-T port selection for half-duplex mode, full-duplex mode, and also with autosensing and autonegotiation.

- Half-duplex mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 7F3FH
  CSR13 = 0001H

- Full-duplex mode

  CSR6<9> = 1, CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 7F3DH
  CSR13 = 0001H

- Autonegotiation Advertising 10BASE-T and 100BASE-TX half-duplex and full-duplex Ability

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 3FFFFH
  CSR13 = 0001H

D.4 AUI Port Selection

This section describes the AUI port selection for both 10BASE5 and 10BASE2 modes.

- 10BASE5 (AUI) mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0705H
  CSR15<3> = 1
  CSR13 = 0009H

- 10BASE2 (BNC) mode

  CSR6<18> = 0
  CSR13 = 0000H
  CSR14 = 0705H
  CSR15<3> = 0
  CSR13 = 0009H

E

General-Purpose Port and LED Programming

This appendix describes the procedure for programming the general-purpose port. The general-purpose port consists of the following pins:

Pin 100—**gep<0>/aui_bnc**
Pin 101—**gep<1>/activ**
Pin 102—**gep<2>/rcv_match**
Pin 103—**gep<3>/10bt_link**

Each pin of the general-purpose port may be programmed for one of the following functions:

Input port with interrupt
Input port without interrupt
Output port
LED/Control

The procedures provide the CSR15 values for programming each of these functions. It uses 21143 pin 103 (**gep<1>/activ**) as an example. The CSR values provided in each line should be written in one CSR access.

E.1 Input Port Selection with Interrupt

To select the input port with the interrupt function, write the following values:

First write CSR15<27> = 1, CSR15<25> = 1, CSR15<21> = 0, CSR15<17> = 0

Then write CSR15<27> = 0.

E.2 Input Port Selection Without Interrupt

To select the input port without the interrupt function, write the following values:

First write CSR15<27> = 1, CSR15<25> = 0, CSR15<21> = 0, CSR15<17> = 0

Then write CSR15<27> = 0.

E.3 Output Port Selection

To select the output port function, write the following values:

First write CSR15<27> = 1, CSR15<21> = 0, CSR15<17> = 1

Then write CSR15<27> = 0.

E.4 LED/Control Selection

To select the LED/Control function, write the following values:

First write CSR15<27> = 1, CSR15<21> = 1

Then write CSR15<27> = 0.

F

Support, Products, and Documentation

If you need technical support, a *Digital Semiconductor Product Catalog*, or help deciding which documentation best meets your needs, visit the Digital Semiconductor World Wide Web Internet site:

http://www.digital.com/semiconductor

You can also call the Digital Semiconductor Information Line or the Digital Semiconductor Customer Technology Center. Please use the following information lines for support.

For documentation and general information:	
Digital Semiconductor Information Line	
United States and Canada:	1-800-332-2717
Outside North America:	1-510-490-4753
Electronic mail address:	semiconductor@digital.com

For technical support:	
Digital Semiconductor Customer Technology Center	
Phone (U.S. and international):	1-508-568-7474
Fax:	1-508-568-6698
Electronic mail address:	ctc@hlo.mts.dec.com

Digital Semiconductor Products

To order the Digital Semiconductor 21143 10/100-Mb/s Ethernet LAN Controller and for more information about an Evaluation Board kit, contact your local distributor. The following tables list some of the semiconductor products available from Digital Semiconductor.

Chips	Order Number
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (PQFP package)	21143–PA
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (TQFP package)	21143–TA
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller	21140–AC

Evaluation board kits include an evaluation board, and can include a complete design kit, an installation kit, or an accessories kit.

Evaluation Board Kits	Order Number
Digital Semiconductor 21143 PCI Evaluation Board Kit	21A43–01
Digital Semiconductor 21140A 10/100BASE-TX Evaluation Board Kit	21A40–TX

Digital Semiconductor Documentation

The following table lists some of the available Digital Semiconductor documentation.

Title	Order Number
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Product Brief	EC–QWC2A–TE
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Data Sheet	EC–QWC3B–TE
Using the Digital Semiconductor 21143 Boot ROM, Serial ROM, and External Register: An Application Note	EC–QYZ1A–TE
Digital Semiconductor 21143 Connection to the Network Using MII-based Physical Layer Devices: An Application Note	EC–QXY7A–TE

Title	Order Number
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Product Brief	EC–QN7MB–TE
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Data Sheet	EC–QN7PC–TE
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual	EC–QN7NC–TE

Third–Party Documentation

You can order the following third-party documentation directly from the vendor.

Title	Vendor
PCI Local Bus Specification, Revision 2.1 PCI Multimedia Design Guide, Revision 1.0 PCI System Design Guide PCI-to-PCI Bridge Architecture Specification, Revision 1.0 PCI BIOS Specification, Revision 2.1	PCI Special Interest Group U.S. 1–800–433–5177 International 1–503–797–4207 Fax 1–503–234–6762
Institute of Electrical and Electronics Engineers (IEEE) 802.3 and 1149.1	The Institute of Electrical and Electronics Engineers, Inc. U.S. 1–800–701–4333 International 1–908–981–0060 Fax 1–908–981–9667

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